# Analysis of Multiconverter - UPQC Configuration with Different Filtering Schemes for Shunt Compensation

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**Abstract:** Power quality (PQ) issues, such as voltage and current distortions, sag, swell and interruptions in supply voltage, pose a big challenge for the distribution systems. The increasing grid penetration of intermittent renewable energy sources has further complicated this issue. Unified power quality conditioners (UPQCs) can act as a comprehensive solution for these PQ issues by providing harmonic current mitigation, reactive power compensation and sag/swell alleviation. However, UPQC fails to maintain load voltage in case of interruption in supply voltage. Multiconverter-UPQC (MC-UPQC) topology addresses this drawback and maintains continuous power supply even during the grid failure by interline power feeding from adjacent live feeder. Synchronous reference theory is widely employed for the control of MC-UPQC. In such a scenario, the dynamic response of the MC-UPQC is significantly affected by the low pass filtering of the *d*-axis component of load current. This paper analyzes the dynamic response of MC-UPQC with different filtering methods. This analysis reveals that 2<sup>nd</sup> order Butterworth filter provides the best dynamic response for the shunt controller among the tested filter topologies. This is supported through the simulation and experimental studies presented in this work.

Keywords: Custom power devices, harmonics, power quality, unified power quality conditioner (UPQC)

#### 1. Introduction

With the increasing use of power electronics, the problems of current harmonics in the grid has greatly increased (Rönnberg & Bollen, 2016). This has further resulted in voltage distortion and power factor degradation. The combination of these issues has degraded the power quality (PQ). Furthermore, the PQ is further degraded by the sag, swell, flicker and interruptions in supply voltage (Valtierra-Rodriguez.M. et al., 2014). These PQ issues severely impact the system operation and loads by introducing increased losses, excessive temperature rise, perturbing torque in rotating machines, insulation failure, reduced system efficiency and power transfer capability(Gohil.M. & Sant.A.V., 2017). Hence, the mitigation of PQ issues is of importance.

Grid integration of renewable energy sources, such as solar and wind energy, is being employed across the globe and their installed capacity is increasing with each year (Kumar.V. et al. 2016). The reason behind the wider acceptance of the grid tied wind and solar energy is the increasing energy demand, depletion of fossil fuels, and global warming issues (Bose.B.K., 2013 & Sant.A.V. et al. 2015). Wind and solar energy based generation is highly sensitive to the atmospheric conditions, which affect the reliability of supply (Teh.J. and Cotton.I., 2016). Thus, though the grid integration of renewable energy systems reduce the reliance on coal based electric power generation, their intermittent nature and non-sinusoidal current injection, add to the existing complications related to the PQ issues (Arrillaga.J., 2000).

Different custom power devices are reported in literature to mitigate the power quality issues (Khadem, S. K. et al., 2010). Active power filters technology has significantly matured and is employed for harmonic current and voltage mitigation, and reactive power compensation. These power filters are implemented when the harmonic spectra is not fixed and varies due to variable loading and supply conditions. Based on the type of compensation, active power filters are mainly classified as (i) Shunt active filters - mitigate harmonic currents and compensate reactive power (Sant.A.V. and Gohil.M.H., 2019), and (ii) Series active power filter or dynamic voltage restorer - mitigate sag, swell and harmonic in supply voltage (Jayaprakash, P. et al., 2008 & Babaei, E. et al., 2010). Thus, shunt active filter employs shunt compensation to only mitigate the current related PQ issues, whereas dynamic voltage restorer employs series compensation to mitigate only the voltage related PQ issues (Singh.B. et al., 1999 & Singh.B. et al. 2009).

Unified power quality conditioner (UPQC) is a custom power device that combines the operation of shunt active filter and dynamic voltage restorer to deal with harmonic current and voltage mitigation, reactive power compensation, and voltage sag/swell alleviation(Teke.A. et al. 2011). References (Khadkikar.V., 2012, Mohammed.B.S. et al., 2013, Liu, Z. et al., 2018 & Fujita.H. et al., 1998) have reported different power structures and control systems for UPQC. UPQC caters to most of the power quality issues, but it is unable to address interruption in supply voltage. This shortfall is addressed by Multiconverter-UPQC (MC-UPQC) configuration which maintains continuous power supply even during the grid failure by interline power feeding from adjacent live feeder (Mohammadi.H.R. et al., 2009 & Karelia.N., 2019). Reference (Pappula.S.K. and Malaji.S., 2018) has reported MC-UPQC with interline feeding. Synchronous reference frame (SRF) theory is widely employed for the

control of custom power devices (Kesler.M. and Ozdemir.E., 2011, Kanjiya.P. et al., 2013, Bojoi.R. et al., 2004, Bhattacharjee.K., 2013, Kota.V.R. et al., 2016). Control of MC-UPQC with synchronous reference frame (SRF) theory is reported by (Naidu.P.V. and Basavaraja.B., 2012). In SRF theory based control, the dynamic performance of UPQC is greatly impacted by the low pass filtering of the *d*-axis current. This paper presents the detailed analysis of the dynamic response of MC-UPQC with different filter configurations under various operating conditions. Experimental study on the response of different filter configuration is also included in this work. Different types and orders of filters are considered in this study. The analysis of the *d*-axis current among the filter topologies considered. The simulation study validates the performance of MC-UPQC with the  $2^{nd}$  order butterworth filter based filtering of *d*-axis current results in operating conditions. In each of the operating condition the MC-UPQC with  $2^{nd}$  order butterworth filter based filtering of *d*-axis current results in operating that meets the IEEE standard 519.

# 2.12-Switch And Multiconverter Unified Power Quality Conditioner Topologies

The structure of conventional 12-switch UPQC comprising of two voltage source inverters for shunt and series compensation is shown in Fig. 1. In this configuration, two 6-switch voltage source converters (VSIs), individually employing series and shunt active filtering action, are connected back to back through a common dc link capacitor. VSC-I acts as a dynamic voltage restorer to mitigate the sag or swell in supply voltage to maintain the rated voltage at the load terminals. On the other hand, VSC-II acts as a shunt active power filter to implement shunt compensation for mitigating the current harmonics and providing reactive power compensation. Thus, the 12-switch UPQC configuration provides complete PQ solution by taking care of harmonic currents and voltages, reactive power demanded by the load and sag/swell in supply voltages (). However, it cannot handle the interruption in supply voltage. Under such condition, the UPQC cannot maintain the continuity of supply to the load.

MC-UPQC is one of the derived configurations of UPQC that can handle the interruption in supply. Besides this, MC-UPQC incorporates the features of the conventional 12-switch UPQC such as compensating anomalies related to source voltage, load current and harmonics mitigation without any need for a battery back-up (Mukassir.S.M. et al., 2018, Chaudhary.P. and Singh.G., 2020). The structure of MC-UPQC is shown in Fig. 2. This configuration comprises of VSC-I, VSC-II and VSC-III. VSC-I and VSC-III employ series active filtering connected to Feeder-1 and Feeder-2, respectively. VSC-II employs shunt active filtering for Load-1 connected at Feeder-1. It is to be noted that the MC-UPQC can be employed only in the case of availability of adjacent feeder. Feeder-1 and Feeder-2 are the two adjacent feeders feeding individual Load-1 and Load-2, respectively. VSC-II and VSI-II are connected in series and shunt to the Feeder-1 in the proximity of the Load-1.



Figure 1. Structure of conventional 12-switch UPQC

VSC-III is connected to the common dc-link of MC-UPQC. This converter is connected in series with the Feeder-2. Thus, MC-UPQC is connected to Feeder-1, through VSC-I and VSC-II, as well as Feeder-2, through VSC-III. This structure of MC-UPQC can allow for flow of power from Feeder-2 to Load-1 connected to Feeder-1.





Figure 2. Structure of MC-UPQC

Consider a scenario where the Load-1 and Load-2 are respectively being fed from Feeder-1 and Feeder-2. In such scenario, the three VSC operate in the following manner:

- (i) VSC-I operates to mitigate sag/swell and harmonics in the voltage being supplied by Feeder-1,  $v_{Fla}$ - $v_{Flb}$ - $v_{Flc}$ , so as to maintain the  $v_{Lla}$ - $v_{Llb}$ - $v_{Llc}$  at their rated values and free from distortions.
- (ii) VSC-II operates to supply harmonic currents and reactive power demanded by Load-1, so that the current being supplied by the Feeder-1,  $i_{Fla}$ - $i_{Flb}$ - $i_{Flc}$ , have distortions compensated within the limits specified by IEEE standard 519. This also results in currents being delivered at unity power factor.
- (iii) VSC-III operates to mitigate sag/swell and harmonics in the voltage being supplied by Feeder-2,  $v_{F2a}$ - $v_{F2b}$ - $v_{F2c}$ , so as to maintain the  $v_{L2a}$ - $v_{L2b}$ - $v_{L2c}$  at their rated values and free from distortions.

When the Feeder-1 supply is interrupted, Load-1 would not receive the requisite power to operate. In case, Load-1 is a sensitive load this can result in severe damage being sustained. In such case, MC-UPQC can operate to maintain supply to Load-1 by connecting it to the adjacent healthy feeder i.e. Feeder-2. Under such circumstances, the VSC operations are:

(i) VSC-I has no role to play and with the gate pulse not being provided.

(ii) VSC-II and III allow for interline feeding that results in the sensitive Load-1 being fed from Feeder-2. Thereby, ensuring the continuity of supply for sensitive load even under interruptions on Feeder-1.

# 3.Control Of MC-UPQC

Fig. 3 and 4 show the block diagram representation of the control system for shunt and series connected VSCs of the MC-UPQC. The sensed load currents,  $i_{L1a}-i_{L1b}-i_{L1c}$ , are first transformed into  $\alpha$ - $\beta$  reference frame with the help of Clarke transformation. The resulting  $\alpha$ - $\beta$  currents,  $i_{L1a}-i_{L1\beta}$ , are transformed to SRF with the Park transformation. This transformation necessitates the phase angle information associated with fundamental positive sequence component of voltages being supplied by Feeder-1. Phase locked loop (PLL), employing SRF algorithm,



Figure 3. Block diagram representation of control system for shunt connected VSC



Figure 4. Block diagram representation of control system for series connected VSC

processes the Feeder-1 voltages,  $v_{Fla}$ - $v_{Flb}$ - $v_{Flc}$ , to estimate the phase angle corresponding to fundamental positive sequence component of  $v_{Fla}$ ,  $\theta_1$ .

 $i_{L1d}$ - $i_{L1q}$  are individually comprise of ac and dc components as shown in (1) and (2), where,  $i_{L1dac}$  and  $i_{L1qac}$  are ac components of  $i_{L1d}$ - $i_{L1q}$  and  $i_{L1ddc}$  and  $i_{L1qdc}$  are the dc components of  $i_{L1d}$ - $i_{L1q}$ .

$$i_{L1d} = i_{L1dac} + i_{L1ddc}$$
(1)  
$$i_{L1q} = i_{L1qac} + i_{L1qdc}$$
(2)

 $i_{L1d}$  is further processed through a low pass filter to separate the two components and obtain  $i_{L1ddc}$ .  $i_{L1ddc}$  represents the fundamental positive sequence component of current being supplied by Feeder-1,  $i_{Ldf}$ .

The switching losses in VSC are responsible for a reduction in *dc*-link voltage  $v_{dc}$ , and hence, it needs to be regulated. Proportional-integral (PI) controller, shown in Fig. 3, processes the deviation in *dc*-link voltage,  $v_{dc}$ , from its reference value,  $v_{dc}^*$ . Based on the resulting difference,  $v_e$ , the PI controller determines the current to be drawn from the Feeder,  $i_{dcref}$ , to regulate the *dc*-link voltage at the desired value. The sum of  $i_{dcref}$  and  $i_{Ldf}$  is to be supplied by the Feeder-1. As shown in (3),  $i_{Ldf}$  and  $i_{dcref}$  are subtracted from  $i_{L1d}$  to obtain reference *d*-axis component for the VSC-II. With this the reference currents for the VSC-II in *d-q* reference frame are

$$i_{Ldref} = i_{L1d} - i_{Ldf} - i_{dcref}$$
(3)  
$$i_{Lqref} = i_{L1q}$$
(4)

The *d-q* axes reference currents, computed in (3) and (4), first undergo inverse Park transform followed by inverse Clarke transform to obtain reference current in *a-b-c* reference frame,  $i_{sharef}$ - $i_{shcref}$ . VSC-II is controlled to inject  $i_{sharef}$ - $i_{shcref}$ - $i_{shcref}$  so that the necessary harmonic current mitigation and reactive power compensation is achieved. By using PWM hysteresis current control, required gate pulses are generated for the VSC-II to inject necessary compensating currents in each phase.

The functions of the series VSC in each feeder are to mitigate voltage sag and swell, to compensate harmonics in the supply voltage and compensate interruption in Feeder-1. The voltages measured across the terminals of Load-1 are transformed into  $\alpha$ - $\beta$  reference frame using Clarke transformation. The resulting voltages,  $v_{L1\alpha}$ - $v_{L1\beta}$ , are

further transformed into d-q reference frame. The resulting d-q axes voltages,  $v_{Lld}-v_{Llq}$ , are compared with reference value  $V_{mref}$  and zero, respectively. The d-q axis voltage errors  $v_{ed}-v_{eq}$  are separately processed by the individual PI controllers.

The output of these PI controllers processing  $v_{ed}$ - $v_{eq}$ , are the d-q axis reference voltages,  $v_{1dref}$ - $v_{1qref}$ . These reference voltages are transformed into  $\alpha$ - $\beta$  reference frame,  $v_{1\alpha ref}$ - $v_{1\beta ref}$ , which are then further transformed in to the a-b-c reference frame,  $v_{1\alpha ref}$ - $v_{1\beta ref}$ . The sinusoidal pulse width modulation technique is used to generate gate pulses  $G_1$ - $G_6$  for the respective VSCs implementing series compensation in the respective feeders. The necessary voltage is injected in the feeder to affect the mitigation of sag/swell in feeder voltages using series injection transformer.

#### 4.Performance Analysis Of Different Filter Topologies

For shunt active filtering, the SRF theory is utilized for the extraction of compensating signal. In shunt compensation control, for the separation of dc and ac components of d-axis load current a low pass filter is generally employed. The slow dynamic response of low pass filter is a concern. In order to overcome this issue, the performance of different filter topologies is analyzed in this work. The five different filter topologies employed considered in this analysis are: (i) Butterworth filter, (ii) Chebyshev I filter, (iii) Inverse Chebyshev, (iv) Elliptical filter, and (v) Bessel filter. Table I shows the transfer function for these five filter configurations, where *n* is the order of filter,  $\omega$  is frequency of the signal,  $G_n$  is the filter transfer function and  $H_n$  is the gain,  $\omega_c$  is the cut-off frequency (approximately the -3dB frequency),  $G_0$  is the *dc* gain (gain at zero frequency),  $\varepsilon$  is a ripple factor,  $T_n$  is the chebyshev polynomial of the  $n^{th}$  order,  $\xi$  is a selectivity factor and  $R_n$  is the  $n^{th}$  order elliptical rational function,  $\theta_n$  is the reverse Bessel polynomial,  $\omega_n$  is the frequency chosen to give the desired cut-off frequency. For elliptical filter, the value of the ripple factor specifies the pass band ripple, while the combination of the ripple factor and the selectivity factor specify the stop band ripple. When analyzing the performance of the five filter configuration of different orders are analyzed based on the parameters, such as settling time, total harmonic distortion (% THD), maximum amplitude and % attenuation. The test signal, x(t) employed for analyzing filter performance can be stated as

$$x(t) = 15.5\sin(\omega t) + 3\sin(3\omega t + \phi) + 1.5\sin(12\omega t + \phi)$$
(5)

where, t is the time,  $\omega$  is the fundamental frequency and  $\phi$  is phase angle.

Filter	Transfer Function
Butterworth Filter	$G(\omega) = \left  H(j\omega) \right  = \sqrt{\frac{G_0^2}{1 + \left(\frac{j\omega}{j\omega_c}\right)^{2n}}}$
Chebyshev-I Filter	$G_n(\omega) =  H_n(j\omega)  = \frac{1}{\sqrt{1 + \varepsilon^2 T_n^2 \left(\frac{\omega}{\omega_0}\right)}}$
Chebyshev-II Filter	$G_n(\omega) =  H_n(j\omega)  = \frac{1}{\sqrt{1 + \varepsilon^2 T_n^2 \left(\frac{\omega_0}{\omega}\right)}}$
Elliptical Filter	$G_n(\omega) =  H_n(j\omega)  = \frac{1}{\sqrt{1 + \varepsilon^2 R_n^2 \left(\frac{\xi\omega}{\omega_0}\right)}}$
Bessel filter Filter	$G_{n}(\omega) =  H_{n}(j\omega)  = \frac{\theta_{n}(0)}{\theta_{n}\left(\frac{j\omega}{\omega_{0}}\right)}$

Table. 1. Transfer Functions of Different Filter Configurations







Performance Evaluation of 4th Order Filters



Performance Evaluation of 5<sup>th</sup> Order Filters



Figure 6. Performance evaluation of IV, V and VI order filter

Fig. 5 shows the performance of butterworth, chebyshev I, chebyshev II, elliptical and bessel filters of 1<sup>st</sup>, 2<sup>nd</sup> and 3<sup>rd</sup> orders when processing x(t). Similarly, Fig. 6 shows the performance evaluation of these filters for 4<sup>th</sup>, 5<sup>th</sup> and 6<sup>th</sup> orders. Settling time (ms), %THD, peak value and %attenuation for each filter configuration of different order are

plotted in Fig. 7. As the purpose of this analysis is to determine a filter that can be employed in shunt controller of MC-UPQC to extract the positive sequence fundamental active component of current, the accuracy of filter performance in terms of attenuating the higher order frequencies is critical. In case of all filters of order I, % THD is very high and hence, first order filter configurations are not considered for further evaluation.



**Figure 7.** Graphical representations of comparative analysis of different filter configurations







**Figure 8.** Comparative analysis of chebyshev I and II, elliptical and Bessel filters of different orders



Figure 9. Comparative analysis of butterworth filter of different orders

Settling time is the most important parameter with respect to the dynamic performance. II order butterworth and bessel filters have minimum settling time among the analyzed filter configurations. Hence, these two filter configurations need to be further analyzed to check their suitability for improving the dynamic performance of MC-UPQC. For any filter, it is essential to have minimum % attenuation for the fundamental component. Chebishev-I and elliptical filters offer the lowest attenuation. II order butterworth filter has marginally inferior performance in terms

of %attenuation, however it offers far smaller settling time. Same is the case with these three filters when their orders are increased.

Fig. 8(a-d) shows the graphical representation of comparative analysis of performance of each filter based on settling time, % attenuation, peak value and %THD for different filter configurations of order 1-6. Similarly, Fig. 9 shows the graphical representation of comparative analysis of performance of butterworth filter based on settling time, % attenuation, peak valueand %THD. Butterworth filter of order 1-6 are considered. On analyzing these two figures it is revealed that the II order butterworth filter offers optimal performance in term of settling time, %THD and %attenuation.



Figure. 10 Hardware set-up for comparative analysis



Figure. 11Hardware results showing response of IInd order filters

Fig. 10 shows the hardware test set-up. The performance of the different second order filter topologies for the given input signal is analyzed with dSPACE 1104. Fig. 11 shows the performance of different II order filter topologies available at the DAC terminal of dSPACE 1104 and observed on a digital storage oscilloscope. x(t) is considered for all the filters. The results of hardware implementation are conforming the simulation results. For dynamic performance improvement, the settling time is the main criteria which must be as least as possible. This apart, % THD must also be as least as possible as to filter out all the noise in the signal which will stabilise the output quickly. To avoid signal loss in a view to reduce the need for signal conditioning, %attenuation must also be least possible. Peak amplitude translates to the overshoot that is highly undesirable from stability point of view, hence needs to be as low as possible. Looking towards all these criteria, Fig. 6-8 and 11 clearly shows that II order butterworth filter provides optimal performance for the shunt controller action for MC-UPQC.

#### 5. Results And Discussion

The operation of MC-UPQC with II order butterworth filter for filtering the d-axis current in shunt compensation controller is analyzed in MATLAB/SIMULINK software. The system parameters are provided in the APPENDIX. Four different operating scenarios analyzed and presented in the succeeding paragraphs.

![](_page_9_Figure_5.jpeg)

**Figure. 12** Performance of MC-UPQC with the proposed control scheme with Feeder-1 feeding Load 1 at rated voltage

![](_page_9_Figure_7.jpeg)

Fig. 12 shows the performance MC-UPQC with II order butterworth filter for filtering the d-axis current in shunt compensation controller under normal operating condition. Feeder-1 supplies 3-phase balanced voltages at the terminals of Load-1. The maximum line-line voltage across Load-1 is recorded as 1 pu. With Load-1 being a nonlinear load, the load currents are non-sinusoidal with the THD of 10.83%. As the harmonic currents and reactive power demanded by the load is being supplied by VSC-II, the currents being supplied by the Feeder-1 is sinusoidal with THD less than 2%. VSC-I is not required to operate as there is no sag or swell in the supply voltage. Also, as Load-1 is being delivered the necessary power from Feeder-1, the VSC-III is not required to operate and hence, Load-1 remains disconnected from Feeder-2.

In the case 30% sag in the voltage being supplied by Feeder-1, as shown in Fig. 13, VSC-I of the MC-UPQC with the proposed control scheme is required to operate. When the peak value of voltage at Feeder-1 is reduced to 0.7, VSC-I mitigates this sag by injecting the necessary voltage through injection transformer so that the peak value of voltage across Load-1 is maintained at 1pu. Also, due to the nonlinear loading, VSC-II is required to provide the shunt compensation. This results in currents being supplied by Feeder-1 having a %THD of less than 5, which is in line with the IEEE standard 519. The peak values of load current, harmonic currents supplied by the VSC-II and Feeder-1 current are 0.66 pu, 0.34 pu and 0.61pu, respectively. VSC-I supplies 0.6 pu.

Fig. 14 shows the performance of MC-UPQC with the proposed control scheme under 20% swell in the Feeder-1 voltage. At 0.3 seconds, when swell occurs, the Feeder-A voltage attains the peak value of 1.2 pu. VSC-I is

controlled to inject voltage with the peak of 0.45 pu such that the phasor addition of voltages results in load voltage being maintained at 1 pu. As the load voltage is regulated at 1 pu, the shunt compensation implemented by VSC-II remains unaltered. The voltage across Load-1 is maintained at 1 pu without experiencing disturbance in spite of voltage swell at Feeder-1.

![](_page_10_Figure_3.jpeg)

proposed control scheme with Feeder-1 feeding Load 1 at 20% swell in supply

**Figure 15.** Performance of MC-UPQC with the proposed control scheme during interline feeding through Feeder-2 during the interruption on Feeder-1

Fig. 15 shows the MC-UPQC performance with the proposed control scheme when voltage interruption takes place on Feeder-1 at 0.3 seconds. During this period of interruption, the Feeder-1 voltage is zero. Standard UPQC is not designed to support the load under such condition. However, MC-UPQC allows for interline power feeding through an adjacent feeder. In this case, the adjacent feeder is Feeder-2. When interruption in supply occurs on Feeder-1, gate pulses to VSC-I are stopped. VSC-III, which was not having any effect on Load-1, is operated to connect the Feeder-2 with Load-1. VSC-III and VSC-II have common dc link. VSC-III transfers the power to the common dc link. VSC-II performs dc to ac conversion for feeding Load-1 at rated voltage. With interline feeding, the voltage at Load-1 is maintained at 1pu without any noticeable delay. Thus, the continuity of supply is maintained across Load-1 even in case of the power failure on Feeder-1. Moreover, with the proposed control strategy, MC-UPQC provides harmonic current mitigation, reactive power compensation and alleviation of sag and swell in supply voltage even during the time when the Feeder-1 is supplying Load-1. Thus, the MC-UPQC operation with the proposed control strategy provides the desired operation with fast dynamic response under different operating conditions.

#### 6. Conclusion

The standard UPQC topology cannot maintain the load voltage in case of interruption in supply. MC-UPQC overcomes this drawback through interline feeding to maintain the voltage across load terminal during the supply interruption. Thus, MC-UPQC provides continuous power supply for the load by feeding it from an adjacent feeder. The dynamic performance of MC-UPQC is significantly affected by the low pass filtering of d-axis current involved in the control of shunt compensation. In order to improve the dynamic performance, this paper analyzed the dynamic performance of MC-UPQC with different filter configurations, such as butterworth, chebyshev-I, chebyshev-II, elliptical and bessel filters. Filters of the order I to VI are considered and their performance are analyzed based on settling time, % attenuation, % THD and peak amplitude for optimum performance improvement. simulation analysis reveals that II order butterworth filter provides optimum performance. This simulation study is also verified by the dSPACE 1104 based experimental results. The performance analysis of MC-UPQC with II order butterworth filter is analyzed under sag/swell in supply voltage, nonlinear load and supply interruptions reveals IEEE compliant operation with improved dynamic performance and continuity of supply to load from adjacent feeder in case of interruption in supply on the feeder to which the load is connected.

# Appendix

# **A. Simulation Parameters**

AC supply voltage : 415 V, 50 Hz; Load : 25 KW (Non Linear); Ripple filter :  $R_f = 2\Omega$ ,  $C_f = 20\mu$ F; Reference *dc*-link voltage : 700 V DC; *dc*-link capacitance  $C_{dc}$ : 6800 $\mu$ F; Series PI controller I &II :  $K_p$ = 0.4,  $K_i$  = 200; Shunt PI controller :  $K_p$  = 20,  $K_i$  = 10; Interfacing inductor : 5mH

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