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*Research Article*

# Efficient MOSFET utilization of ALU for high speed applications

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**Abstract:** Full adders are the basic building blocks of various circuits like Central Processing Unit (CPU) and Digital Signal Processors (DSP). In this project design and implementation of high speed and efficient MOSFET's utilization of ALU is going to be done. ALU is the combination of 10T full adder, 10T 16 bit Ripple carry adder and Multiplexer, de-multiplexer and SRAM. All these are implemented and designed using GDI-technique. So, optimizing GDI technique and full adder in terms of delay let us achieve low delay circuits. The architecture utilizes adiabatic inverter for logic level implementation. The modified and proposed architecture designs reduce the stage delay, transistor count. In this complementary pass transistor logic presented and it will used to design a full adder circuit using XOR-XNOR design. From results, it can observe that the 10T full adder will reduce the number of MOSFET's compared to the 14T full adder. Along with that 10T 16 bit Ripple carry adder and Multiplexer and de-multiplexer and SRAM will reduce the utilization of MOSFET's. Hence, this project gives effective output.

**Keywords:** Full Adder, GDI (Gate Diffusion Input), MOSFET's, Ripple Carry Adder (RCA), Multiplexer, De-Multiplexer, SRAM (Static Random Access Memory).

## 1. Introduction (Times New Roman 10 Bold)

With technological advancements and furthermore the versatile applications extension, control utilization has turned into an essential focal point of consideration in VLSI advanced style. In this way Digital sub-edge circuit style is one among the most centre regions for low capacity to ultra-low power applications.

Basically, Arithmetic and logic operations are utilized in the high speed applications. Arithmetic operations are addition, subtraction, division and multiplication and logical operations are AND gate, OR gate, XOR gate and XNOR gate. The main intent of the arithmetic and logical operations is to provide the communication at high speed. Low-control style of VLSI circuits has been recognized as a system which will gratitude the extreme interest for transportable customer gadgets item. With the power consumption in Workstations, transportable individual correspondence frameworks and the advancement of the contracting innovation, the endeavor in low-control small scale gadgets has been extraordinary and low-control VLSI frameworks have developed with high demand. An improved structure should expend less power, have less engendering delay and stay away from any glitches in the yield. The configuration is likewise expected to be dependable on the low voltage supplies and diverse recurrence ranges [1].

Adder is one of the chief fundamental bits of Expansion for the normal and generally utilized essential number juggling activities in numerous VLSI frameworks. Other comparable arithmetic operations are subtraction, multiplication, division, address and so on. Using parallel adders the full adder is organized and improving 1-bit full adders execution expects a fundamental occupation in VLSI. Unmistakable varieties of full adders misuse absolutely exceptional reasoning constructions and advances. The battery driven and compact gadgets are interest of current industry application which needs an execution of low force and region productive gadgets. As shown by Moore's law increasing module center upon silicon wafer in the system [2-3]. The arrangement of interconnection restricted circuit thickness on a chip, anyway semiconductor door length is diminished to gigantic measurement. Today mechanical applications are organized in 2 nm range.

Low power and High speed are the designs which exchange offs in VLSI industry. Initially, the plan of full adders which shapes the essential building squares of all computerized VLSI circuits has been experiencing a significant enhancement, being roused by three fundamental structure objectives, viz. limiting the transistor tally, limiting the power utilization and expanding the speed. Most of the VLSI applications, for example, advanced flag preparing and microchips, utilize number-crunching activity.

Addition, subtraction, division and Multiplier and accumulate, are instances of the most normally utilized activities. The development of compact gadgets like PDAs, PDAs, and so on, request fast handling capacities that additionally expend less power. The1-bit full adder is the building square of these activity modules. In this way, improving its execution is basic for upgrading the general module execution. In this paper, we present a novel 1-bit full-adder cell utilizing XOR-XNOR circuit, which offers quicker activity, and devours less power than the other full-adder cell dependent on XOR-XNOR gates [4-5].(Times New Roman 10)

**2. Existed system**

The regular full adder with enormous number of semiconductor size could be utilized for improving the region, delay and the force. This could be a system which related construction to plan the full adders with the age of all the semiconductor sizes. The regular circuit couldn't be utilized for the general applications and the execution. The unit can't be prevailing for the gadget in the 14T adder. The below figure (1) shows the schematic of 14T full adder.

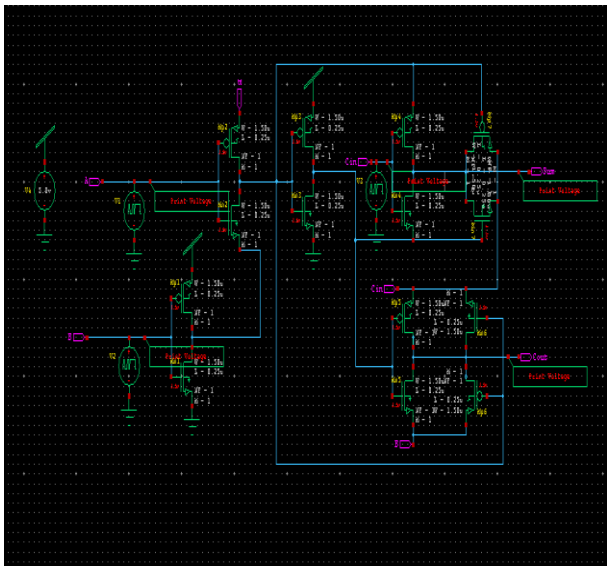

**Fig. 1: SCHEMATIC OF 14T FULL ADDER**

At first the hardware began their advancement with the innovation of adder. However , with the assistance of adder just the development of electrons was contemplated. After vacuum tubes transistors and diodes were presented. However , for bigger circuits it was hard to manufacture them in a board as they involved bigger space and devoured more power. The full adder circuit execution is subject to the methodology for structuring the circuit. The speed of activity of a circuit is in a roundabout way found with the assistance of defer time figuring which specifically relies upon the transistor check, the rationale profundity and other criteria. The power utilization relies upon the exchanging movement and the number of the transistor estimation. The below figure (2) shows the schematic of ripple carry adder with 14T full adder.

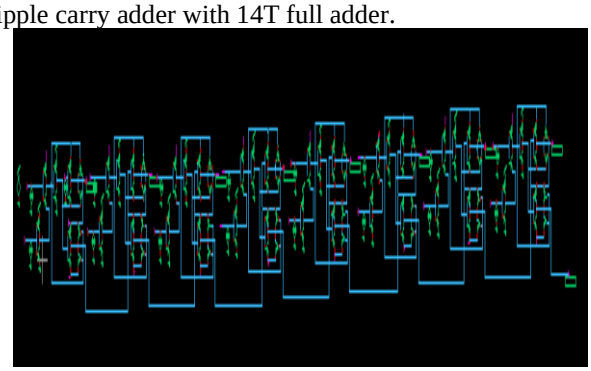

**Fig. 2: SCHEMATIC OF RIPPLE CARRY ADDER WITH 14T FULL ADDER**

The transistor measure and steering multifaceted nature knows the territory for circuits. An overview of writing uncovers a wide range of various sorts of XOR-XNOR gates that have been acknowledged throughout the years. The early structures of XOR-XNOR gates depended on either 4 transistors or 3 transistors that are utilized in many plans.

Full adder goes about as the essential square of all adders which are utilized to perform multi bit increases. There are additionally different approaches to plan the Full Adder circuit as far as CMOS rationale. With expanding request in speed and power, our principle point is to configure the full adder circuit so it devours less power and quicker. The vast majority of the power in any circuit is being devoured by the power given to the information way of the circuit which comprises of the transistors. Subsequently by lessening the quantity of transistors we can decrease the power utilization additionally by diminishing the information way, the circuit can be made quicker.

### 3. Proposed system

The below figure (3) shows the schematic of proposed system. The proposed system is new for FA circuits for different applications which have been appeared in Fig. 3. These new FAs have been utilized switch hybrid logic style, and every one of them is structured by utilizing the proposed adiabatic logic style. The notable four-transistor structure is utilized to actualize the proposed cross breed FA cells.

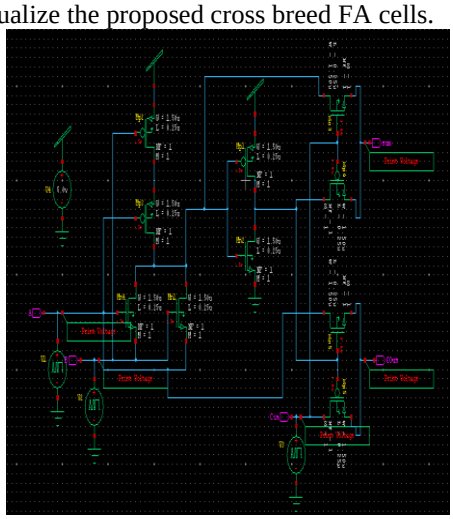

**Fig. 3: SCHEMATIC OF 10T FULL ADDER**

The full adder circuit is made with logic style that has no static and short out power dispersal. Hybrid full adder which has the power utilization NOT gates on basic way and comprises of 20 transistors. The benefits of this structure are full-swing yield, low power scattering and extremely rapid, strength against supply voltage scaling, and transistor estimating. In the event that A B = 1, at that point the yield Cout flag equivalents to the info flag An or Yet, to level the information sources capacitance, both of the information flags An and B are utilized for execution and are associated with the transistors N9 and P10 individually. The below figure ($) shows the schematic of 4×1 multiplexer.

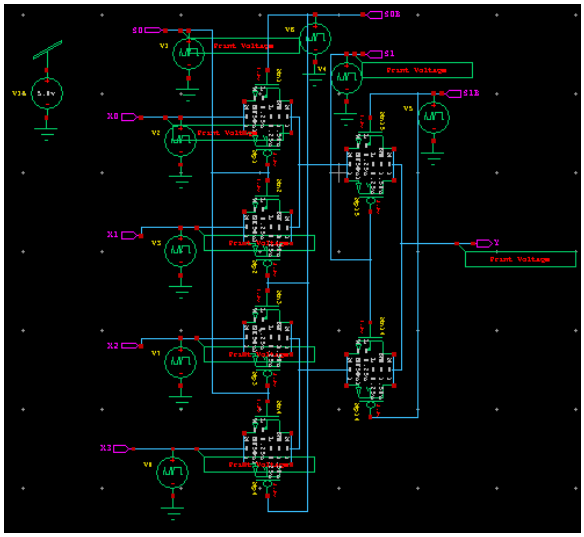

**Fig. 4: SCHEMATIC OF 4×1 MULTIPLEXER**

The main issue of hybrid full adder will decrease the output driving capacity when it is utilized in the chain structure applications, for example, swell convey adder. Obviously, this issue obtained in the circuits has the

utilization has the transmission work hypothesis in their usage without buffering yield. One approach to diminish the power utilization of the FA structures is to utilize a XOR/XNOR gate and NOT gates to produce the other XOR or XNOR flag. It might be normal that the power utilization of full adder is not as much as that of FA because of the decrease in the quantity of transistors. The below figure (5) shows the schematic of 4×1 de-multiplexer.

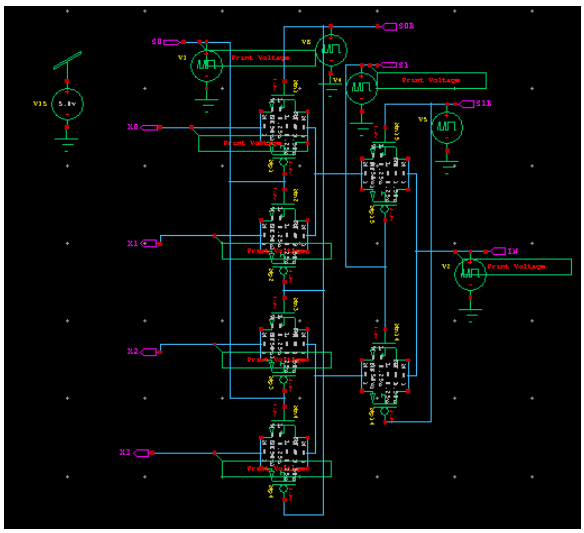

**Fig. 5: SCHEMATIC OF 4×1 DE-MULTIPLEXER**

However , the NOT gate on the basic way of the circuit expands the short out power. So there is no delay decrease in all out power dissemination of the FA. Additionally, the NOT gate will marginally enhance the yield driving capacity of the circuit. The below figure (6) shows the schematic of ripple carry adder with 10T full adder.

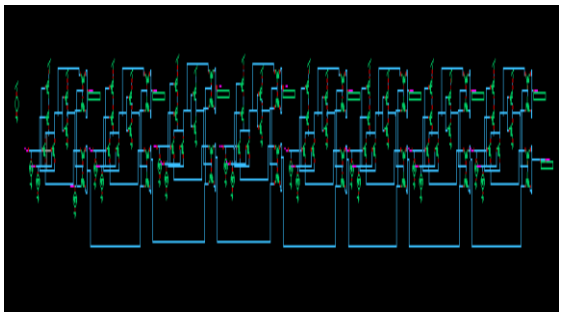

**Fig. 6: SCHEMATIC OF RIPPLE CARRY ADDER WITH 10T FULL ADDER**

The schematic of ripple carry adder with 10T full adder, utilizing the cushion on the yield of a circuit is practically required, particularly in applications that the output capacitance of each stage is high. Hence, the driving ability of VLSI circuits is corrupted because of the production of parasitic capacitors and resistors during manufacture, just as expanding during edge voltage of transistors over the time, however the yield support enhances this circumstance.

Hence that the info signs are created by the cradle, at that point for all conceivable information mixes, the Sum and $C_{out}$ yields are not driven by the contributions of the circuit. To do this work, three extra NOT gates are sufficient, in light of the fact that there was at that point the A flag and can be made the cushioned A flag with an additional NOT gate. So the capacitance of XOR and XNOR hubs are small, and the postponement of the circuit will be made strides. With the progression of innovation and diminished transistor sizes, the conduct and execution of a circuit couldn't be examined without transistor estimating, since a little change in the extent of transistors may significantly change the execution of the circuit. Accordingly, picking the proper strategy for transistor measuring, before acquiring the vital parameters of the circuit is essential.

**4.Results**

The below figure (7) shows the output waveform of 14T full adder.

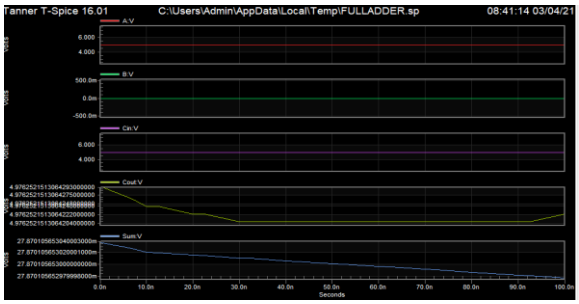


**Fig. 7: OUTPUT WAVEFORM OF 14T FULL ADDER**

The below figure (8) shows the output waveform of Ripple carry adder with 14T full adder.

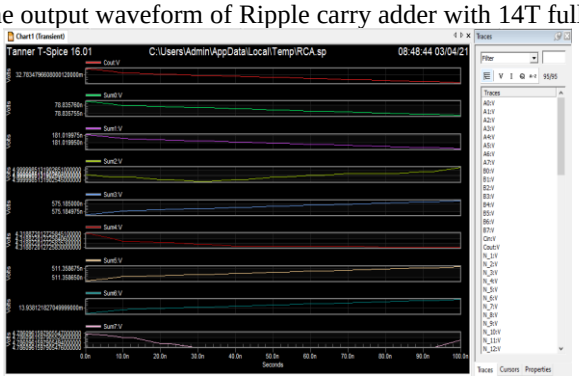


**Fig. 8: OUTPUT WAVEFORM OF RIPPLE CARRY ADDER WITH 14T FULL ADDER**

The below figure (9) shows the output waveform of 10T full adder.

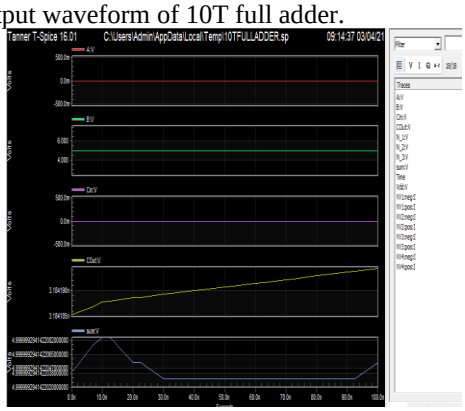


**Fig. 9: OUTPUT WAVEFORM OF 10T FULL ADDER**

The below figure (10) shows the output waveform of 4×1 multiplexer.

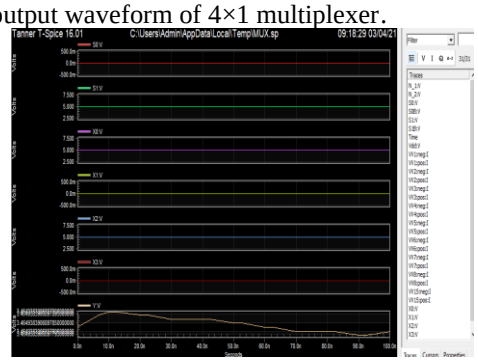


**Fig. 10: OUTPUT WAVEFORM OF 4×1 MULTIPLEXER**

The below figure (11) shows the output waveform of 4×1 De-multiplexer.

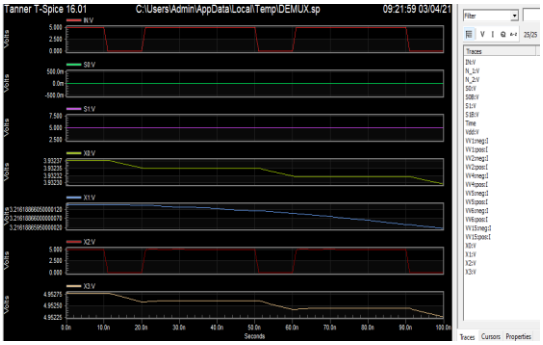


**Fig. 11: OUTPUT WAVEFORM OF 4×1 DE-MULTIPLEXER**

The below figure (12) shows the output waveform of Ripple carry adder with 10T full adder.

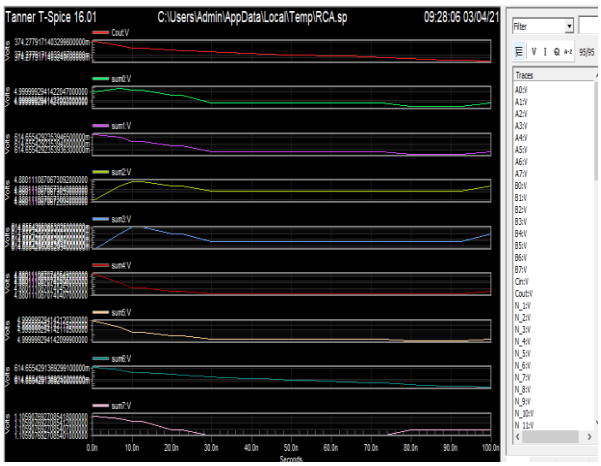


**Fig. 12: OUTPUT WAVEFORM OF RIPPLE CARRY ADDER WITH 10T FULL ADDER**

In the proposed ALU design multiplexer, de-multiplexer and SRAM designs are also implemented along with full adder and ripple carry adders the below table (1) shows the comparison of proposed and existed design. In this full adder and ripple carry adder MOSFET utilization is given in detail manner.

**Table. 1: COMPARISION TABLE**

| **Design** | **Proposed Design** | **Existed Design** |
|---|---|---|
| Full Adder | MOSFETs - 10 | MOSFETs - 14 |
| Ripple Carry Adder | MOSFETs – 80 | MOSFETs - 112 |

## 5.Conclusion

Hence in this paper efficient MOSFET's utilization of ALU for high speed applications was done. ALU is the combination of 10T full adder, 10T 16 bit Ripple carry adder and Multiplexer, de-multiplexer and SRAM. All these are implemented and designed using GDI-technique. This reduces the number of MOSFET's in very effective way.

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