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Research Article

Design of power management technique for WSN application with configurable architecture

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Abstract: The demand for high performance Wireless Sensor Network(WSN) is growing and its power dissipation has scarce the life of WSN. Wireless Sensor Network(WSN) needs the development with power efficient deployment. In WSN sensor nodes are remotely placed with inadequate energy budget, so this proposed work mainly focus development of an effective power saving scheme for wireless sensor node using FPGA configurable architecture. Design and implementation of hybrid power management scheme (DVFS + Clock gating) is presented in this paper. It performs functionalities like to activate power management unit as per the state of application tasks under execution. In this work, the power consumption of proposed implementation on FPGA for sensor node is compared with the power consumption of the processor based implementation of sensor nodes. The obtained result shows that the power consumption of hybrid power management technique is drastically reduced

Keywords: Power saving, DVFS, Clock Gating, FPGA

1. Introduction

Power consumption is a big challenge in modern day world. All portable devices are run on battery power like, laptop, mobile, PDA. So, the circuits embedded in devices must be with low power consumption. In 70s and 80s area and delay are much important features, but there is tradeoff between area and delay. If circuit becomes complex, testing becomes complex. Design of testability must be included in design. But from 2000 onwards, number of portable devices with increased power consumption becomes an important issue. More power dissipation leads to increase in temperature which is inacceptable in case of wearable embedded system. Due to increase in temperature device failure rate is improved. It affects the reliability of system. So, it is required to reduce the power consumption of portable devices due to design metrics of embedded systems such as size of system, reliability, inefficiency due to number of resources, high performance requirements.

It is possible to reduce power at device level (transistor level) or at much higher level architecture level. Whenever we design a circuit at higher level we can take some design decisions that can affect power consumption.

The power dissipated in CMOS circuits is combination of dynamic Power and static Power. It is specified by following equation:

$$P_{Active} = \text{Static power} + \text{Dynamic Power}$$

$$P_{Active} = I_{Leakage} V + C_{eff} V^2 f \quad (1)$$ where, V: Voltage, C_{eff} : load capacitance, f : Frequency, $I_{Leakage}$: Leakage current

The techniques required for reducing dynamic power as well as static power.

Reduction of dynamic power:

By considering equation of the dynamic power the power will be reduced by reducing α - the activity factor, by reducing load capacitance C, by reducing clock frequency f or by reducing supply voltage. Reduce α : there are some techniques like clock gating and sleep mode are used to reduce the activity factor.

2.Related background:

This section is aimed to provide a review of past theoretical work important to power management techniques and configurable architecture. The need for reducing power consumption in embedded system is increasing, that can be implemented at system level and architecture level.

i. Clock Gating : It is one of the power saving method used in many systems. It facilitates reduction in dynamic power consumption by disabling the portion of circuitry to reduce state transitions. L. Benini et al. [1] have done work on clock gating. It includes many aspects like the sequential element selection, governing the

clock skew, auto gated flipflops for look ahead clock gating. This technique is applied at all levels in system architecture like block design, logic design. The probabilistic model of the clock gating network is generated based on the system mathematical model which gives more power saving. **ii. Dynamic Voltage Frequency Scaling(DVFS) Technique :** DVFS method is used to reduce leakage as well as dynamic power consumption. DVFS [2-3] is a method for altering the frequency of system along with scaled voltage by considering performance and power requirements. Ajit Pal [4] has introduced a general model of DVFS based on workload traces is as shown in fig. 1. The DC/DC converter is used to set the required voltage and frequency generator is used to set the required frequency. The effect of DVFS on power consumption with different workload is as shown in fig. 2. **a. Microprocessor based DVFS :**

Modern microprocessors come with the built-in support for DVFS. A number of new microprocessors such as ARM1176JZF-S, ARM CortexA9, AMD-K6TM-2E+Processors Intel M series, Transmeta Crusoe are equipped with the DVFS functionality.

In most of the microprocessors or microcontrollers DVFS is implemented by considering different ways like temperature aware DVFS, energy harvesting based DVFS, performance aware DVFS.

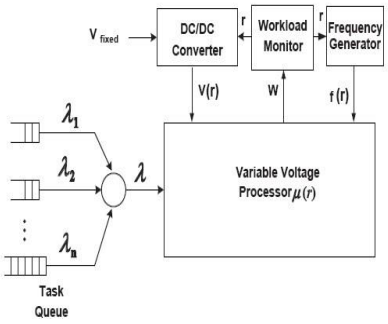

Figure 1: General Model for DVFS

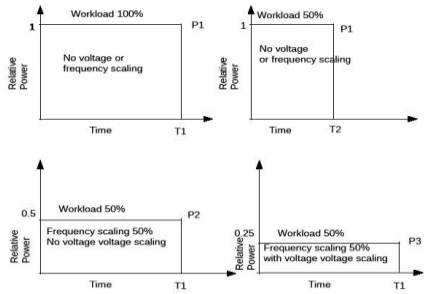

Figure 2 : Effect of DVFS for different workloads

In various embedded systems, high performance processors are used to support different system operations. This will increase the power consumption which finally resulting in heat problems. In order to recover the heat problems off-the-shelf devices, microprocessors rely on DVFS based dynamic thermal management schemes. Jae Min Kim et al. [5] has implemented temperature aware DVFS to avoid the problem of heat.

To overcome the limit on power availability energy harvesting is a capable method in order to improve the life of battery-powered embedded systems. Yi Xiang et al. [6] has considered this approach to save energy with DVFS. Runtime power management framework is provided with energy harvesting and DVFS.

Due to poor performance and unreliability of temperature-aware methods, novel performance constraint-aware DVFS method reduce the uneliability is presented by Rong Ge et al. [7]. He has developed the PEACH (Performance and Energy Aware Cooperative Hybrid computing) model for the same purpose i.e. to maintain performance. In above mentioned methods of DVFS are only applied to microprocessors, microcontrollers or COTS devices. However, these authors had not explored the issue of power management in soft core processors. **b. FPGA based DVFS :**

Field Programmable Gate Array (FPGA) technology is acquiring importance for embedded systems. Power reduction in FPGAs become essential to build reliable embedded system. Implementation of DVFS is explored for programmable logic like fine grained DVFS, look ahead DVFS etc.

Paolo Mantovani et al. [8] and Stigin Eyerman et al. [9] have introduced fine grained DVFS for FPGA platform. This technique is applied either to computationally intensive or memory intensive operations. FPGA-based infrastructure that explores analysis of high-performance embedded systems SoCs supporting multiple independent voltagefrequency (VF) domains is proposed. Each VF domain contains probes which detect the idle time due to congestion or unavailable access to memory. DVFS technique with different policies like policy none(*PN*), policy traffic(*PT*), policy burst(*PB*), policy limit(*PL*) is implemented. Analysis between coarse grained and fine grained DVFS is explored by Stigin Eyerman et al. [10]. DVFS technique is implemented by using on chip regulators on FPGA platform which will help to reduce delay introduced due to off chip regulators. Tao Chen et al. [10] has proposed a DVFS framework for hardware accelerators. In which look ahead approach of DVFS is used for power saving. The execution time of task is predicted by the predictor and sets a voltage & frequency level to meet the requirements. In same way Adaptive Voltage Supply (look ahead approach) which is applied to motion estimation processor is implemented for power saving by Jose Luis et al. [11].

These above mentioned methods like fine grained DVFS, look ahead DVFS are only applied either at accelerators, SOCs, or to motion estimation processor. However, these techniques are not applied to soft core processors. After reviewing various power saving techniques at microprocessor or FPGA level, it is observed that many of the researchers have implemented either DVFS or clock gating for reduction of power consumption. However no one has explored the hybrid power management technique which will utilize DVFS and clock gating in coordination with state identification of processor.

3. Methdology:

3.1.Hybrid Power Management scheme :

The functionality of this scheme is to provide power saving through DVFS or clock gating as per control signals given by cooperative unit. Power dissipation mainly depends on signal transition in activity in the circuit and the clock is responsible for activity in the circuit. Clock is triggering all parts of circuit. If any part of the circuit is not working currently, its clock will be disabled, so that for the respective part the signal switching will be reduced means the power dissipation will be reduced. Hence clock gating is considered as very simple technique to significantly reduce power. DVFS is also another power saving technique which will scale the voltage & frequency as per requirement. Algorithmic flow of proposed hybrid power management scheme is as shown in fig.3

Parameters considered for scaling model are,

Task set (*Ti: T_1, T_2, T_3*): TEA,CRC,RLE algorithms developed as custom instructions.

frequency range = f_{min} - f_i - f_{max}

Voltage range = V_{min}- V_i -V_{max}

Processor scaling model $(f_{min}, \beta, \Delta f, f_{max})$ would be,

β = Scaling $\beta = (\beta_1, \beta_2, \beta_3, \ldots\ldots, \beta_n)$ Coefficients,

Δf: the step that the frequency can be varied

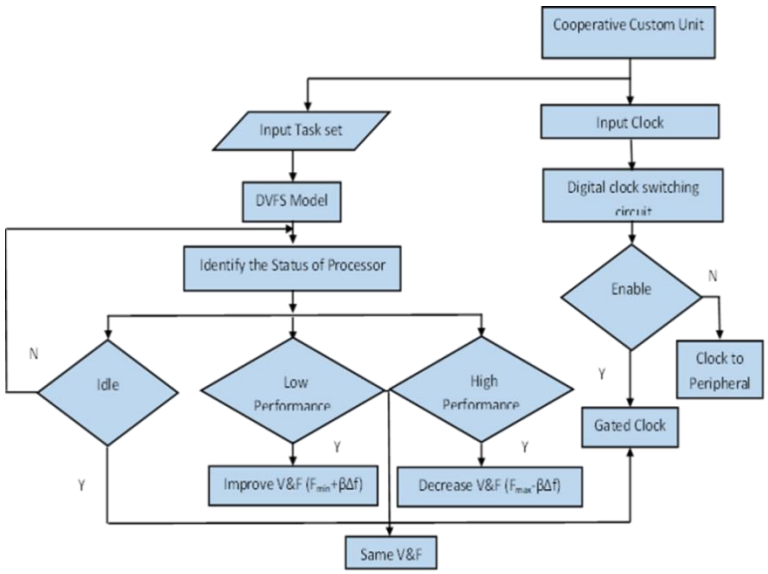

Figure 3. Algorithm flow of the hybrid power management scheme

4.Implementation:

Initially the module is simulated only with basic DVFS technique, then the same module is implemented with clock gating technique. Later the module of basic algorithms is simulated & implemented with the proposed power management scheme by hybrid method of integration of DVFS & clock gating as per the state identification of processor.

This simulation is performed using modelsim simulator. The functionality checking and verification of code is done using simulation. Fig.5 shows the modelsim simulation of proposed technique.

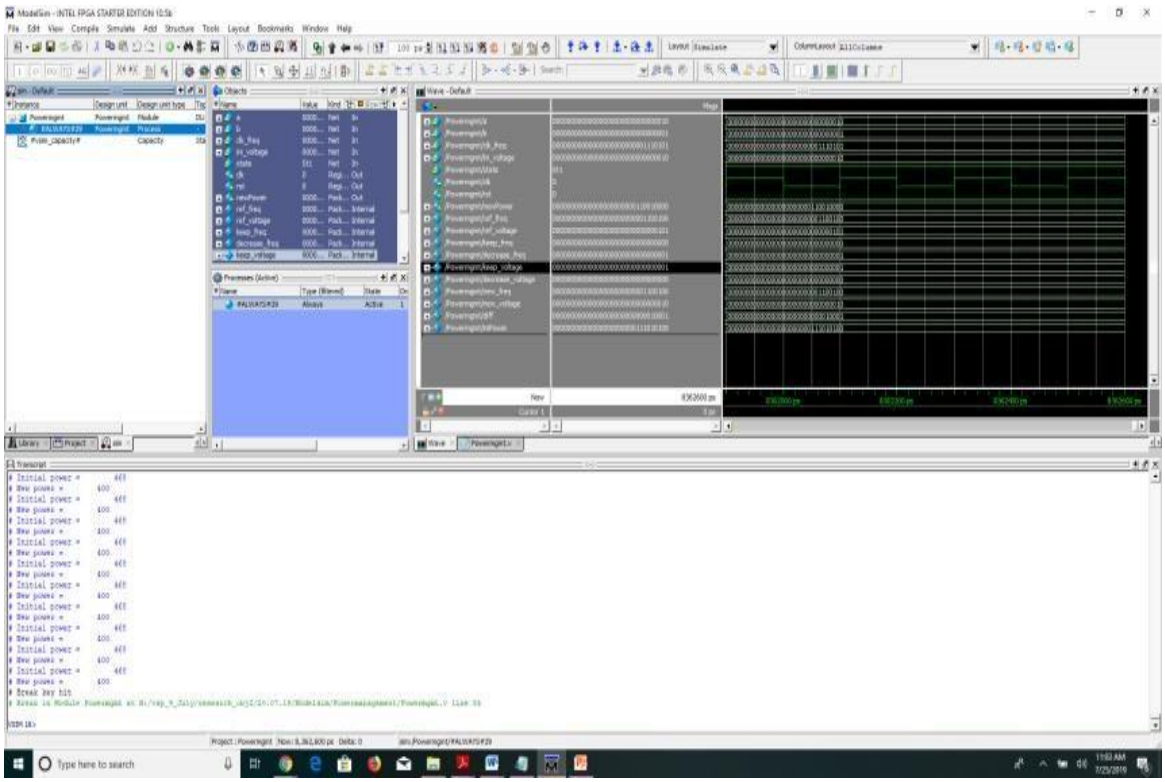

Fig. 4 functionality verification of power management using modelsim

Three basic algorithms of WSN application i.e. TEA, RLE, CRC are considered as basic task set for implementation of power management unit. These customized algorithms are executed with application of all modules i.e. with clock gating only, with DVFS, and with proposed hybrid power management unit. The project is

build & compiled with Xilinx vivado tool. Then the project is implemented on FPGA platform. Fig. 5 & 6 shows the RTL block design of proposed technique with simulation in vivado platform.

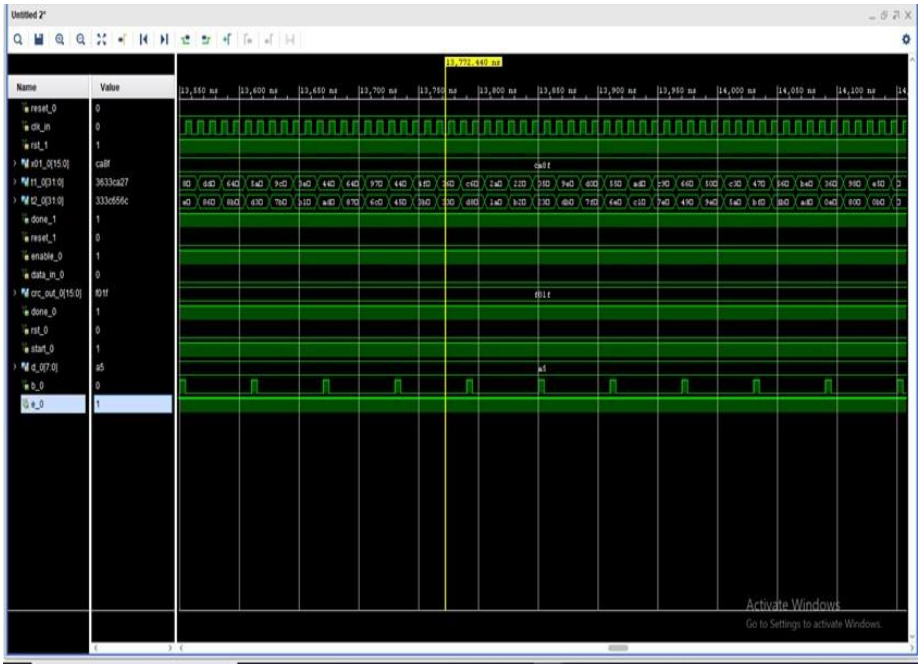

Fig.5 Simulation of power management with customized tasks

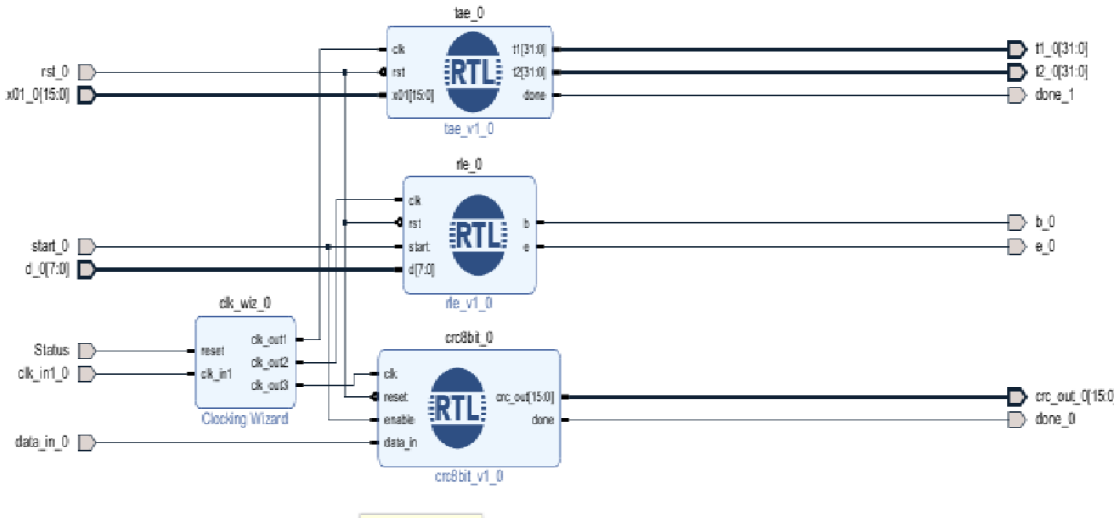

Fig.6. RTL block diagram of power management scheme

5. Result & analysis:

In this section, the details of the results and experimental analysis are presented. The comparison and analysis is done with the help of parameters like power consumption, resource utilization like slice logic, LUT logic, registers. The implementation results of proposed technique and comparison with two basic techniques for power consumption is as shown in table no.1

Table no.1 Comparison of power consumption

Method	**Power consumption(mw)**		**Total Power(mw)**
	Dynamic Power	Static Power	
With DVFS only	1.083	0.124	1.207
With Clock Gating only	0.623	0.115	0.738
Hybrid Power Management	0.356	0.116	0.465

Fig. 8 shows that power consumption of proposed implementation is less w.r.t. implementation with clock gating only. As well as it is drastically reduced as compared with implementation using DVFS Technique.

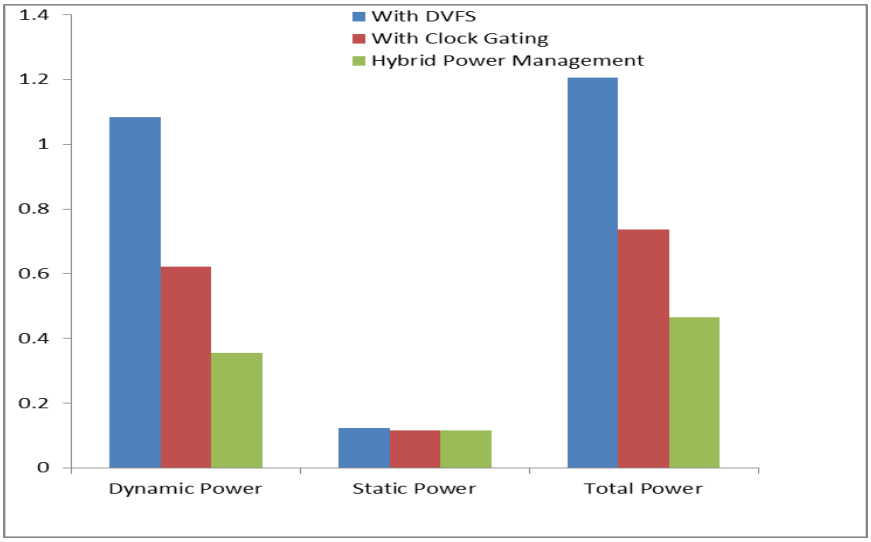

Fig. 7 Comparison of power consumption

The results of power saving for proposed implementation is compared with earlier microcontroller based and FPGA based power saving techniques. The result shows that there is average 35% improvement in power saving as compared to microcontroller based power saving as well as 40% w.r.t. FPGA based power saving technique.

Table No. 2 Comparison of power saving

Type	**Model**	**Power saving (in %)**
Microcontroller based DVFS [5]	DVFS	12.7
Microcontroller based DVFS [6]	DVFS	45
FPGA based DVFS [8]	DVFS	23
Proposed Technique FPGA based DVFS	DVFS + Clock Gating	55.69

Hardware Utilization: The Hardware utilization of proposed technique in terms of slice logic, LUT logic , registers and I/O is as shown in following table.

Table no.3 Comparison of hardware utilization

Hardware Component	**With DVFS**	**Hybrid Power Management Unit**
Slice logic	9873	11758
LUT Logic	9602	9609
Registers	158	223
I/O	113	116

6.Conclusion:

In this paper, the hybrid approach for power saving of WSN node with FPGA platform by considering specific task set of WSN application is implemented. This approach is based on the tasks implemented as hardware blocks with application of power saving technique.

The implementation is carried with three approaches with clock gating only, with DVFS only and then with proposed hybrid technique. The result power saving with proposed implementation is improved by 55.69%. The results are also compared with earlier FPGA based power saving techniques which leads to improvement of 32.69%. In future, we would also like to explore the state identification technique by implementation of customized RTOS acceleration.

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