Performance Analysis of High Speed Inexact Speculative Adder

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Abstract: A high-speed model of the recent Inexact Speculation Adder(ISA) design is presented in this paper. Also a fine grain pipeline and clock gating is included in this architecture to improve its speed and reduce the power consumption respectively. Simulations of the pipelined ISA, pipelined Speculator, PCLA and pipelined Compensator are presented. The pipelined ISA, pipelined Speculator, pipelined CLA and pipelined Compensator incorporated with the power saving techniques of sleep, stack and sleep stack approaches are also presented. HSPICE is used for stimulation and the required parameters such as delay average power, and power delay products are acquired and presented. It is observed that due to the application of the low power techniques of sleep, stack and sleepy stack, the power delay product has been reduced by 80% compared to the carry-look ahead adder (CLA) based design of ISA.

Keywords: Inexact Speculation Adder, Pipeline, PCLA, Speculator,Compensator.

1. Introduction (Times New Roman 10 Bold)

In the modern electronics era sophisticated signal processing's are being incorporated using the VLSI circuits. The circuits performing signal processing's are not only demanding complex computations but also consume more amount of energy. Hence the need for low power circuits are abundant since the number of operations being done is very large with very high frequency and it needs cooling. Now a days all electronics equipment becomes handy and portable. For its operation stored power in the form of battery is required. In order to ensure the proper operation and reliability, the portable devices needs considerable peak power considerations in its design. However the charge of the battery depends on the time averaged power and it is more important. Hence the life of such portable equipment's depend on the charge of the battery.

There are four sources of power dissipation in digital CMOS circuits: switching power, short-circuit power, leakage power and static power.Present day digital circuits are using more arithmetic operations such as addition for producing an output. Hence digital adders **(SubodhWairya et al.,2011)**are being used widely in electronic applications and he applications which need digital adders are multipliers, Microprocessors ,DSP processors, etc. Since it is known that millions of instructions are executed per second in processors, the performance of multipliers should be considered in terms of its speed and power consumption. The performance of some of the adders are mentioned as follows. Compact design is exhibited by Ripple carry adders it is slow in its speed **(G. Sasi et al.,2019).** Carry look ahead occupies more area but it is fast**(JagannathSamanta et al., 2013).** But the carry select adder functions as a balance between the two said adders **(Mohammad Khadir et al., 2020).**

A hybrid adder design with carry look-ahead or carry select adder is presented **(Yuke Wang et al., 2002 and PadmanabhanBalasubramanian et al., 2018)** in order to improve the speed of addition. However the area efficient and power efficient logic systems designs are one of the emerging areas research in VLSI system design. The pace of addition is restricted by the propagation of carry in digital adders. A carry is sequentially generated and propagated to the next position only after the sum of the previous bit positions are completed in an elementary adder.To reduce the carry propagation delay the carry save look aheadadder**(Ravikumar A Javali et al., 2014)** is used in most computational systems which generates multiple carries independently and choose the appropriate carry and generate the sum.

The present era demands the high speed adders ,though power and area are equally important.It is possible to come out with a high speed adder with low power using approximate and inexact circuit technique **(Vincent Camus et al., 2015)**.A trade off can be considered on accuracy on such circuits to enhance the speed and power by speculation. This type of adders are cited as inexact speculative adder. The literature reports a lot of such ISA**(R. Priyaet al., 2013, ShivaniParmeret al., 2012 , I-Chyn Wey et al., 2012, B. Ramkumar et al., 2012 and S.Manjui et al., 2013)**. However, further improvement in the speed of such adders are in need by retaining the exactness with minimum error. This work concentrates on pipelined carry look ahead adder(PCLA) based ISA

and it is further enhanced by adopting the low power techniques such as clock gating, stack approach , sleep approach and sleepy stack approach without changing the architecture.

2. Proposed Architecture of Inexact Speculation Adder

Figure 1 shows the block diagram with data flow of traditional ISA for n-bit addition. In order to enhance the speed of the circuit , the adder unit is modified with 4-bit CLA. This architecture consists of the following sub blocks 1) Speculator and Adder Blocks: It has two n-bit operands which are required for addition and they are expressed as A = {$A0$, $A1$, ...−1} and B = {$B0$, $B1$, ...Bn−1}; while, the carry input, carry output and the sum are expressed as Cin ,$Cout$ and S = {$S0$, $S1$, ...Sn−1}, respectively.

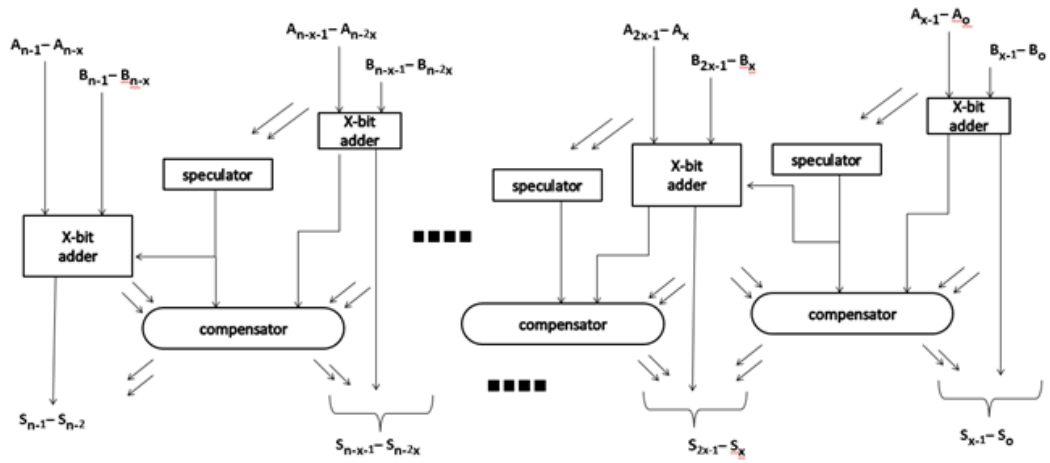

Figure.1. Block diagram of Inexact Speculative Adder

Fig 2. shows the circuit diagram of the adder design with speculator.This block uses the CLA logic for speculating the carry output in every block of 4-bit adder. Speculation is fetched out for 'r' msb bits in each block , where the size of block is greater than 'r', (i.e., r < x = 4). Eventually, the errors may be positive or negative and are introduced by the input carry (0 or 1) for each speculator block .The output carry is denoted by Cso for each and every speculator block and this carry is fed as input carry to the succeeding adder block. Hence there is no need for the 4-bit adder blocks to wait for the carry input which arise from the previous block of 4- bit adder.

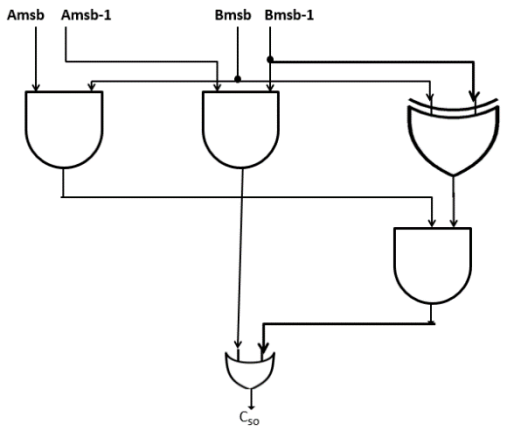

Figure.2 Gate level Speculator circuit

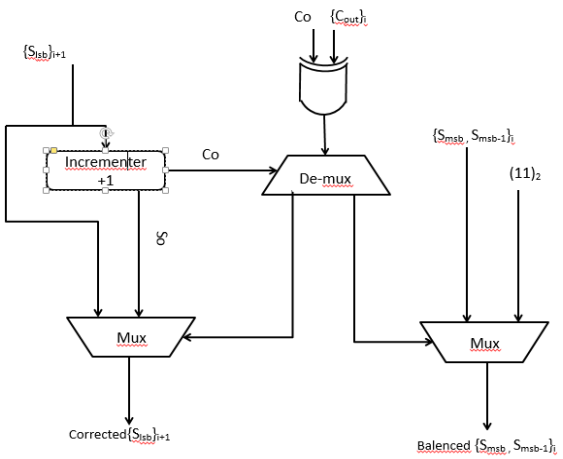

Figure.3 Comparator Block

Rather, the concerned speculator blocks provide the required carry simultaneously for all adder blocks to perform simultaneous additions. The computation in Speculator block is based on the equation as follows:

$$Pi = Ai \oplus Bi \;;\; Gi = Ai \;.Bi \;; Ci + 1 = Gi + (Pi \,.Ci) \qquad (1)$$

Where (i+1)th carry bit is calculated using the carry (Ci) , generate (Gi) and the propagate (Pi), of ith bit.
This block is present through the critical path of ISA architecture, and also it computes the carry for few bits, it wont produce much delay. In the same time the CLA logic perform the addition of 4-bit input in the adder block and the equation used for this addition is shown below.

$$Si = Pi \oplus Ci \quad (2)$$

The sum output is not the exact output from each parallel adder block, because the speculated carry inputs are used to perform addition. The compensator block performs the job of correction of such sum value and is shown in fig1. Maximum delay is being incurred by the adder and compensator blocks in the architecture.Inorder to reduce the delay the pipelining technique is used. Inorder to reduce power the power reducing techniques of sleep,stack and sleepy stack techniques are also followed.Figure 3 shows the compensator block architecture used in the ISA adder. In this block a comparison of carry output from each and every 4-bit adder block is done with the speculated carry with the help of an XOR gate.

Hence ,XOR gate generaes an error flag (fe) at its output which enables any one of the two compensation techniques.The compensation techniques are error correction and reduction techniques. If the XOR-gate output is '0' the sum value is directly routed to final output.Otherwise if it is 1, it indicates an occurrence of an error which may be positive or negative.

A low sum is induced due to the speculation of '0' instead of '1' which is indicated by a positive error. Similarly high sum is induced due to the speculation of '1' instead of '0' which is indicated by a negative error. An unsigned decrement or increment is done by the compensation block to the set of LSBs towards the error direction. Correction can be performed only if no overflow occurs.On the other case if any overflow occurs a set of MSBs of the previous sub-adder is balanced by the compensation block in the direction opposite to that of the error.
The balancing is carried out considering the condition as follows

$$2n > \{2n + 2n\text{-}1 + 2n\text{-}2 + ...+ 20 \} \quad (3)$$

Suppose if the sum is resulted in $2n$ errors then it can be compensated by causing LSB errors intentionally in the converse direction (for example, $Sn{-}1 = 1 \rightarrow Sn{-}1 = 0$). Thus if each and every LSBs are balanced in the converse direction, the overall error is decreased in to 1,as shown below

$$\{2n - 2n\text{-}1 - 2n\text{-}2 - .....- 20 \} = 1 \quad (4)$$

The correction or balancing in the compensation block will be completed before the 4-bit adder block completes calculating the sum total of all the other bits. An important characteristics of this ISA adder is that both the compensation and the pre-computing of error correction are not present in its critical path. However the XOR gate, multiplexer.and de-multiplexer are present in the compensation block of the ISA in its critical path. In the proposed design, clock gating is done in order to fetch the clock signal into every stage. On performing this modification, the ideal stages of the architecture can be varied from clock switching which significantly reduces the power consumption. Such gating is valid only during the beginning and ending sessions of the addition process **(PadminiG.Kaushiket al., 2013 and Ashutosh Gupta et al.,2016)**. Various power reduction techniques are also included in the design.

2.1. **Fine-Grain Pipelined Architecture**

Fig. 4 shows the architecture of pipelined Inexact Speculative Adder. Let $\partial comp$, $\partial 4b{-}adder$ and $\partial spec$ be the combinational delay of compensator, 4-bit adder, and speculator blocks in a conventional ISA architecture. The carry is speculated for each and every 4-bit adder block and the local sum is being calculated by the adder block based on it. Thus by analogize the speculated carry-in with the prior carry-out which arise from 4-bit adder, the faulty speculation can be identified.

At the same time the the correction and balancing operations are performed by the compensator block. The delays present in the critical path of ISA due to speculator of the $i$thinstant , the 4-bit adder and the compensator delays of (i+1)th instant are expressed as follows,

$$\partial\text{critical} = (\partial\text{4b-adder}) + (\partial\text{spec})+1 + (\partial\text{comp})i+1 \quad (5)$$

The detailed critical path delay due to compensator blocks and internal architectures of speculator are given below

$$\partial\text{critical}+(\partial\text{4b-adder})+(2\times\partial\text{xor}+\partial\text{and})+1+(\partial\text{xor}+\partial\text{demux}+\partial\text{mux})i+1 \quad (6)$$

where $\partial demux$, ∂mux , ∂xor and ∂and, are respectively the combinational delays of the de-multiplexer, multiplexer ,logical XOR and logical AND gates. The critical path delay can be reduced by introducing the fine grain pipelining in ISA architecture and achieving a fast VLSI-architecture.

The pipeling process is explained using the architecture shown in figure in which the traditional blocks has been restored by the pipelined 4-bit CLA(PCLA), pipelined compensator (PCOMP) and pipelined speculator (PSPEC) units.

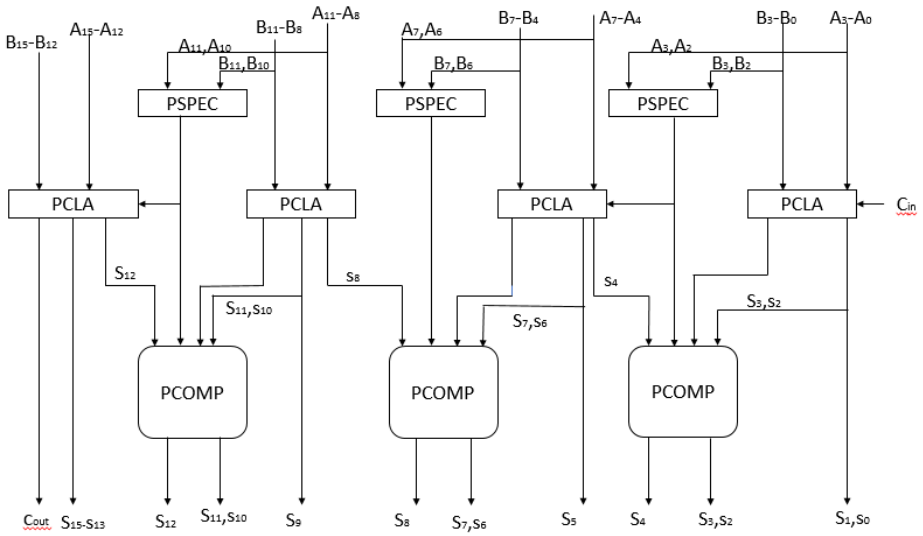

Figure.4 Architecture of pipelined Inexact Speculative Adder

Also two pipeline stages are present in the sub blocks of PSPEC, PCLA and PCOMP. This architecture consists of five stages of pipeline and six levels of levels of registers as shown in figure 5.Simiarly pipelines stages are incorporated in the designs of PSPEC, PCOMP and PCLA there by reducing the delay.

The frequency of operation of the proposed ISA is decided by the critical path delay and it is given by the expression

$$\partial\text{crt-prop} = \partial\text{clk-(ff)} + \partial\text{xor} + 3\times\partial\text{and} + \partial\text{setup(ff)} \quad (7)$$

where $\partial setup(ff)$ and $\partial clk{-}Q(ff)$ represent setup time and clock-to-Q delay of launch and capture flip flops, respectively, in the design. Thus the maximum operating clock frequency that can be obtained by this ISA architecture is given by

$$\text{Fmax} \leq 1/\{\partial\text{crt-prop} - \partial\text{skew}\} \quad (8)$$

where $\partial skew$ depict the clock skew.

2.2 Low Power Techniques

There are several VLSI techniques available to achieve low power in order to achieve a better trade-offs between power, delay and its product. Every technique contributes an efficient method to reduce leakage power without altering the architecture.The low power techniques adopted in this work are 1)SLEEP approach,2)STACK approach and 3)SLEEPY STACK approach. Figure 5,6 and 7 shows the diagram of sleep ,stack and sleepy stack approaches respectively.

In SLEEP approach**(Se Hun Kim et al., 2006 and Jun Cheol Park et al., 2006)**,in between the VDD and the pull-up network a "sleep" PMOS transistor is placed. An NMOS transistor is placed as a "sleep" transistor in between the GND and the pull-down network.These sleep transistors turns off the power to the circuit from the power rails when the circuit is idle and is turned on when it is active. Thus a reduction in leakage power is achieved effectively by cutting off the power source.

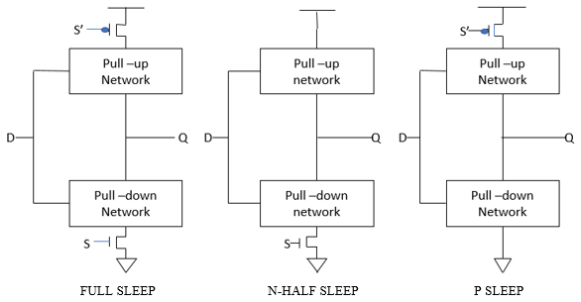

Figure.5 Sleep Approach

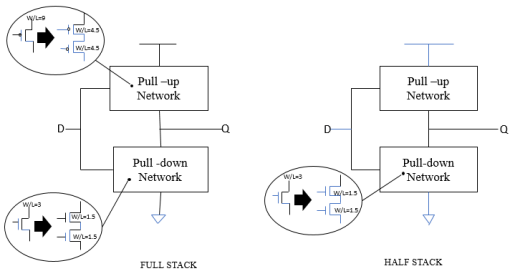

Figure.6 Stack Approach

In STACK approach , stacking of the transistor is employed for further leakage reduction.The pull up and pull down network are divided into two half size**(Ali Peiravi, et al., 2012).**This dividing of the transistor will not affect the W/L ratio of the circuit **(K. Roy et al., 2003).** The stacking of the transistor is provided by the dividing of pull up PMOS network and it provides better leakage saving. Thus this method provides better performance by suppressing sub threshold leakage current and DIBL leakage **(D.Vijayalakshmi et al.,2016).**

A combination of sleep and stack approaches are employed in SLEEPY STACK approach **(SagarDafet al., 2015)**. Like the stack approach in this technique also the existing transistors are divided in to two half size transistors.Then a sleepy transistor is added in parallel tone of the divided transistor

Thus the stacked transistors suppress the leakage current and the sleep transistors turned off the power during sleep mode. Also the delay is reduced during the active mode, since the sleep transistors are in parallel to any one of the stacked transistor..

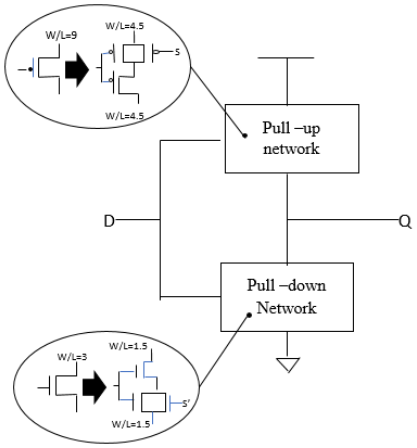

Figure.7 Sleepy Stack Approach

However the draw back of this approach is large area occupied due to presence of three transistors for a single transistor.

3. Results and Discussions

The existing and proposed architecture are simulated by using HSPICE simulator. Output of the existing inexact speculative adder and the proposed inexact speculative adder are analysed. From the results and it is concluded that the proposed architecture reduces the delay compared with the existing system. The Synthesis is done using Xilinx ISE. Figure 8 shows the simulation output of a 4-bit pipelined carry look-ahead adder. Figure 9 shows the simulation output of a 4-bit pipelined carry look-ahead adder using sleep technique. Figure 10. shows the simulation output of pipelined compensator. Figure11 shows the simulation output of a pipelined compensator using sleep technique. Figure 12 shows the simulation output of a pipelined speculator.Figure 13 shows the simulation output of a pipelined speculator using sleep technique.

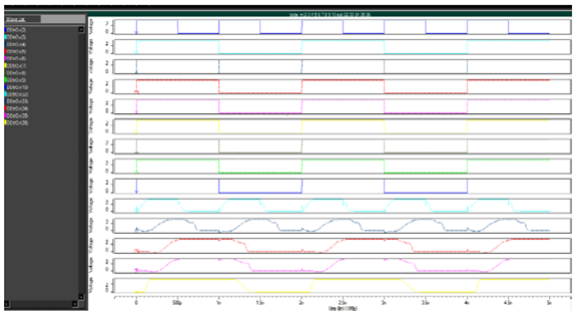

Figure.8 Output of 4-Bit Carry Look Ahead Adder

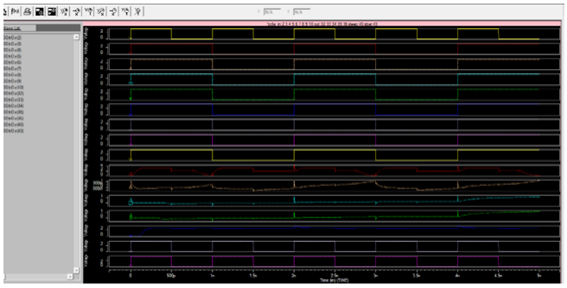

Figure.9 Simulation output of pipelined 4-Bit Carry Look Ahead Adder with sleep technique

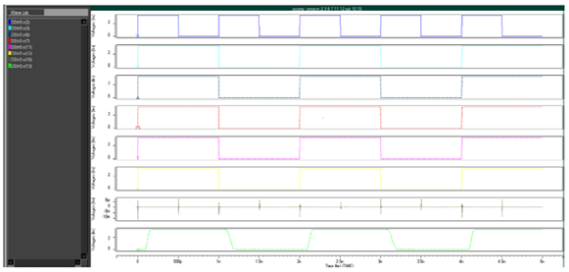

Figure.10 Simulation output of Pipelined compensator

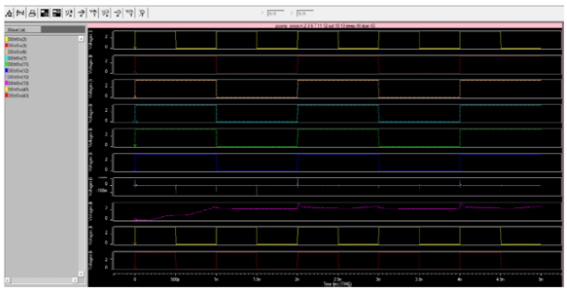

Figure.11.Simulation output of Pipelined compensator with sleep technique

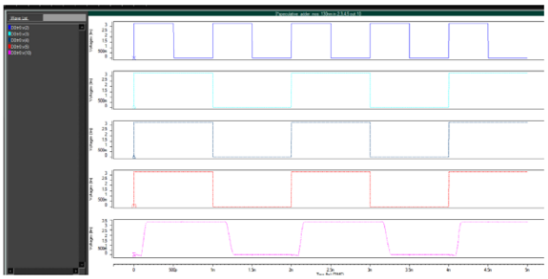

Figure.12 Pipelined speculator output

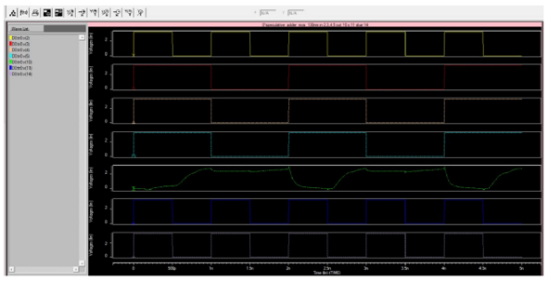

Figure.13 Output of Pipelined speculator with sleep technique

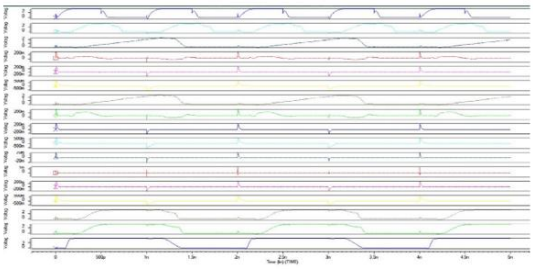

Figure.14 Output of pipelined inexact speculativeadder

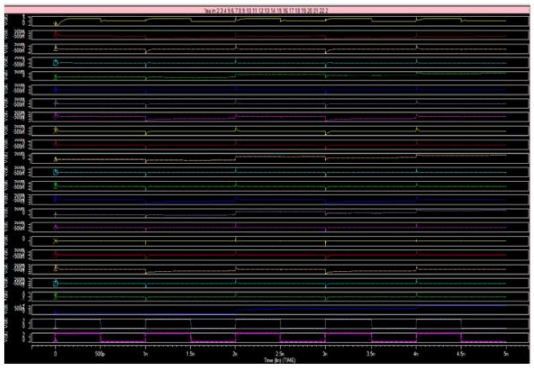

Figure.15 Output of pipelined inexact speculative adder of proposed system

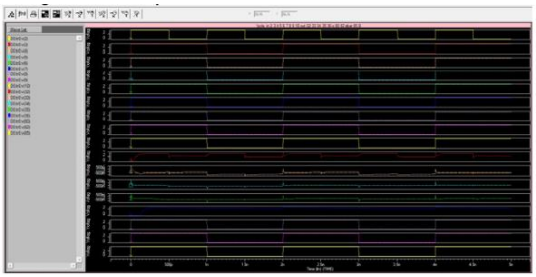

Figure.16 Output of pipelined carry look head adder with stack technique

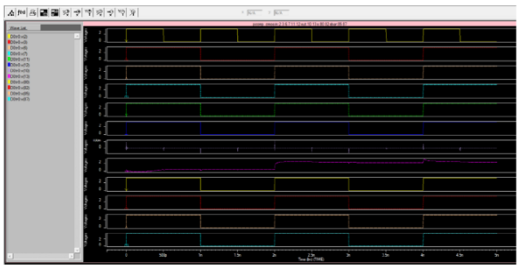

Figure.17 .Output of pipelined compensator with stack technique

Table.1. Power Delay Analysis of Existing System

Device	Average Power(mW)	Delay(ps)	Power delay Product(pJ)
Inexact Speculative Adder	0.37	41.546	2.820
4-bit PCLA	0.098	268.45	17.735
Pipelined Speculator	1.245	500.95	31.05
Pipelined compensator	3.49	1.65	0.286

Table.2. Power Delay Analysis of proposed ISA using sleep technique

Device	Average Power (mW)	Delay(ps)	Power delay Product (pJ)
Inexact Speculative Adder	0.8073	17.418	2.574
4-bit PCLA	0.7859	198.12	28.5
Pipelined Speculator	0.0669	341.39	15.388
Pipelined compensator	0.1193	.6	0.03646

Table.3. Power Delay Analysis of proposed ISA using stack technique

Device	Average Power(mW)	Delay(ps)	Power delay Product(pJ)
Inexact Speculative Adder	0.725	1.2994	0.175
4-bit PCLA	0.6871	149.46	18.80
Pipelined Speculator	0.03484	250.29	5.875
Pipelined compensator	0.08391	4.229	0.2390

Table.4. Delay Analysis of proposed ISA using sleepy stack technique

Device	Average Power (mW)	Delay(ps)	Power delay Product(pJ)
Inexact Speculative Adder	0.7548	7.659	1.0588
4-bit PCLA	0.7155	250.5	32.827
Pipelined Speculator	0.04220	498.4	0.1417
Pipelined compensator	0.09435	1.7199	10.933

Figure 14 shows the simulation output of a pipelined inexact speculative adder of existing system.Figure 15 Output of pipelined inexact speculative adder of proposed system. Figure 16 shows the simulation output of a 4-bit pipelined-carry look-ahead adder (PCLA) output using stack technique.Figure 17 shows the simulationoutput of Pipelined compensator (PCOMP) output using stack technique.Figure 20. Power delay analysis of proposed ISA with stack technique. Table 1. depicts the parameters and the values obtained for the power delay analysis of existing system. Table 2. depicts the parameters and the values obtained for the power delay analysis of proposed ISA using sleep technique.Table 3. depicts the parameters and the values obtained for the power delay analysis of proposed ISA using stack technique.

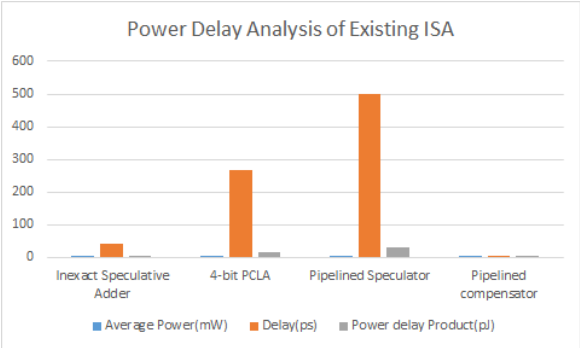

Figure.18 Power delay analysis of existing ISA

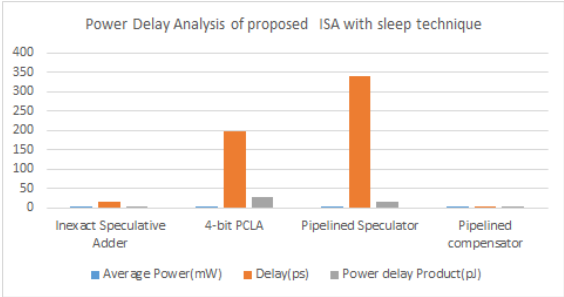

Figure.19 Power dely analysis of proposed ISA with sleep technique

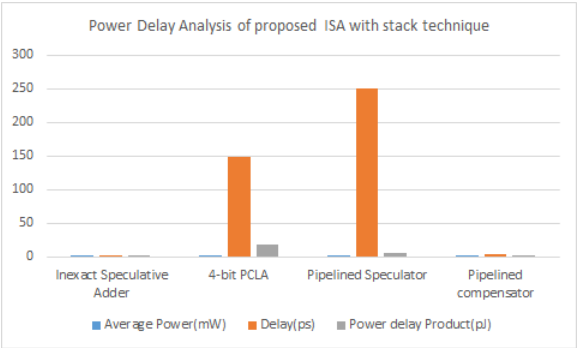

Figure.20. Power delay analysis of proposed ISA with stack technique

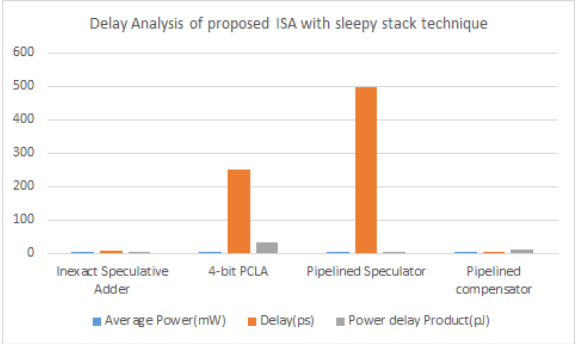

Figure.21. Power delay analysis of proposed ISA with sleepy stack technique

Table 4. depicts the parameters and the values obtained for delay analysis of proposed ISA using sleepy stack technique.It is observed that an Figure 18. Shows the power delay analysis of existing ISA. Figure 19 shows the power delay analysis of proposed ISA with sleep technique. It is observed that the delay and power delay product is reduced in the proposed system with sleep technique. Figure20 shows the power delay analysis of proposed ISA with stack technique. It is also observed that the delay and power delay product is reduced in the proposed system with stack technique Figure 21 shows the power delay analysis of proposed ISA with sleepy stack technique. A further reduction is observed in the delay andpower delay product of the proposed system with sleepy stack technique. An increase in the power is observed in all the case ,it may be due to the extra circuitry added to obtain less delay. At the same time a drastic decrease in the delay is observed in the proposed system which leads to an increase in speed.

4. Conclusion

This paper presents the high-speed model of the recent ISA design. Fine grain pipeline and clock gating is included in this architecture to improve its speed and reduce the power consumption respectively. Simulation results of the existing ISA,Speculator, CLA and Compensator are presented. Also the simulation results of the proposed system including the pipelining techniques in ISA,Speculator, CLA and Compensator are presented. The results of pipelined ISA, pipelined Speculator, pipelined CLA and pipelined Compensator with together with the power saving techniques of SLEEP,STACK and SLEEP STACK approaches are also presented. It is observed that The average power consumption is high in the proposed system due to the inclusion of additional circuitry for the reduction of delay. But the delay is considerably reduced in the proposed system with pipelining and power reduction techniques.

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