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Research Article

A New Approach in Wirelss Communication: Design and Development of a Simulator For Receiver Processor

Dr. B.Suneela[a] , E.Suresh[b] , Ali Baig Mohammad [c] , Mohana Lakshmi [d] , G.Aparna [e] Dr.M.Kezia Joseph [f]

[a] Associate professor, Lords Institute of Engineering Technology, Hyderabad, Telangana, India.
Email id suneela@lords.ac.in
[b] Associate Professor, Department of ECE,KITS WARANGAL, Hasanparty, Telangana. India
Email id esuresh_77@yahoo.com.
[c] ALI BAIG MOHAMMAD, Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Andhra Pradesh, India, pincode is 522502, Email id : mdabaig@kluniversity.in.
[d] K.Mohana Lakshmi, Associate Professor, CMR Technical Campus, andlakoya, Medchal, Hyderabad, India. Email id: - mohana.kesana@gmail.com
[e] Research Scholar, ECE Department, University College of Engineering, Osmania University, Hyderabad, Telangana, India, Email id :- aparnaece27@gmail.com.
[f]. Professor, ECE Department, Stanley College of Engineering and Technology for Women, Abids, Nampally, Telangana, Hyderabad. Email id:- keziajoseph@stanley.edu.in.

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Abstract: In this paper we designed and developed a Simulator for radar receiver and transmitted sub system using VIRTEX5 FPGA Board. In this radar Receiver processor subsystem the function of the receiver processor is to accept different data parameters like Frequency, Amplitude, Direction Finding, Pulse Width and PRI presence pulses from different receivers. There is a need to test the receiver processor in standalone mode before integrating or comparing it with the other receiver. The purpose of this simulator module is to design and develop a simulator based on VIRTEX 5 FPGA simulator board using RS232 serial communication link. The project is broadly segregated into two major activities which will be carried out in two methods. In stage I, a Graphical User Interface (GUI) is designed and developed based on LABVIEW which provides the pulses parameters of intercepted pulse along with the parameter code using a computer. Next the selected code is encoded. Subsequently followed by sending of the coded data using an RS 232 serial link to the target hardware. The target hardware is a VIRTEX 5 FPGA based simulator board.

In stage II, firstly the coded data is decoded based on received parameter code. This activity is carried out by developing a code based on 'C' language using the hardcore power PC 440 processor available in the VIRTEX 5 FPGA in an embedded design environment. Subsequently followed by design and developed of digital glue logic which finally generates all the required parameter data like Frequency, Amplitude, Direction Finding, Pulse Width and PRI presence pulses for the received parameter code. This activity is carried out by developing a code using 'Embedded C' language.Finally all the developed code in phase II is tested for its complete functionality in the simulated environment. Subsequent to which the complete code is implemented on the target hardware board and testing will be carried out for the complete functionality using VIRTEX 5 FPGA Board.

Keywords: VIRTEX 5 FPGA Board, Graphical User Interface (GUI), LABVIEW, radar receiver

1. Introduction to Project

2.1 Brief Overview:

Electronics today has an important role in a country's development process, it can be called a fundamental component in modern technology and country's technological progress is assessed on the basis of its capabilities in this area. Electronics play a catalytic role in enhancing production and productivity in key sectors of economy.

The Proposed design & develop a simulator using VIRTEX5 FPGA board for radar transmiter/ receiver processor using rs232 serial communication link is created by using Embedded 'C' programming language and implemented in this part of radar receiver subsystem. This simulator generates a pulse which is synchronized with the parameters Frequency, Amplitude, Direction Frequency, Pulse Width, Pulse Repetition Internal. It finds variety of applications in simulators and EW.

A graphical user interface (GUI) is designed and developed based on LABVIEW software which provides the selectivity of different receivers along with the parameter code using a computer. Next the selected code is encoded. Subsequently followed by sending the code data using an RS232 serial link to the target hardware. The target hardware is a Virtex 5 FPGA based simulator board.

The design of our project is broadly classified into 3 modules:

MODULE -1 (GUI – Graphical User Interface)
MODULE-2 (EMBEDDED SOFTWARE)
Module -3 (RADAR PARAMETER GENERATOR)

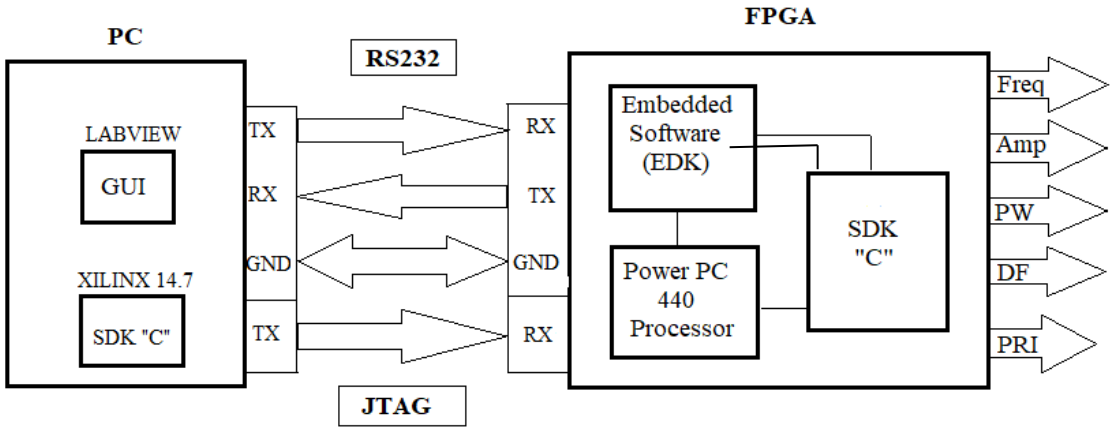


Fig 2 Block Diagram

2.2 Technical Specifications:

Inputs:

1.Input data:From GUI

2.Clock:System clock of 40MHz

3.Reset:Switch

Outputs:

1.Frequency:14-bits

2.Amplitude:8-bits

3.Direction Finding:12-bits

4. Pulse Width:16-bits

5. Pulse Repetition Interval:36-bits

Hardware Requirements:

1. Front End:GUI(using Lab view)
2. Medium:RS232 cable with both end connected
3. Back End:Xilinx 14.7
4. Synthesis:Xilinx Platform Studio(XPS)
5. Target Hardware:VIRTEX 5 (FPGA board ML507)

Software Requirements:

1.GUI:Lab view

2. Embedded Software:'C' language in EDK environment from Xilinx Software

3. Simulation Method

3.1 Introduction:

The function of the receiver processor is to accept different parameters data like frequency, direction finding, amplitude and RF presence pulses from different receivers. There is a need to test the receiver processor in standalone mode before integrating it with the other receiver. The purpose of this project is to design and develop a simulator based on Virtex 5 FPGA simulator board using RS232 serial communication link. The project is broadly segregated into two major activities which will be carried out in two phases.

In Phase I, a Graphical User Interface (GUI) is designed and developed based on visual MATLAB which provides the pulses parameters of intercepted pulse along with the parameter code using a computer. Next the selected code is encoded. Subsequently followed by sending of the coded data using an RS232 serial link to the target hardware. The target hardware is a Virtex 5 FPGA based simulator board.

In phase II, firstly the coded data is decoded based on received parameter code. This activity is carried out by developing a code based on 'C' language using the hardcore power PC 440 processor available in the Virtex 5 FPGA in an embedded design environment. Subsequently followed by design and developed of digital glue logic which finally generates all the required parameter data like frequency, direction finding, amplitude and RF presence pulses for the received parameter code. This activity is carried out by developing a code using 'C' language.

Finally all the developed code in phase II is tested for its complete functionality in the simulated environment. Subsequent to which the complete code is implemented on the target hardware board and testing will be carried out for the complete functionality.

3.2 Graphical User Interface(GUI):

Usage of GUI in the project:

Theinput is given to the GUI module. The data from this module can be accessed for further processing. The main purpose of using GUI is for selection purpose, so that a program is written using the LABVIEW to obtain the GUI window. The program is written such that the selected data interfaces with RS232 for the purpose of serial communication.

The following information gives the description about LABVIEW and the way how the GUI window is created.

3.3 Embedded Development Kit:

The serial data received using RS232 is fed as input to EDK. The coded data is decoded to identify the corresponding parameter code. This activity is carried out by developing embedded software based on 'C' language using the hardcore Power PC 440 processor available in the virtex 5 FPGA in an embedded design environment. Here the received input data contains the parity bits, start bits and stop bits, so it removes those bits and the required data is passed to the radar parameter generator environment.

3.3.1 What is EDK?

The Xilinx Embedded Development Kit (EDK) provides a suite of design tolls which are based on a common framework that enable you o design a complete embedded processor system for implementation in a Xilinx FPGA device.

EDK depends on ISE components to synthesize the microprocessor hardware design, to map that design to an FPGA target, and to generate download the bits stream.

3.3.2.1 The Base System Builder:

About Base System Builder (BSB) wizard to create the foundation for any new embedded design project. It might be all you need to create your design, but if you require more customization, the BSB saves you a lot of time because it automates basic hardware and software platform configuration tasks common to most processor designs, After running the Wizard, you have a working project that contains all the basic elements needed to build a more customized or complex system, should that be necessary.

3.3.4 PowerPC 440 Processor:

The PowerPC 440 embedded processor implements the full, 32-bit fixed-point subset of the IBM Book E: Enhanced PowerPC architecture. The PowerPC 440 embedded processor fully complies with this architectural specification. The 64-bit operations of the architecture are not supported, and the embedded processor does not implement the floating-point operations, although a floating-point unit (FPU) can be attached (using the APU interface). Within the embedded processor, the 64-bit operations and the floating-point operations are trapped, and the floating-point operations can be emulated using software.

3.3.4.1 PowerPC 440 Features:

The PowerPC 440 embedded processor contains a dual-issue, superscalar, pipelined processing unit, along with other functional elements required to implement embedded system-on-a-chip solutions. These other functions include memory management, cache control, timers, and debug facilities. In addition to three separate 128-bit Processor Local Bus (PLB) interfaces, the embedded processor provides interfaces for custom coprocessors and floating-point functions, along with separate 32 KB instruction and 32 KB data caches.

3.4 Radar Parameters Generator:

The input from the EDK environment is fed to the radar parameter generator environment. We write the program using 'C' language in ISE 14.7 environment from Xilinx software. The program is written such that radar parameters are defined related to the given data. The design and development of digital logic which finally generates all the required parameter data like frequency, direction, finding, amplitude and RF pulses for the appropriate selected parameter code.

3.4.1 Brief Description of Radar Parameters Generator Architecture:

The entire design constitutes the following four modules and their realization is explained briefly in the form of Pseudo code in the following section.

The basic four modules are

- Lookup table (LUT)
- Chirp modulation
- Pulse generation
- Delay

3.4.1.1 Lookup Table:

- The data on the 8 bit input lines of the LUT forms the address which is set using a GUI using the VB software.
- Depending on the selected address the corresponding parameters alone with a pulse is outputted from the LUT are displayed.

3.4.1.2 Chirp Modulation Generation:

The generation of Frequency modulation of the data is carried out using the following steps:

- The process begins when the address corresponding to generation of chirp is set.
- The counter is enabled to count till the value of the PRI.
- For the first period there is a modulation in frequency and appropriate frequency would be output on the bus.
- The procedure is similar for the second and third periods.
- If the address set is not corresponding to the chirp generation then a single frequency would be the output without any frequency modulation.

3.4.1.3 Pulse Generator:

The pulse generation is carried out using the following steps:

- A counter is initiated to count PRI (Pulse Repetition interval) of the pulse.
- Compare count with PW (pulse Width)
- Signal is high when the count is less than PW (Pulse Width)
- Signal is low when the count is greater than PW and less thanPRI.

3.4.1.4 Delay Module:

This module is developed using the following steps:

- A counter is initiated to count till PRI value.
- When count value reaches PRI value then the counter is initialized to '0' and subsequently all the output parameter data are made to '0'.

Output:

SYSTEM IMPLEMENTATION AND TESTING

The hardware implementation and testing is carried out in two stages

- Configuring FPGA
- Testing

a. Configuring FPGA:

The steps involved are:

- Synthesis
- Implementation
- User constraints

b. Description of Steps Involved:

Synthesis:

Synthesis involves the conversion of Embedded C code to GUI output electronics, logic synthesis is a process by which an abstract specification of desired circuit behavior, typically at register transfer level (RTL), is turned into a design implementation in terms of logic gates, typically by a computer program called a **synthesis** tool.

Implementation:

Implementation includes the following three main phases, namely

- Translate
- Map
- Place and Route

2a) Translate:

The translate phase is where we merge the inputs between $ and # and send through GUI in LABVIEW using JTAG .

2b) Map:

The map phase then decodes the information sent and divides into Frequency, Amplitude, Direction finding, Pulse width, Pulse repetition interval.

2c) Place and Route:

The place and route phaseis where we place components onto the chip, connect the components and extract the data using RS232 cable and output will be displayed in the GUI.

User Constraints:

In this step we assign to the pins and save them. This is done for pin locking.

Procedure:

The procedure for designing a simulator in receiver processor is classified into 3 modules. In the first module we create a GUI for selecting the input data. Then the selected data is transmittedthrough the RS 232 interface to the FPGA. In the second module, we decode the data what we have received from RS232 through Embedded software environment (EDK).

In the third module we write the code for displaying the radar parameters which is done in a Embedded C environment. Synthesis is followed by implementation. To implement the design all of the steps 1 have been carried out by using the set up. A green check mark indicates that the process is completed successfully. A **.bit** file is created. Then the generate programming file icon is executed.

Then for programming the FPGA the generated **.MCS** file is dumped using a JTAG connector.

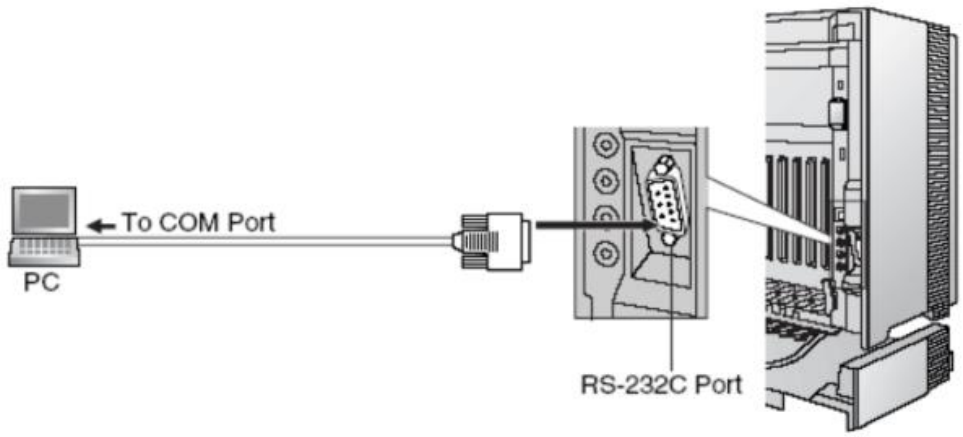


Fig 5.1 RS232 Serial Communication

C. Testing:

The evaluation board has a VERTIX 5 FPGA integrated along with its associated circuitry. With the desired file dumped onto the FPGA we can view the desired outputs. The inputs are the data that we select from GUI. The respected output parameters from the desired input selection. The parameters are frequency, amplitude, direction finding, pulse width ,pulse repetition interval.

1.1 GRAPHICAL DESIGN:

The architectural design of selected processor and memory (see figure 5.2)

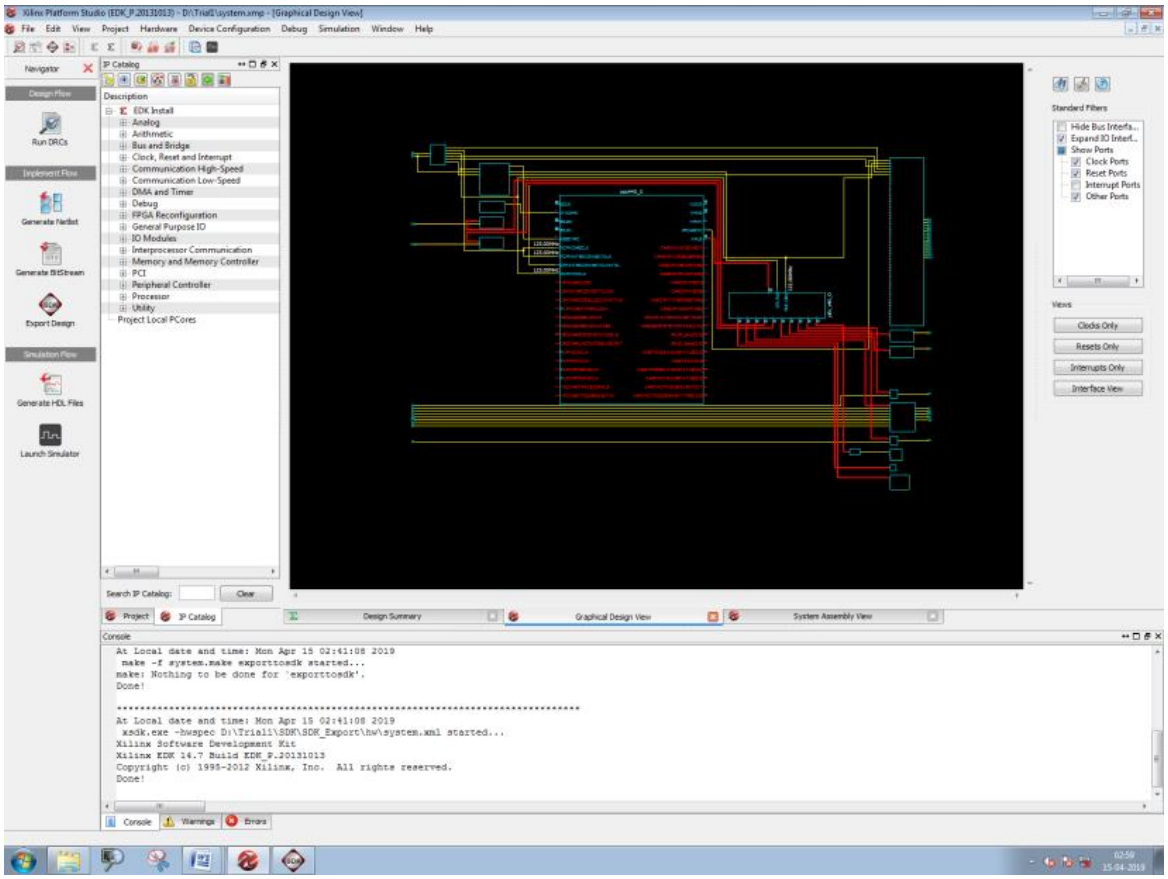


Fig 5.2 Graphical Design of Memory

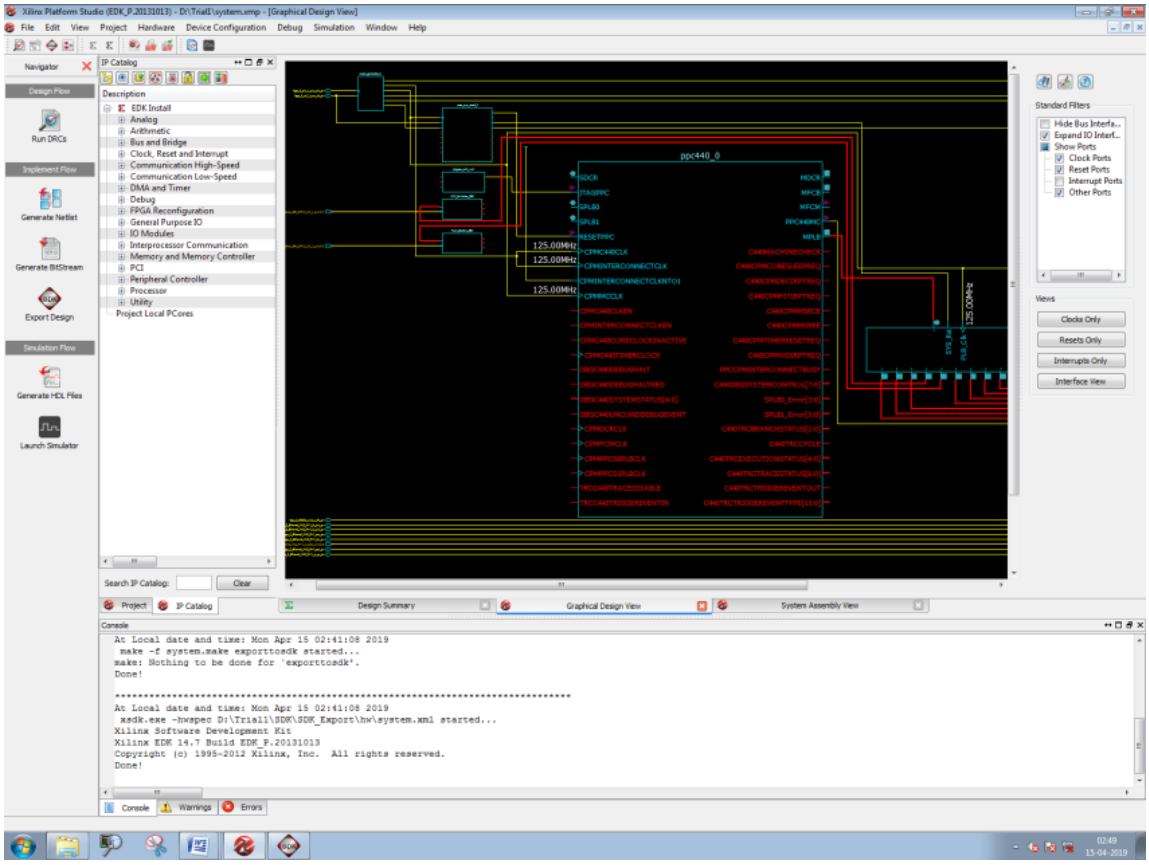


Fig 5.2 Power PC 440Design

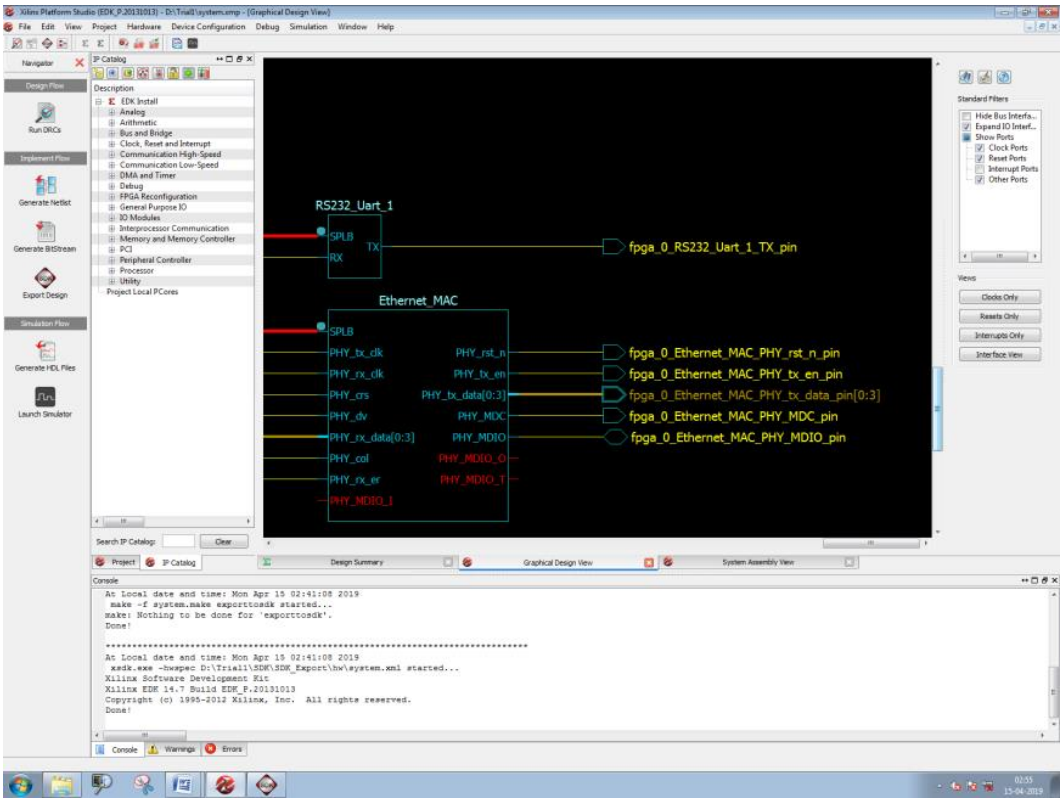


Fig 5.3 Power PC 440 Design 1

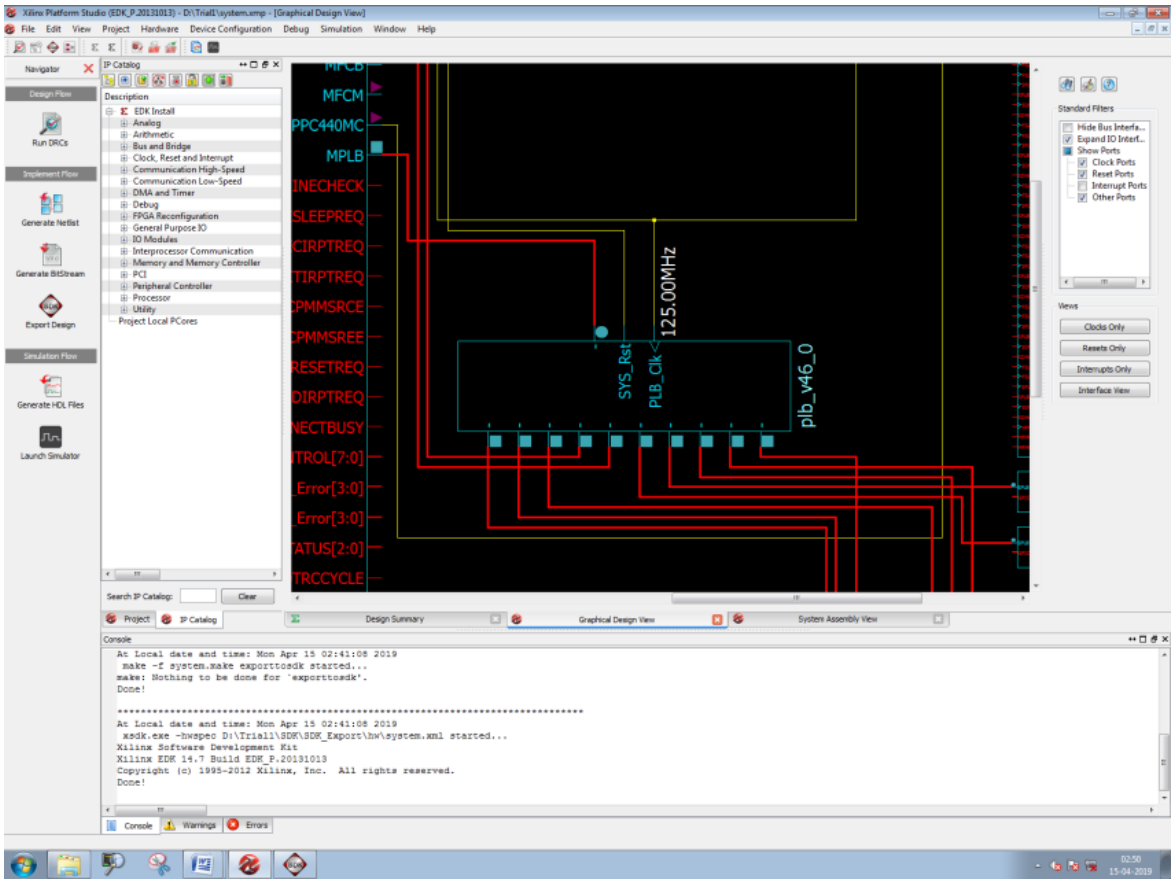
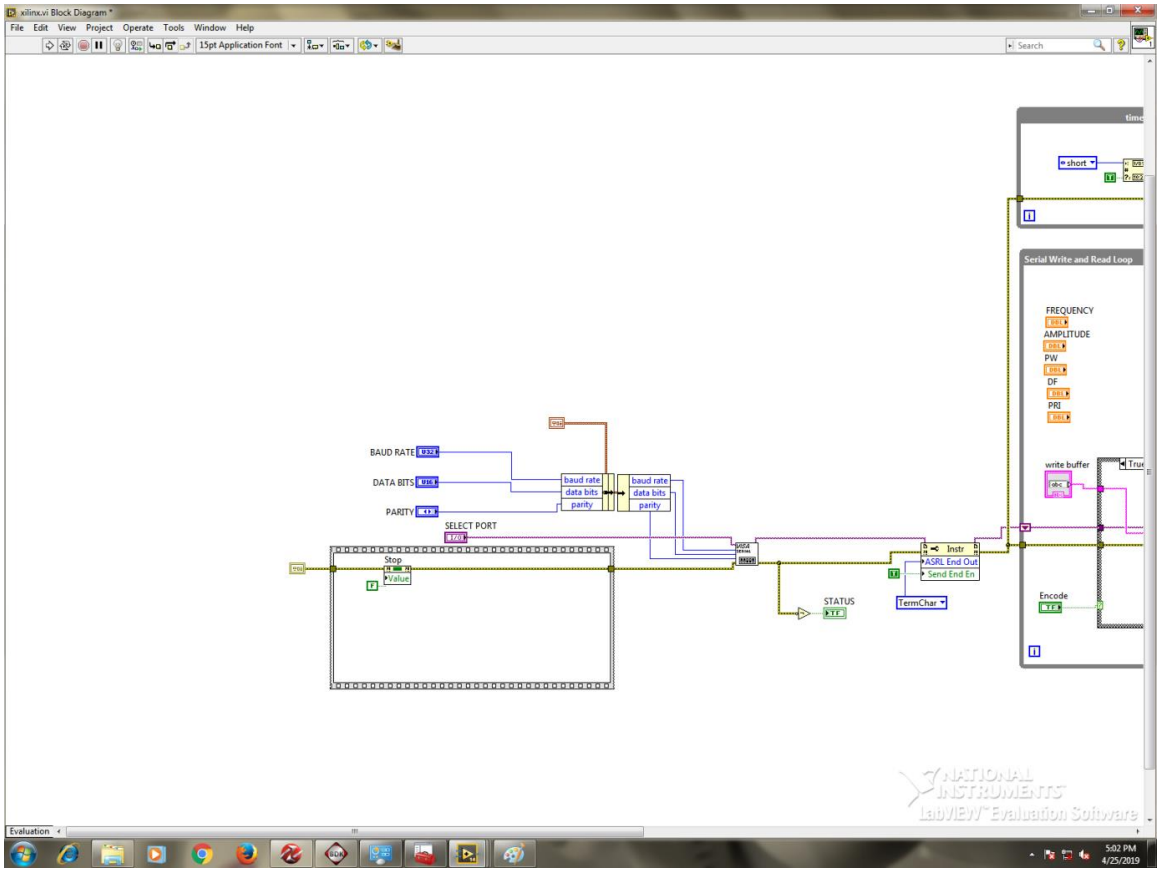
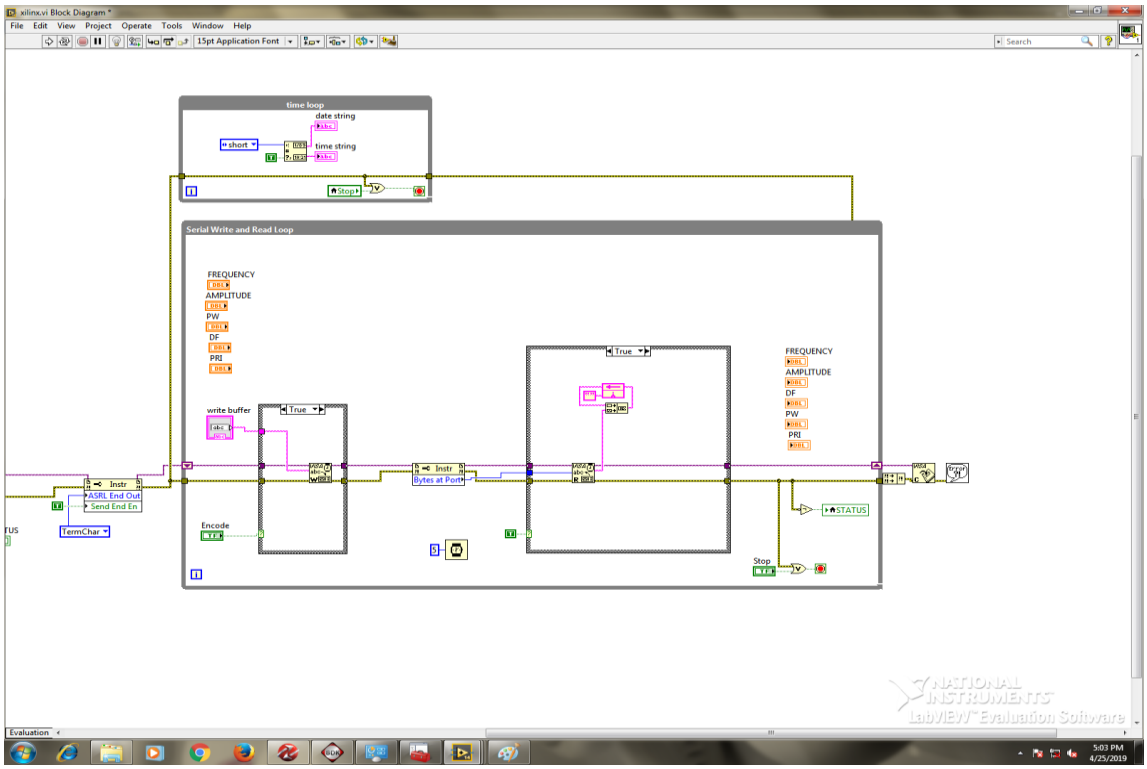


Fig 5.4 Power PC 440 Design2

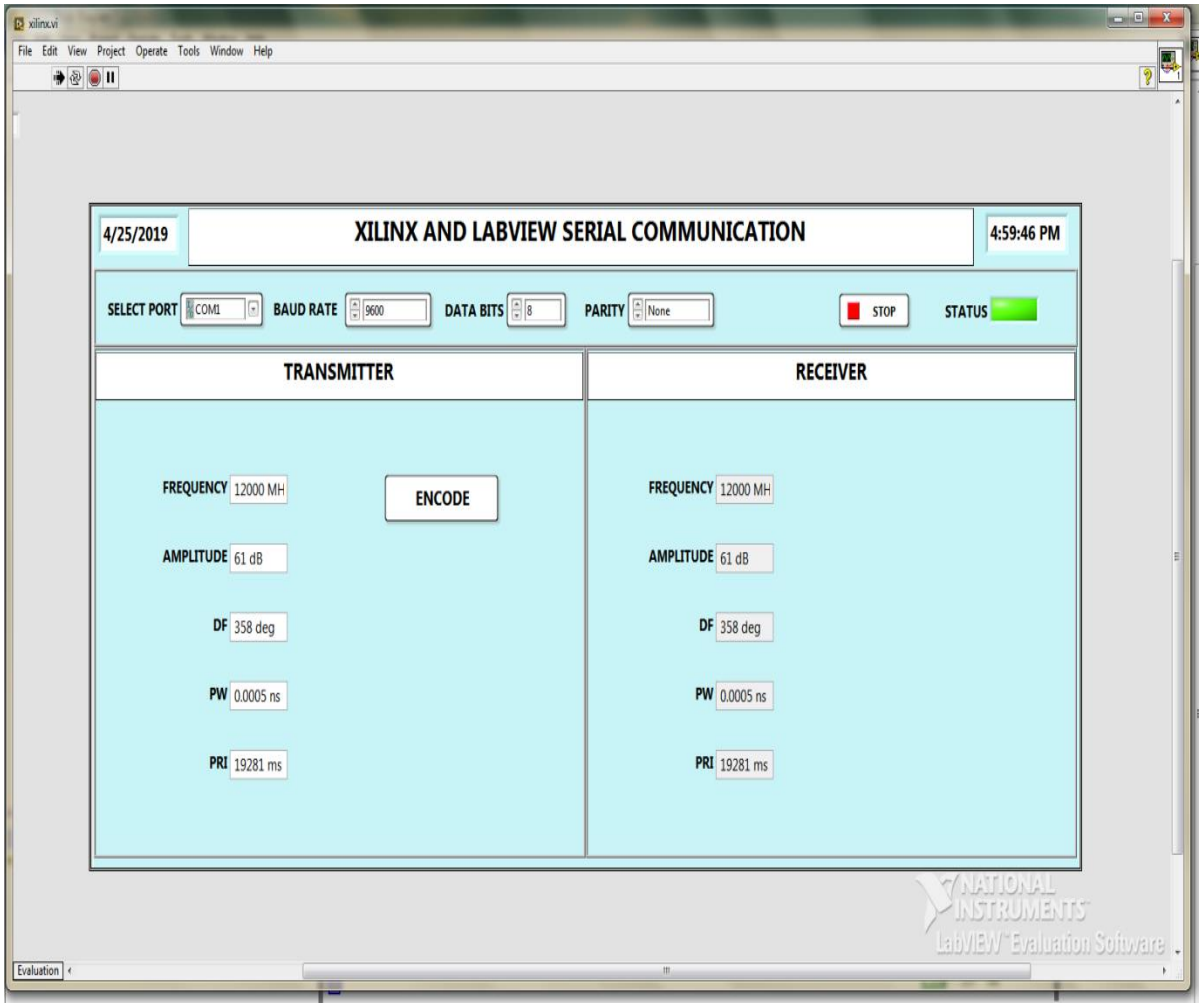
4. Simulation Results

GUI Blocks Using Labview





GUI Input And Output



5. Conclusion

In these proposed modules "DESIGN & DEVELOP A SIMULATOR USING Virtex5 FPGA BOARD FOR RADAR TRANSMITER/ RECEIVER PROCESSOR USING RS232 SERIAL COMMUNNICATION LINK" it successfully created an GUI graphical user interface using Embedded software LABVIEW ,various Radar parameter generator have also been designed and simulated. Each module is designed separately. The Radar parameters like frequency, amplitude, direction finding, pulse width, pulse repetition interval are generated. This simulation results are found to be satisfying the function of .Hardware implementation has been carried out by dumping the code on VERTEX 5 ML507 FPGA based hardware and tested for its complete functionality.

6. Future Scope

The embedded system interface unit has got capability to interface data from various on board interfaces such as RS232 link, In this project the communication interface between JTAG and simulator board is restricted to RS232 link. For the purpose of communication ASCII protocol is used, which is the basic Automatic repeat request protocol. The future scope of the work involves using Ethernet as the communication link or using "selective repeat protocol", because unlike the ASCII protocol it keeps channel busy by continuously sending enough frames through channel without waiting for the acknowledgement for the first frame. When it receives a NACK it stops sending frames, and only retransmits that particular frame and continues sending frames from where it stopped.

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