# Design Of Power Amplifier For A Unlicensed 2.4ghz Zigbee Transceiver

**Veena Hallur[1], Sudharshan K M[2], Prashant V Joshi[3]**

[1]PG Scholar, VLSI and Embedded System, School of Electronics & Communication Engineering, REVA University Bangalore, India,veenashhnd@gmail.com
[2]Associate professor, School ofElectronics & communication Engineering, REVA University, Bangalore, India, sudharshankm@reva.edu.in
[3]Associate professor, School ofElectronics & communication Engineering, REVA University, Bangalore, India, prashanthvjoshi@reva.edu.in

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**Abstract:** ZigBee has a wider range of applications. Three frequency bands of operation that ZigBee operates at are the 868-MHz, 915-MHz, and industrial unlicensed 2.4-GHz, scientific, and medical (ISM) bands. Out of three, this 2.4GHz band is an unlicensed band hence its very attractive and is commonly available throughout the world. The typical low data rate applications include those for home automation and industrial, commercial uses, consumer electronics, personal health care appliances peripherals and as well as for toys and games which are able to run for five months to two years on just batteries. Hence these areas of applications motivated to design A CMOSPA operating at 2.4GHz.In this work a single ended multistage cascode feedback linear power amplifier used and implemented it in .18um technology. Also, an efficient matching network is designed in order to get maximum efficiency, multistage for higher gain and feedback is designed to get linear output power and reliability is also more. The power amplifier operates at 2.4 GHz frequency meeting with the desired specifications.

**Keywords:**Power Amplifier (PA); Power Added Efficiency (PAE); 1dB Compression Point (CP).

## 1. Motivation

In Industry people will be reluctant to implement the PA using CMOS as the overall power consumption for a transceiver will get dominated by PA. As the portable devices are battery operated they will have limited energy stored, hence not only the integration of PA but also the PPA performance-power-area are the most important part of work .The matching network of a PA and its power dissipation is also a part of improvement.

As the CMOS technology has improved to the extent that many RF functions such as VOC, low noise amplifier, and mixers can be implemented using CMOS with high value and low cost. Hence implementing it on a single chip will reducecost by various factors such as interface matching between different chips, time to market and size. But implementing the CMOSPA and integrating is a challenge.

## 2. Introduction

The potential for including the PA in a single-chip CMOS transceiver, or in fact, in a single-chip that would serve as the entire analog and digital processing unit for a cellular phone would dramatically reduce the cost and form factor of the PA, allowing for the placing of cellular phone transceivers/processors in almost anything, including something as small as a watch.

For a service provider it costs heavily as the number of stations increases for a wider range of reception. If we can increase the power of the output signal which can transmit through a wider range without compromising the signal strength and noise, we can reduce the number of stations hence the cost for service providers will be reduced. The complexities in designing the power amplifies such as high efficiency, high currents, linearity, and power losses cause it more difficult to implement.

## 3. Literature survey

**TABLE 1. Different CMOS PA Results Comparison from Recent Papers**

| Reference | Technology | Frequency (MHz) | $V_{bat}$ (V) | Size ($mm^2$) | Gain (dB) | $P_{out}$ (dBm) | PAE (%) | Applications |
|---|---|---|---|---|---|---|---|---|

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| [2] | CMOS 90nm | 2400 | 4.3 | 4.32 | 28 | 30.1 | 33 | WiMAX |
| [3] | CMOS 0.18μm | 2400 | 4.3 | 2 | 37 | 31 | 33 | WLAN/ WiMAX |
| [4] | CMOS 65nm | 2450 | 4.3 | 2.7 | 32 | 31.5 | 25 | WLAN |
| [5] | CMOS 0.18μm | 2500 | 4.3 | 1.98 | 31.3 | 31 | 34.8 | WLAN/ WiMAX |
| [6] | CMOS 0.18μm | 2500 | 4.3 | 2.4 | 22 | 30.8 | 30.6 | WLAN/ WiMAX |
| [7] | CMOS 0.18μm | 2400 | 4.3 | 0.88 | 25 | 24.1 | 42 | WLAN |
| [8] | CMOS 0.18μm | 1850 | 4.5 | 0.4 & 1.69 | 15.8 | 30.5 26.8* | 57 44.3* | WCDMA |
| [9] | CMOS 0.18μm | 1950 | 4.5 | 2.75 & 1.69 | 24.5~ 32.2 | 30.8 29.1* | 44.1 41.1* | WCDMA |

Different CMOSPA and WCDMA PAs performance has been compared and is shown in Table 1 from [10].

## 4. Why class-e for zigbee

For ZigBee transmitters the battery is not rechargeable so to use the battery for longer duration the power dissipation inside the transmitter should be very low. To make the input power utilization maximum, we need to increase the PA efficiency.

In the Class-E power amplifier the driver stage is biased in the triode region, hence the power dissipation in the power amplifier is less. Also, it provides very high efficiency. Finally, at the operating frequency the matching circuit used in the Class-E PA acts as a short circuit, so the matching network does not dissipate any power. Hence, the above two requirements can be faithfully achieved by using a Class-E power amplifier.

## 5. Main problems in class-e power amplifier

The drawbacks of Class-E PA which needs to be improved and the techniques to improve them is listed in Table 2.

**TABLE 2: Main Drawbacks of Class-E PA**

| **Problem** | **Technique to solve problem** |
|---|---|
| Limits the linear Voltage range of circuit | Cascode Stage |
| Reliability | Thick Gate-oxide and ac ground. |
| Low Trans-conductance | MultistageCascode PA |
| Non-Linearity | Negative Feedback Network |

### 1) Cascode Technique

In Class-E amplifiers the big difference we see between the drain and the gate will cause the breakdown of the gate oxide .Over a period of time because of this breakdown in the daily usage it will affect the reliability of the circuit. By reducing the voltage at the transistor drain will improve circuit reliability. Because of the linear relationship between the $V_p$ and $V_{DD}$ results in the dropdown of the $P_{out}$ which can be improved by cascodeArchitecture.

The cascode structure allows the top transistor to have its gate oxide stress reduced by providing it a constant gate biasing [1]. Additionally, this method reduces the drain-source voltage of both transistors. On the other hand, with a single transistor, the swing from will cause tremendous stress on the gate oxide.

The ideal cascode class-E PA operation is very similar to the non-cascode version. As shown in Fig.1,$S_1$and $S_2$ are considered to be ideal switches and$C_p$ is considered to be the parasitic capacitances from $S_1$ lumped up into a general capacitor for the sake of simplicity. The remainder of the circuit is the exact same as from the non-cascode class-E PA.

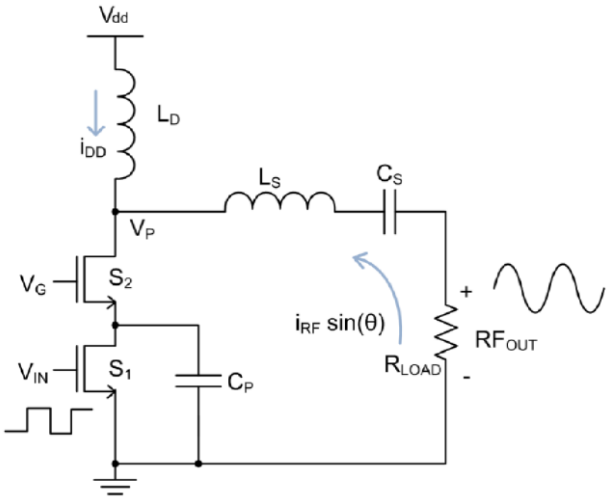


**Fig.1.Ideal cascode class-e PA circuit.**

**2) Thick Gate-Oxide**

One of the major drawbacks of a cascode stage is the high voltage stress arising between the gate and the drain. Because of the large capacitance of CG devices, the capacitance will be short for high frequency signals. Here the thick gate-oxide technique is reducing voltage stress.

The capacitance between gate and drain is inverse proportional to the thickness of gate oxide. So, if the gate-oxide thickness is going to increase then the capacitance will decrease as shown in equation 2.

$C_{dg} \propto C_{ox}WL \quad (1) where, \quad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (2) \qquad g_m \propto \frac{\varepsilon_{ox}}{t_{ox}} \quad (3)$

But at the same time trans-conductance $(g_m)$ is going to decrease as in equation 3 because it is also inverse proportional to the thickness of gate-oxide. So, the gain of the amplifier will decrease. This is the problem of thick gate-oxide.

**3) Multistage**

Multistage technique is used to increase the gain of the overall circuit. As shown in the Fig.2, the overall gain is the product of individual stage gains. Hence from the equation 4 the overall gain will increase.

$A_{open} = A_{DR} \cdot A_{PW} \cdot |\alpha_3| \quad (4)$

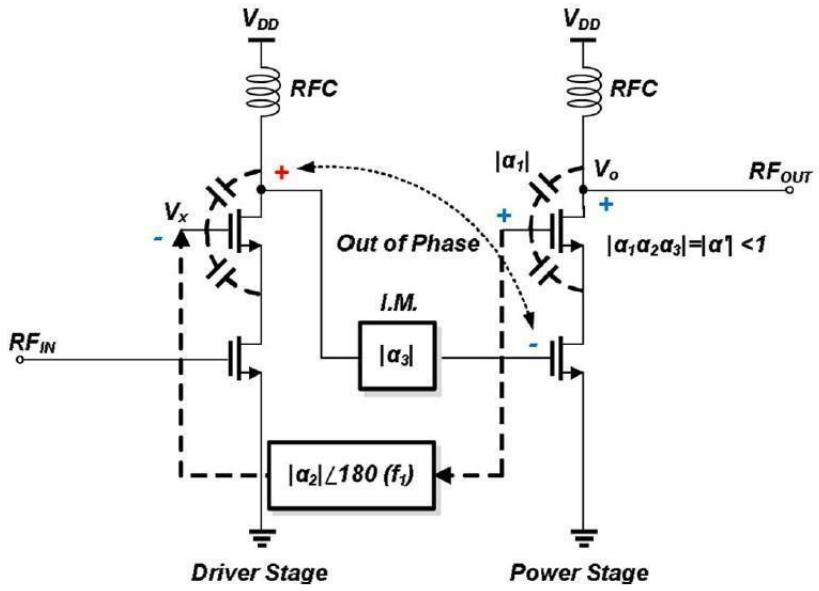


**Fig. 2. Multistage cascode amplifier**

**4) Negative Feedback**

Most widely used method to remove the nonlinearity in the analog world is the negative feedback, it reduces the noise as the output is feedback and reduces it by a factor of it.

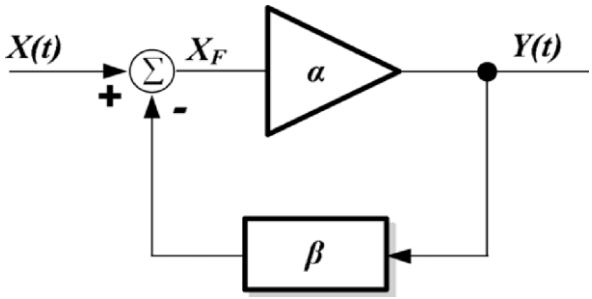


**Fig. 3. Negative feedback system.**

By using this technique, we can reduce the harmonic element shows by following equations. The negative feedback circuit is as shown in Fig. 3, Assume input signal,

$$X(t) = V_m \cos(\omega t) \quad (5)$$

Then the output signal before feedback

$$Y(t) = a\cos(\omega t) + b\cos(2\omega t) + c\cos(3\omega t) \quad (6)$$

$a, b$ *and* $c$ *are harmonic coefficient*

After feedback

$$X_F = (V_m - \beta a)\cos(\omega t) - \beta b\cos(2\omega t) - \beta c\cos(3\omega t) \quad (7)$$

Output signal after feedback

$$Y_F = \alpha_1(X_F) + \alpha_2(X_F)^2 + \alpha_3(X_F)^3 + \cdots \quad (8)$$

Consider 1st harmonic

$$Y_{F,1} \approx \cos\omega t\,(\alpha_1(V_m - \beta a)) \quad (9)$$

Comparing 1st harmonics of both before and after feedback

$$a = \frac{\alpha_1}{(1+\alpha_1\beta)}V_m \quad (10)$$

So here the 1st harmonic of after feedback is reduced by $(1 + \alpha_1\beta)$ factor compare before feedback.

## 6. Implementation

The topology of the PA with feedback bias based multistage cascodeamplifier [10] is shown in Fig. 4. In this topology the driver and power stages are used to improve the gain of the overall circuit. The cascade stage improves the efficiency. Overall, this novel method improves the reliability and linearity of PAs. Because of thelarge parasitic capacitance and low substrate resistivity of CMOS technology made thesignal swing coupling

between the transistor ports.

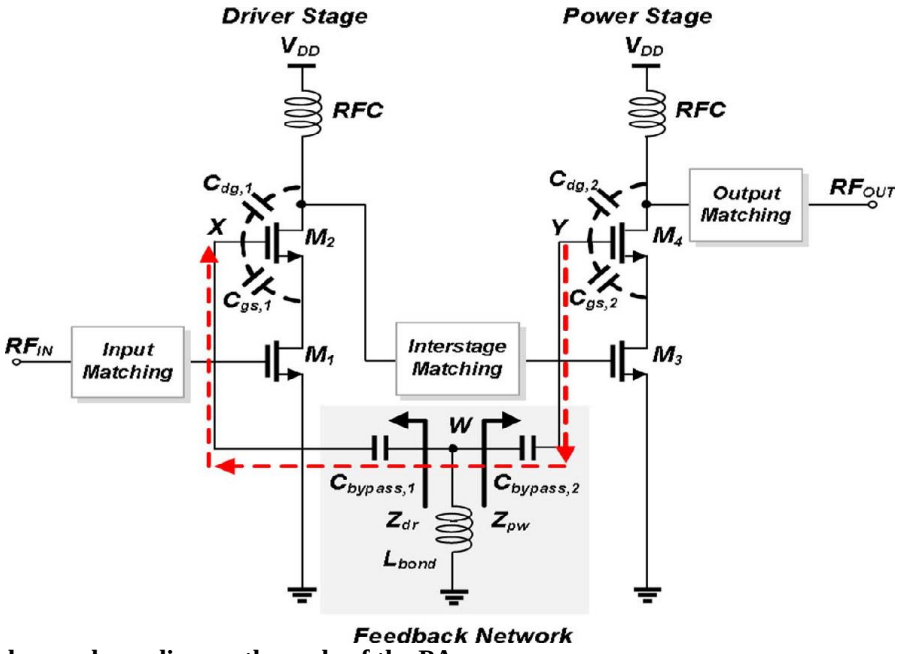


**Fig. 4. Impedances depending on the node of the PA.**

## 7. Proposed design

The proposed circuit shown in Fig. 5, is in the same way as the reference designed for 1.95GHz [10] was designed in UMC 0.18-µm CMOS but this is changed for the 2.4 GHz frequency in ZigBee applications. 2.4-GHz with the fully integrated linear PA is designed for a 3.4V power supply that transmits a linear 21.109dbm output power with a power added efficiency of 40.82% and the gain of this power amplifier is 26.53 dB in a 180nm CMOS technology.

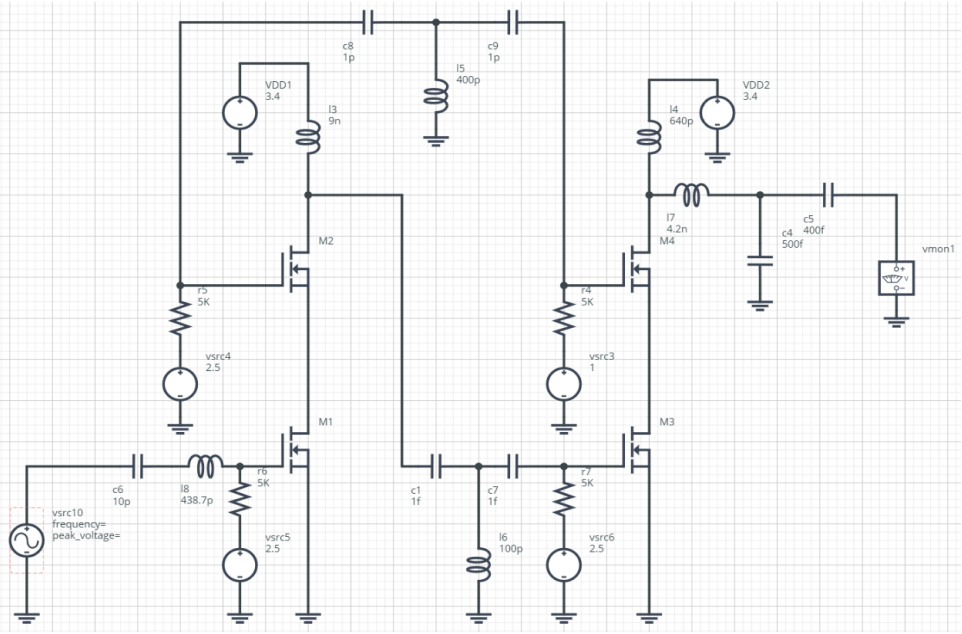


**Fig. 5. Circuit of proposed design**

For this proposed design we are choosing the input, inter stage and output matching tank circuit and resonance frequency is 2.4 GHz. And values of the input matching network are 10 pF capacitance and 438.7 pH. The inter stage matching network consists of two 1 fF capacitances and one 100 pH inductance are connected as a T circuit. And the output matching is also designed for 2.4 GHz frequency which consist of one 400 fF, one 500 fF Capacitances and one 4.2 nH inductance are connected as a T network.

The$M_2$ and $M_1$transistor widths are 1.5mm and 2.4mm in the driver stage, and $M_4$ and $M_3$ transistor widths are 5.6mm and 4.7 mm in the power stage, respectively. Load inductance of the driver stage is 9 nH and power stage is 0.64 nH. And all biasing resistance values of the transistor are 5 KOhm.

**Layout design**

8.

The post-layout of the Multistage Cascode Feedback Bias Based Linear Power Amplifier proposed design is shown in below Fig. 6. The following layout rules improve the metrics of design.

- The gate resistance is reducing by putting parallel metal upon the finger gate.
- Double ended gate structure is used to reduce RF noise.
- Grounded substrate surrounds the core devices and varies as a part of the RF device.
- The overlap capacitance between gate and source is reduced by symmetrical source/drain structure.
- Symmetrical source and drain structure are used for the modeling purpose.

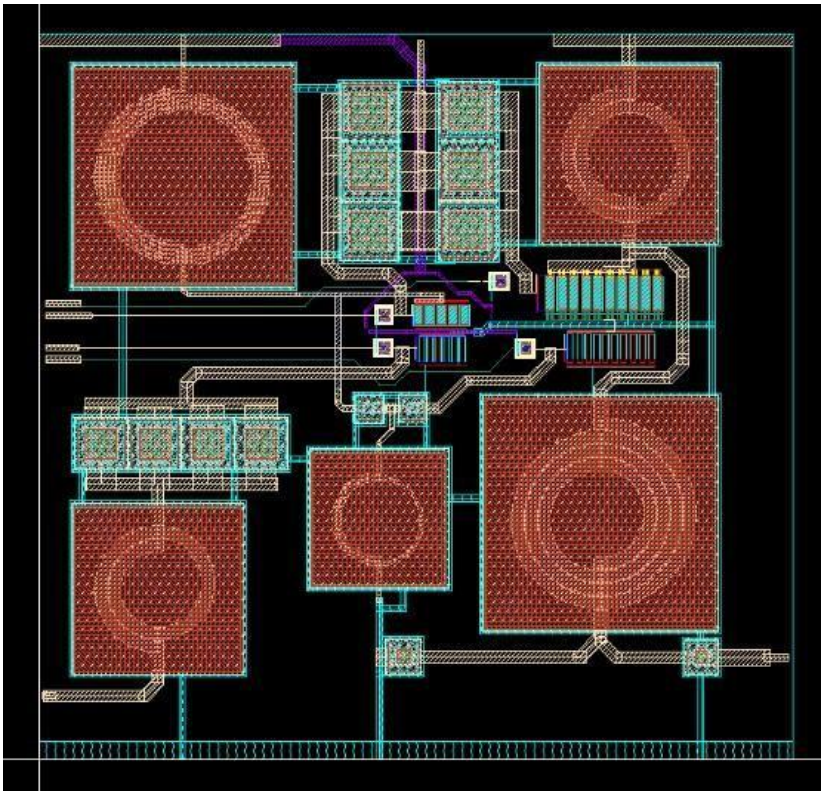

**Fig. 6. Layout circuit of proposed design**

## 9. Results

### 1. Simulation Results for Proposed Schematic Design

#### a. Output Power vs. Input Power

The output power against input power can be plotted using sweep pss analysis. In this analysis the input power is kept as variable and it is varied from -40 dBm to 10 dBm. While plotting output power against input power the input frequency of the input port is kept at 2.4 GHz. After doing the analysis the output power against input power is plotted as shown in Fig.7(a). The simulated output power at 2.4 GHz was 21.007 dBm.

#### b. Power Added Efficiency

The power added efficiency can be plotted using sweep PSS analysis. In this analysis frequency of the input port is kept at 2.4 GHz. Whereas input power is varied from -10 dBm to 10 dBm. After doing the analysis the power added efficiency is plotted as shown in Fig.7(b). The simulated power added efficiency at 0 dBm input power was 48.91 %.

#### c. Power Gain vs. Frequency

The power gain against frequency can be plotted using sweep pss analysis. In this analysis the frequency of the input port is kept as variable and it is varied from 0 GHz to 3-GHz. While plotting output power against frequency the input power is kept at 0 dBm. After doing the analysis the output power against frequency is

plotted as shown in the Fig.7(c). The simulated output power at 2.4 GHz frequency was 28.41 dB.

**d. Input referred 1 dB compression point**

None of the amplifiers is linear over its entire amplification range. So,in order to avoid working of an amplifier in a non-linear region we should use the region where its gain is linear. The input referred 1 dB compression point gives the maximum range of the input power over which amplifier is linear. 1 dB compression point is the point at which the gain is reduced by 1 dB as compared to the gain in the linear region.

The input referred 1 dB compression point can be plotted using sweep pss analysis. In this analysis frequency of the input port is kept at 2.45GHz. Whereas input power is varied from -40 dBm to 10 dBm. After doing the analysis the input referred 1 dB compression point graph can be plotted using the function compression point from Results as shown in the Fig.7(d). The simulated input referred 1 dB compression point was 4.72 dBm.

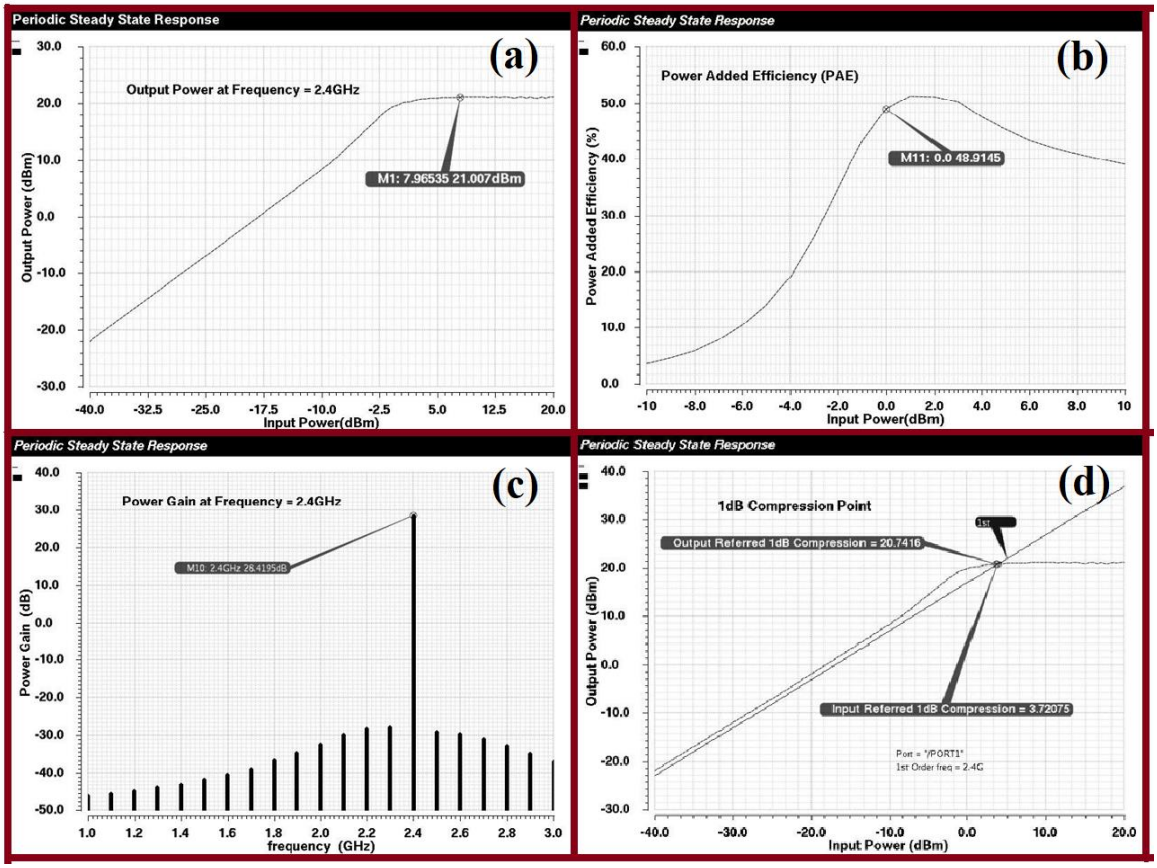


**Fig. 7.Results of schematic design**

**2. Simulation Results for Layout Design**

**a. Output Power vs. Input Power**

The simulated output power at 2.4 GHz was 21.007 dBm as shown in Fig. 8(a).

**b. Power Added Efficiency**

The simulated power added efficiency at 0 dBm input power was 47.84 % as shown in Fig. 8(b).

**c. Power Gain vs. input power**

The simulated output power at 2.4 GHz frequency was 28.40 dB as shown in Fig. 8(c).

**d. Input referred 1 dB compression point**

The simulated input referred 1 dB compression point was 4.71 dBm as shown in Fig. 8(d).

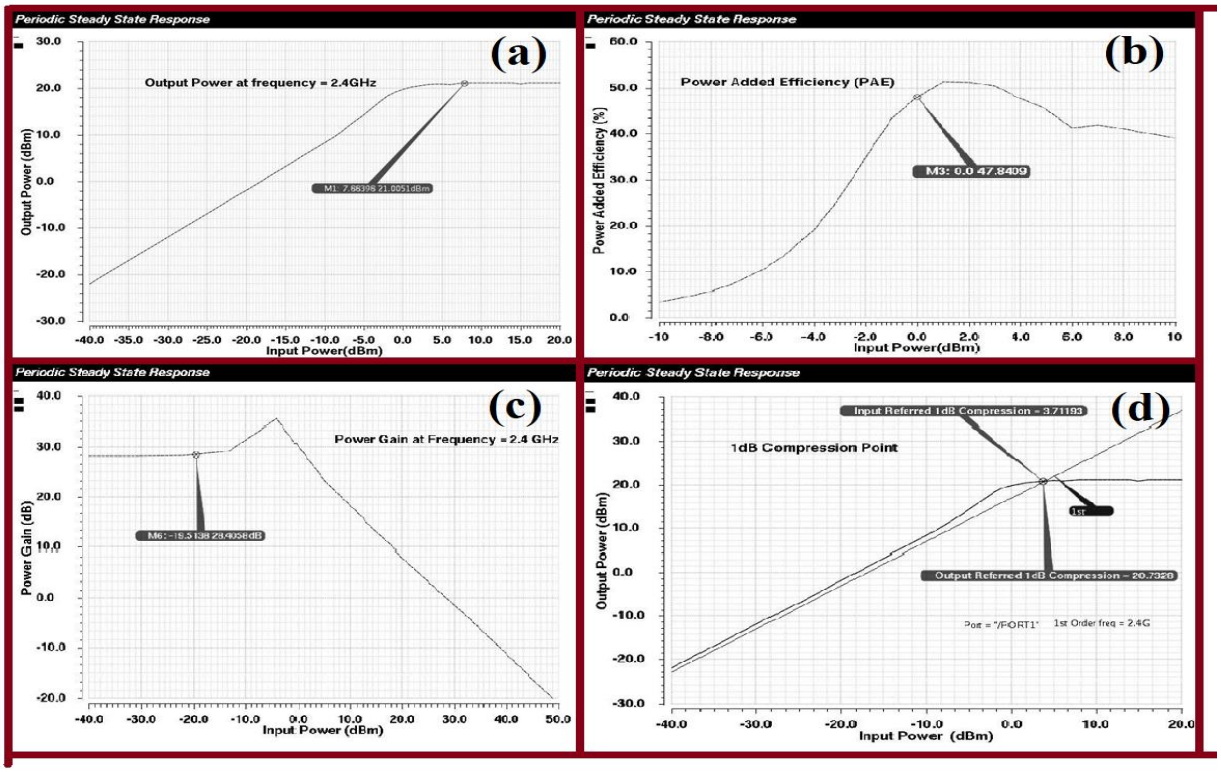


**Fig. 8. Results of layout design**

## 10. Comparison results

**TABLE 3: Results Comparison**

| Parameter | | Circuit Design [10] | Proposed Schematic Design | Proposed Layout Design |
|---|---|---|---|---|
| **Frequency** | | 1.95GHz | 2.4GHz | 2.4GHz |
| **Output Power** | | 23.5dBm | 21dBm | 21dBm |
| **PAE** | | 40% | 48.91% | 47.84% |
| **Power gain** | | 26 dB | 28.41 dB | 28.40 dB |
| **1dB Compression Point** | **Input Referred** | 2 dBm | 3.72 dBm | 3.71 dBm |
| | **Output Referred** | 21.5 dBm | 20.74 dBm | 20.73 dBm |

The performance parameters of reference circuit [10], proposed Schematic and layout are compared in Table 3.

## 11. Conclusion

In this work explored different types of power amplifier topology. With the relative study of all types of power amplifier selected a Multistage Cascode Feedback Bias Based Linear Power Amplifier to obtain high output power with high power added efficiency and also for more linearity and reliability. By using a passive gain boosting technique a new design is proposed. The design is implemented in .18 um UMC technology. The design is simulated to obtain desired results.

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