Design and Verification for I2C interface protocol Using System Verilog

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Abstract: Today's world has reached a goal in which complete module can be instigated on a one chip called SOC (system on chip).Protocols are required to combine these components. One such simple and emerging development protocol is the I2C protocol. I2C uses only two initial fundamentals bidirectional buses of pull up resistors configuration i.e Serial Clock Line (SCA) and Serial Data line (SDL). This protocol provides an efficient & simple method of data transaction among the devices & also support multiple masters, bi-directional serial bus used for quicker to connect with each other devices and no loss of data. System Verilog and its verification is used for designing the real time I2C controller with help of mentor graphics tool by creating test bench environment. Code coverage and functional coverages are the two verification coverage matrices in this environment. DUT achieved 93.3 percentage of code coverage and 100 percentage functional coverage achieved for the data and address parameters. The Benefit of this protocol is ; by using Ultra-Fast mode technique data transfer rate can be improved and its low wiring. In this paper explain about the design of an I2C protocol between a slave and master and its verification by using system Verilog language.

Keywords: Coverage,I2C,System Verilog, SDA, SCL, Verification **.**

1. Introduction

The I2C communication protocol is designed in the 1980s by Philips Semiconductor (now NXP Semiconductor). It is a popular serial communication protocol to interchange data specially between slow and fast devices. The Inter-Integrated Circuit (I2C) helps for communication with different devices. Other benefit such as reusability of modules, software based addressing, on-chip bus interface, data transfer and synchronization to ensure no data loss. More number of pin connection are not required for transmission of information due to decrease in size of I2C.

I2C bus can transfer large amounts of data by using high speed modes (3.3 Mbps). I2C having flexible specification and multi-master bus. I2C consists of only two wires Serial Data Line and Serial clock line and its ability to transmit data without loss makes it simpler and inexpensive than other protocols. I2C bus can be used in advanced Telecom computing Architecture, Power Management bus etc. It will be difficult to design and verifying the functionality of protocol. Hence, for designing hardware verification languages are used. In verification environment there is a different Verification components are required for simulating, accumulating code coverage and testing. More time and more resources are needed for verification compared to design. Coverage had a new features of System Verilog and also support randomization process for checking each random value of the design. In verification environment verify all the functionality and line by line code execution. All these features are covered to verify our environment in this paper.

2. Literature survey

[1] In this paper, I2C protocol designed using Verilog and simulation done successfully. With help of OOPS concepts and System Verilog created test bench Verification environment and having its verification components like generator, monitor, interface, driver and scoreboard were executed. The functionality of the design is verified in the environment. The proposed verification environment includes code coverage. So In this verification, there will be no loss of data.

[2]In this paper, The design was synthesized using Mentor Graphics tool by creating environment. I2C master (verification environment) initiates the transmission of data and the slave nothing butdesign responds. It can be used to interface devices at low speed as motherboard, embedded system, mobile phones, telecom networks other electronic devices or PDAs. In their work, designed an I2C master controller using HDL Verilog.

3. Problem definition

The primary intent of setting up for the design of I2C communication protocol and implement and self-checking using verification environment. This method is efficient and re-useable methodology.The acquired information is analysed and is presented using simulation.

4. Proposed methodology

In this modern verification, Test bench was one of the improved and capable enough to test bulk complex module design of the DUT to verify its features. The proposed method is to practice system Verilog which gives coverage focused verification. The fundamental method of verification is the simulation and verification strategy will decided by which test case has to be tested. The correct implementation and Verification plan is key for successful project. The main intension of this project is to validate the device is functioning the task exactly as mentioned in the specification. The verification environment is to be created depends on design specification. Functional coverage, code coverage results can be achieved successfully.

Hierarchy of developed environment

The Verification components for I2C Master is as shown in Figure 1.

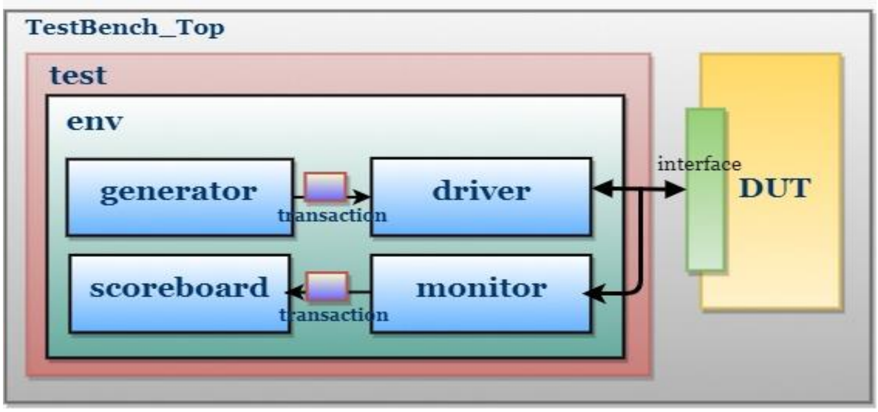


Figure 1. I2C verification environment

To verify the accuracy of the DUT use Test bench function, monitor the operations and verify the expected data displayed.

For this test bench verification environment components:

i. Generator.
ii. Driver.
iii. Interface.
iv. Monitor.
v. Scoreboard.
vi. DUT

I. Generator:

Generator is the verification component in the environment where it create the scenario's based on the input variables/random stimulus. Mail box are the temporary data storage whenever driver gets ready at that point of situation transaction send the input variables to driver in packet level.

II. Driver:

Driver first converts data from packet level to Pin level input variables. The driver leads these signals through interface to configureand reset DUT. Driver transfer these input signals to the monitor followed by transaction mail box and scoreboard.

III. Monitor:

Monitor analysing the data which is received and transmitted from DUT through the interface. Monitor will keep track of SCL (Serial Clock Line) and SDA(Serial Data Line) and also displays various information as per the functions being performed like whether it is read or write operation and coverages . Similarly it also displays start, stop and transfer of data operations. Monitor converts pin level into packet level data which is required for scoreboard operation.

IV. Scoreboard

The scoreboard collects the data from monitor mail box and generator mail box and compare the results of these two transactions and check to verify if the collected information matches with the expectation or not. Scoreboard can keep proper track of all the communications by verifying function of the DUT.

V. DUT (Design under Test):

DUT is the design of the protocol specification and used to verify its features and functions of the I2C protocol in the environment by using system Verilog language.

5. Results

Simulation waveforms are generated and verification will be done for both the READ and WRITE operation cycles as shown in figure 2.

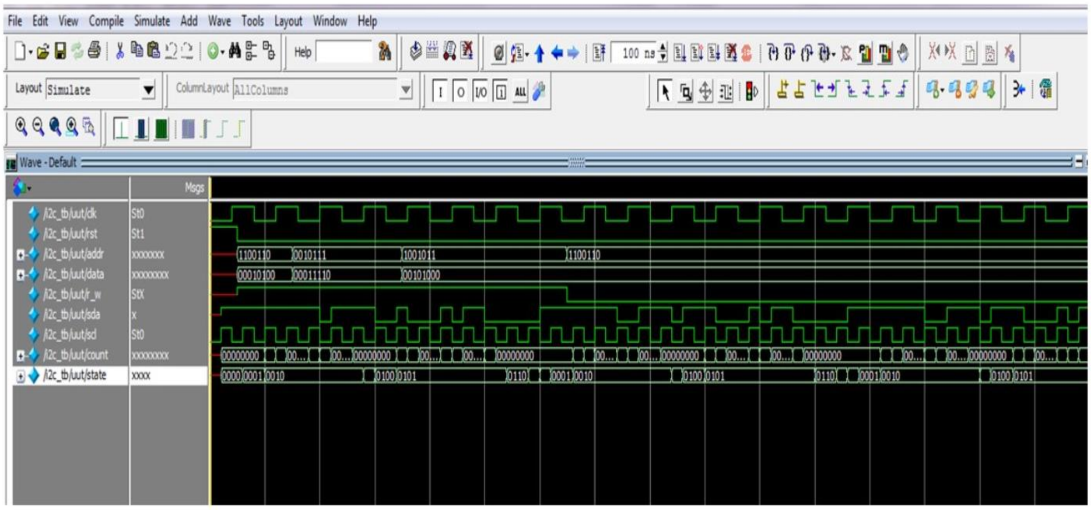


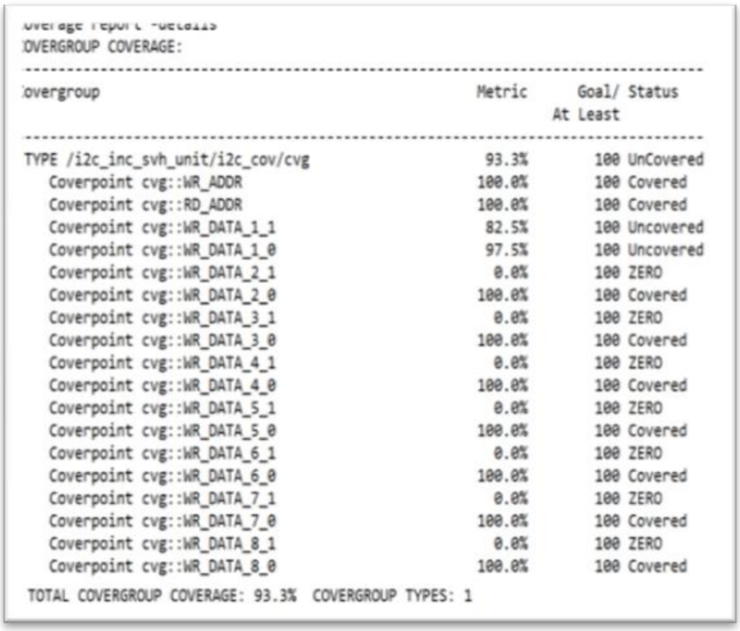
Fig. 2. Simulation results for I2C Master

DUT can be checked all the expected functional requirements by employed to make sure that functional coverage and code coverage realized line by line coverage respectively.

Results:

Code coverage and functional coverage are the two various coverage metrics in which it is covered the complex scenarios with multiple cover groups for the verification of the DUT .

DUT has achieved code coverage 93.3 percentages and as shown in figure 3.



```
overage report -details
OVERGROUP COVERAGE:
------------------------------------------------------------------------------
overgroup                                          Metric      Goal/ Status
                                                            At Least
------------------------------------------------------------------------------
TYPE /i2c_inc_svh_unit/i2c_cov/cvg                  93.3%        100 UnCovered
   Coverpoint cvg::WR_ADDR                         100.0%        100 Covered
   Coverpoint cvg::RD_ADDR                         100.0%        100 Covered
   Coverpoint cvg::WR_DATA_1_1                      82.5%        100 Uncovered
   Coverpoint cvg::WR_DATA_1_0                      97.5%        100 Uncovered
   Coverpoint cvg::WR_DATA_2_1                       0.0%        100 ZERO
   Coverpoint cvg::WR_DATA_2_0                     100.0%        100 Covered
   Coverpoint cvg::WR_DATA_3_1                       0.0%        100 ZERO
   Coverpoint cvg::WR_DATA_3_0                     100.0%        100 Covered
   Coverpoint cvg::WR_DATA_4_1                       0.0%        100 ZERO
   Coverpoint cvg::WR_DATA_4_0                     100.0%        100 Covered
   Coverpoint cvg::WR_DATA_5_1                       0.0%        100 ZERO
   Coverpoint cvg::WR_DATA_5_0                     100.0%        100 Covered
   Coverpoint cvg::WR_DATA_6_1                       0.0%        100 ZERO
   Coverpoint cvg::WR_DATA_6_0                     100.0%        100 Covered
   Coverpoint cvg::WR_DATA_7_1                       0.0%        100 ZERO
   Coverpoint cvg::WR_DATA_7_0                     100.0%        100 Covered
   Coverpoint cvg::WR_DATA_8_1                       0.0%        100 ZERO
   Coverpoint cvg::WR_DATA_8_0                     100.0%        100 Covered
 TOTAL COVERGROUP COVERAGE: 93.3%  COVERGROUP TYPES: 1
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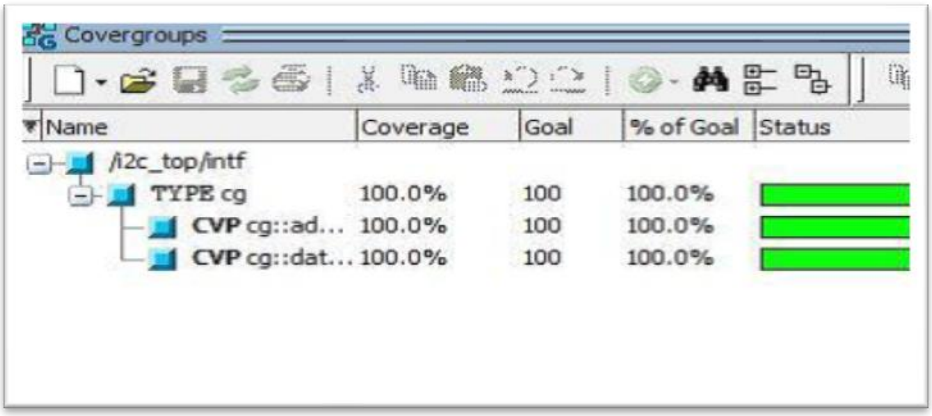
Figure.3 Code Coverage report

The Functional coverage of I2C master nothing but test bench verification components are the cover groups . All this scenarios successfully generated hence,functional coverage will be 100 percentage and it is shown in Figure 4.



Name	Coverage	Goal	% of Goal	Status
/i2c_top/intf				
TYPE cg	100.0%	100	100.0%	🟩
CVP cg::ad...	100.0%	100	100.0%	🟩
CVP cg::dat...	100.0%	100	100.0%	🟩

Figure.4 I2C master Functional Coverage Result.

6. Conclusion

In this Paper, Successfully designed the I2C protocol by using Verilog and generated the simulation. Design is verified by creating test bench verification environment using system Verilog language and its components like generator, driver, monitor, interface and scoreboard were implemented with help of Classes. Finally, for verification and design environment is applied the constrained randomization technique. Here, DUT (design) behaved as Slave and test cases (Verification components) as I2C master. DUT functions has realized by analysing the code coverage in the monitor which is obtained 93.3 percentage. I2C master functionalities has realized by Functional coverage and it is obtained 100 percentage. This is the simplest and easiest method of design and verification of I2C protocol using system Verilog.

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