Turkish Journal of Computer and Mathematics Education Vol.12 No.12 (2021), 767-780

Research Article

Ultra-Low Power Heterojunction Dopingless -Tunnel FET (HD-TFET) Design and Characterization with SiO2/HfO2 Gate Stacking for High Current Drive

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Article History: Received: 11 January 2021; Revised: 12 February 2021; Accepted: 27 March 2021; Published online: 23 May 2021

Abstract: A Heterojunction Dopingless TFET model with gate stacking has been presented for ultra-low power application using 2D layered material in the source-region to enhance the bandgap mechanism and thereby tunnelling probability. A layered phosphorene material (B-Ph) with moderate value of bandgap and low effective mass is used in the present work which also adds on in the characterization of proposed source-region of the SOI (silicon-on-insulator) heterojunction doping-less TFET (HD-TFET). The drain current expression is extracted by analytically integrating the band-to-band tunnelling generation rate over the channel thickness. High-κ HfO_2 has been layered on the top of SiO_2 to get a significant and effective gate oxide thickness, which results in the smaller OFF current (improved subthreshold conduction phenomenon) and offers an extremely low subthreshold swing of 1.8 mV/Decade. The proposed model also demonstrates that the proper choice of work function for both the latterly contacting gate electrode (near the source and drain) materials which can give better results in terms of input-output characteristics, Subthreshold Swing and I_{ON}/I_{OFF} than the conventional TFET devices. ATLAS™, a two-dimensional (2D) device simulator from Silvaco has been used in the device structure modelling and characterization. The numerical simulation of the proposed device is performed on. The device offers promising ON-OFF transition profiling with $\frac{I_{on}}{I_{off}}$ratio of $\approx 10^8$. The small signal behaviour of the proposed HD-TFET model has also been investigated and the performances of the B-Ph/Si gate stacked HD-TFET are observed promising for the possible implementation at circuit level.

Keywords: Tunnelling; Subthreshold swing; Low power; Heterojunction; Doping-less.

1. Introduction

As speed crisis in multi-gigahertz chips keep increasing, power dissipation problem on the other hand is looming large in the electronics industry. The key control to improve the performance per watt is to match up the pace of supply voltage (V_{DD}) down-scaling with device dimensions and simultaneously curbing the leakage current (I_{off}). Electrical transport studies show that chemically synthesized Silicon-Nanowires (SiNWs) have much less structural and dopant fluctuations than top-down fabricated silicon nanostructures, which leads to exceptional device characteristics often outperforming existing planar silicon technology. These nanoscale device trends has shown the great opportunities for applications ranging from high-density, scalable and integrated nanoelectronics to ultra-sensitive nanoscale sensors for chemical and biological detection. The goal of acquiring low standby power, however, largely depends on the subthreshold swing (SS) which must be low enough [1]. The conventional thermally excited transistors like MOSFETs are generally constrained by the thermal limit of 59.6mV/Decade. The tunnel field-effect-transistors (TFETs), also termed as Green transistors, aim to fulfil this demand by employing injection of charge carriers into the channel, which is called as quantum mechanical band-to-band tunnelling (BTBT). However, owing to tunnelling phenomenon, the low value of on-state current imposes a grave concern in the implementation of the tunnel FET devices in practical circuits. A higher current drive capability can be acquired by applying a stronger electric field to the source-channel tunnel junction [2]which necessitates a high gate voltage (V_g)despite the fact the tunnel FET needs to operate at a lower V_g to reduce power consumption. Moreover, conventional tunnel FET structures suffer from an unwanted trade-off between I_{on} and I_{off}, where the anticipated improvement of the former causes an unsolicited rise in the latter. In nutshell, a tunnel FET can be said to be a flawless alternative of the CMOS technology if it enjoys: i). high I_{on} ($\geq \frac{\mu A}{\mu m}$), ii). lowI_{off} ($\leq \frac{nA}{\mu m}$), iii). high V_g, iv). low V_{DD}($\leq$ 0.5 V), v). $SS \ll 59.6$ mV/dec and vi). high $\frac{I_{on}}{I_{off}}$ ($\geq 10^6$) [3, 4].

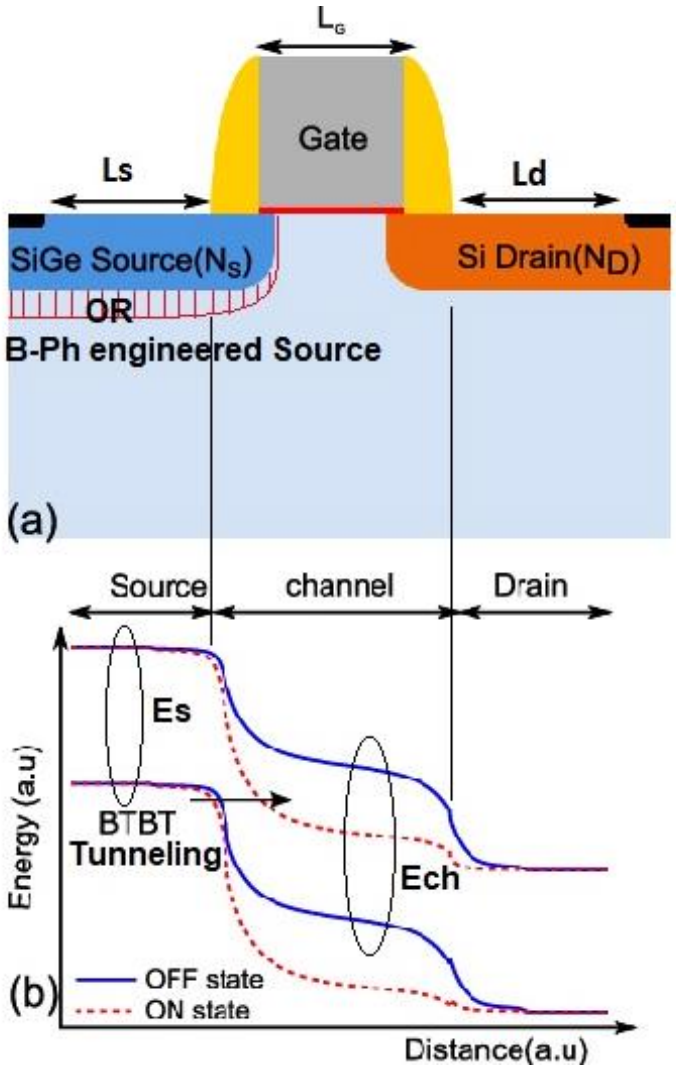


Figure 1: (a) Conventional Tunnel-FET structure having source-engineering with SiGe or narrow bandgap Black-Phosphorous (b) Enhanced band to band tunnelling in ON-state and low leakage effect in OFF state

Researchers have explored a number of possible techniques such as the bandgap engineering (i.e., use of lower bandgap materials such as InGaAs, InAs, Ge, and SiGe in the channel in place of conventional Si) [3]–[5], gate work function engineering (i.e., use of a metal with suitable work functions as the gate electrode in place of conventional poly-Si to eliminate the poly-Si/SiO2 depletion effect) [6], source/drain material engineering (i.e., use of low bandgap materials such as Ge and SiGe in source/drain with Si as channel) [7], [8], strain channel engineering (i.e., introduction of a strain in the Si-channel to enhance the mobility of channel carriers) [9], gate-oxide engineering (i.e., use of a high-k dielectric, a vertical stacked gate oxide structure of SiO2 and a high-k dielectric or a combination of partly high-k dielectric and partly SiO2 above the Si channel as gate oxide) [10], [11], and multiple gate technology (i.e., use of double gate (DG) and triple gate) [5], [12] to improve the ON-current of the TFETs.

In the present work, the source engineered tunnel FET with gate stacking is assessed in terms of transfer and current-voltage characteristics, subthreshold swing (SS), device capacitances and some important small signal parameters. An attempt has been made to report a 2-D analytical model for the surface potential, electric field, BTBT current, SS, and threshold voltage of the DM DG TFETs with a SiO_2/HfO_2 stacked gate oxide structure by considering the source/drain junction depletion regions. The remaining part of the paper is organized as follows: In Section 2, two major efforts namely a) gate stacking with high-k material and b) source bandgap engineering with 2D layered material to achieve the performances in nanoscale devices have been presented. The details of device structure along with simulation parameters are given in Section III. Section IV finally discusses the extracted TCAD simulation results and compares the numerical data with other heterojunction TFETs.

2. Drivers to achieve lower ioff with low subthreshold swing

As nanoscale devices keep offering the novelty trends in their structural design aspects, like Tunnel-FET, Nano-wire, Carbon Nano-tubes, Single Electron transistors, etc, much more rigorous mathematical modelling and characterization techniques are required to compete with the present time models. According to the Wentzel–Kramers–Brillouin (WKB) approximation, the tunnelling probability is calculated as:

$$\mathcal{T}_{\mathrm{WKB}} \approx \exp\left[-\frac{4\mathrm{l_T}\sqrt{2\mathrm{m^*E_g^3}}}{3\mathrm{q}\hbar(\Phi_{\mathrm{S}}-\Phi_{\mathrm{Ch}})}\right] \quad \text{(i)}$$

where l_T signifies the natural tunnelling length of the transition region across the source-channel interface; m^* be the effective mass; the energy bandgap is symbolized by E_g; q and $\hbar$ denote the electronic charge and reduced Planck's constant; the term $(\Phi_S - \Phi_{Ch})$ indicates the source-channel potential difference corresponding to the conduction band in the source and the valence band in the channel [13-15]. In a broadened manner, the tunnelling approximation suggests that the bandgap and effective mass in the tunnelling region should be minimized for high tunnelling probability [12, 15-17]. The heterostructure design, in which material in the source (small bandgap) is dissimilar to the material in the channel and the drain (large bandgap), serves the above purpose to a great extent. The performance of H-TFETs regarding bandgaps and scaling tunnelling lengths across the source and channel interfaces in H-TFETs built on InAs/InGaAsSb/GaSb were optimized effectively with the on-state current of several $\mu A/\mu m$ [18–22]. In H-TFETs, the lattice matching of strained-source material with silicon film imposes another challenge for the device fabrication which, in consequence, deforms the real lattice and causes inflated bandgap[21, 23]. In other words, the silicon heterojunction TFETs are severely prone to performance degradation with the use of classical bulk materials for the source region.

The overall efforts in heterojunction TFETs structures' modelling for low subthreshold swing and lower I_{OFF}, are classified in the following two categories:

A. Effective Gate thickness with High- κ Gate-Stacking

It may be mentioned that the electrical characteristics of the TFETs can be improved significantly by replacing the conventional SiO_2 by a stacked gate oxide of SiO_2 and a high-κ material [10] in the DG TFETs. As the thickness scales below 2 nm, leakage currents due to tunnelling increase drastically, leading to high power consumption and reduced device reliability. The use of silicon nitride instead of silicon oxide as barrier layer can improve the effective capacitance of the gate dielectric stack, since silicon nitride has a higher permittivity (≈ 7) than silicon oxide (≈ 3.9). But if the aim is to enhance the overall thickness of the gate oxide, a high- κ dielectric material like HfO_2 (used in this work) in addition to thin SiO_2 appears to be most suitable due to its compatible inter-layer compatibility with Si and SiO_2. Replacing the silicon dioxide gate dielectric with a high-κ material allows increased gate capacitance without the associated leakage effects. On the other hand, the above discussions show that DMG-based TFETs possess better SS and ON-current characteristics over the SMG-based TFET structures. Thus, it can be easily expected that both the SS and ON-current of the TFETs can be significantly improved by combining the DMG and SiO_2/high-k stacked gate oxide structures in the DG TFETs.

B. Source Bandgap Engineering with 2D layered material

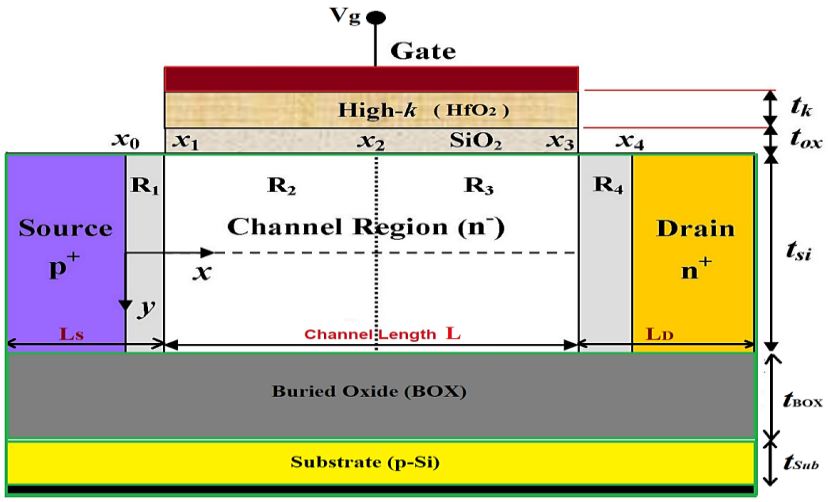
Two-dimensional (2D) layered semiconductors materials may efficiently ameliorate the above-mentioned aspects in H-TFETs as the number of layers in 2D materials is firmly linked with electronic bandgap, and carrier mobility, which are vital to the overall device performance [24–26]. Many researchers have investigated the use of most popular 2D material graphene in TFETs by tuning the bandgap properties including symmetry-breaking operations, or by stacking two layers and applying an electric field [27, 28]. In contrast to other 2D layered material family members like graphene and transition-metal dichalcogenide (TMDC), black phosphorus (B-Ph), also known as phosphorene, is gaining popularity among device designers related to low-power electronics [26]. Bulk phosphorene is a semiconductor with a direct band gap of 0.3 eV, and as the film thickness reduces, the bandgap progressively widens to 2 eV for monolayer phosphorene [24, 29]. The moderate value of bandgap (0.3-2 eV) along with low effective mass $0.146m_e$ makes B-Ph an appropriate candidate for use as source-material in H-TFET applications [24, 29]. From this point of view, Kumar et al. [23] had proposed a stacked metal gate TFET with phosphorene as source material for 30 nm channel length with emphasis on line tunnelling.

In the light of the above-mentioned facts, the present work is dedicated to explore the possibilities of the black phosphorus as source-material in silicon channel-based tunnel FETs for the sub-20 nm technology node. In the proposed B-Ph/Si HD-TFET, the ultra-thin body (channel region) placed over buried oxide (BOX) is kept undoped

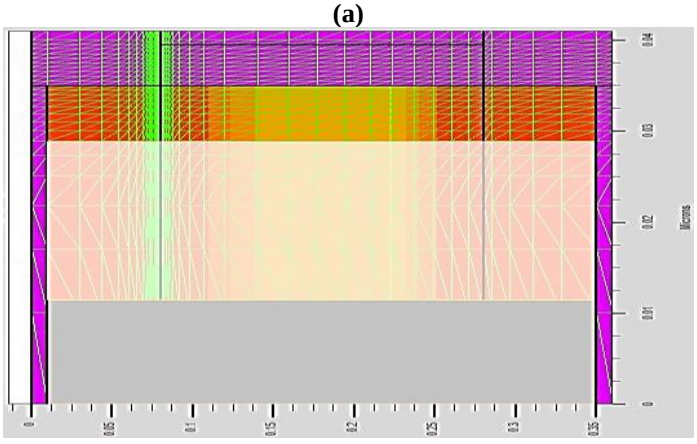
to improve the mobility and hence the performance of the device. The present heterojunction doping-less TFET is designed and simulated for point tunnelling across the source-channel interface [6,19,20]. For this purpose, a heavily doped source with an abrupt doping profile is required to maximize $\frac{I_{on}}{I_{off}}$, which inherently possesses a relatively small tunnelling area. Further, compared to bulk materials, atomic packing factor and density of states (DOS) in 2D materials are extremely low, and little number of foreign atoms are enough to realize heavy doping [24]. Therefore, the number of doping atoms in the black phosphorus source-engineered region of the HD-TFET should be cautiously controlled [23, 31]. Such stringent doping conditions are effortlessly feasible with electrostatic doping in comparison with the conventional ion-implantation and thermal annealing techniques [32, 33].

3. Hd-tfet: simulation models and environment

The proposed schematic cross-sectional view of the doping-less TFET (B-Ph/Si HD-TFET) device with source-engineered Si-heterojunction is shown in Fig. 2. All the dimensions shown in the diagram are not up to the scale and merely represent the proposed idea of the TFET structure. All the targeted dimensions have been marked; where, L_S, L_D, L, t_{ox}, t_k and t_{si} represent source-region length, intrinsic drain-region length, intrinsic silicon-channel length, gate-oxide thickness, high-κ HfO_2 thickness and silicon film thickness respectively. t_{BOX} and t_{sub} represent the buried oxide thickness and the substrate thickness respectively. In spite of the conventional ion-implantation methodology, the electrostatic doping is done in the source region to achieve the targeted higher value of work-function for metal electrode compared to channel material. This enhances the band bending in the source engineered region with higher probability of tunnelling. Moreover, Plasma based methodology has been adopted here for the development of source (p-type) and intrinsic-Si drain (n-type) regions as PLAD (plasma doping) has shown the promising results for both evolutionary and revolutionary doping options due to its unique advantages which can overcome or minimize many of the issues of the beam-line (BL) based implants [34, 35]. In order to make metal-drain electrode contact, the work-function of metal electrode is kept inferior to the channel region material.



(a)



(b)

Figure 2: (a) Cross-sectional Schematic of the Proposed TFET structure with SiO2/HfO2 stacked gate oxide.

(b) Actual image of the simulated TFET profile with meshing through vertical and horizontal dimensions

The simulated structure in ATLAS-2D model for the proposed dimensions has been shown in Fig. 3(b), which depicts various regions and meshing. The meshing strategy shown in the figure is also clearly visible to promote the finer calculations in the high tunnelling region near B-Ph/Si interface at source-channel. Various cut-lines have been made along the vertical and horizontal directions in order to observe and characterize the doping profile, electric fields, tunnelling probabilities and capacitances across the electrodes.

The silicon film serving as the channel region is doped above the buried oxide (BOX) layer, with lightly p-type doping profile. The numerical values of the dimensional and physical parameters considered for the simulation of the B-Ph/Si gate-stacked HD-TFET structure is given in Table-1. The fabrication steps may have some technological challenges, but with swift advancements in the technology, the device can be realized in the near future. The TCAD simulations of the heterostructure tunnel FET have been performed on ATLAS which uses a nonlocal band-to-band tunnelling (BTBT) model along with quantum correction. The non-local derivatives are included in the Jacobian matrix by activating the bbt.nlderivs code [36]. For the simulation purpose, a very fine meshing has been done across the region where the propensity of tunnelling is very high (this could be seen in Fig. 2(b)). The gate-leakage was assumed to be neglected during simulations and can be expected to limit the Off-state current in the fabricated HD-TFET. Besides enabling the bandgap narrowing (bgn) model, electric field dependent Lombardi mobility model (CVT) was activated, which in general accounts for degradation in carrier mobility caused by higher scattering of mobile carriers by the interface charges near the Si-SiO_2 interface.

Table-1: Design parameters for the proposed HD-TFET structure [23, 29].

Parameters	Value
Source Length (Ls)	16nm
Channel Length (L)	50nm
Channel Doping (N_A)	$10^{15} cm^{-3}$
Source Doping	$10^{20} cm^{-3}$
Drain Doping	$10^{18} cm^{-3}$
Gate Oxide (SiO_2) Thickness (t_{ox})	1nm
High-k Dielectric (HfO_2) Thickness ($\boldsymbol{t_k}$)	2nm
Channel Thickness ($\boldsymbol{t_{si}}$)	10nm
BOX Thickness ($\boldsymbol{t_{BOX}}$)	110nm
Substrate Thickness ($\boldsymbol{t_{Sub}}$)	60 nm
Metal-Gate Work-function ($\boldsymbol{\phi_M}$)	4.82 eV
Black Phosphorus (B-Ph) Mono-layers Thickness	8nm

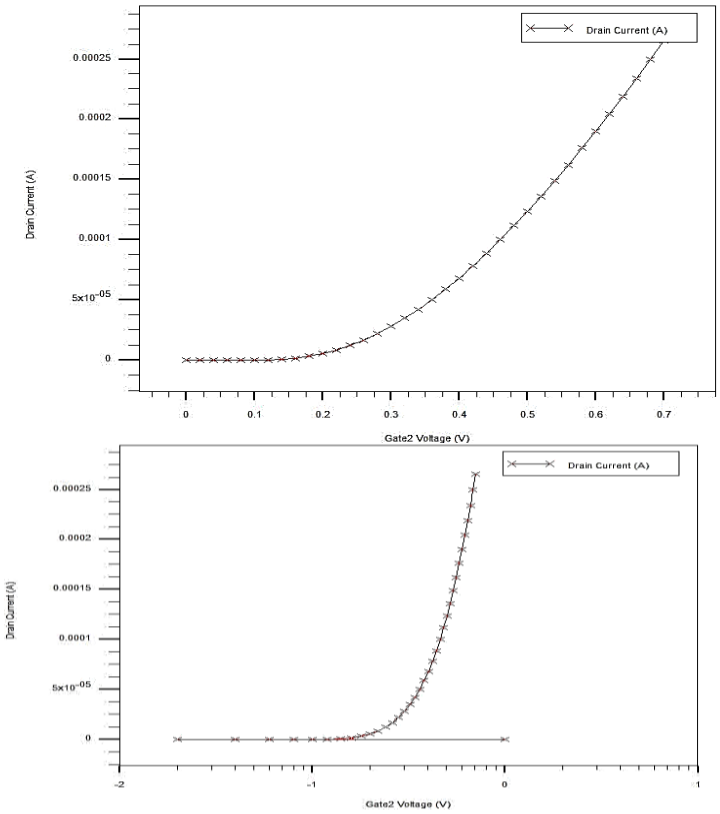
The Fermi–Dirac (FD) statistics was incorporated by enabling the Fermi model at 300K. In SOI transistors, the recombination effects play a critical role due to the presence of two active silicon-oxide interfaces. For this, Shockley–Read–Hall (SRH) recombination models along with direct recombination AUGER model (AUG) accounting for high carrier density have been employed [36].

4. Simulation results: analysis and discussion

The device simulations and characterizations have been performed using ATLAS-2D (SILVACO) tool. The proposed HD-TFET structure has been obtained and already presented in fig. 2(b). In this section, we will compare our model results with the ATLAS-based TCAD simulation data of our proposed DM DG TFET with SiO_2/HfO_2 stacked gate oxide structure. The Auger recombination, bandgap-narrowing (BGN), Shockley–Read–Hall recombination (SRH), concentration, electric field dependent Lombardi (CVT), and nonlocal BTBT models have been used for TCAD simulation of the proposed device. In sub-section A, the most important I_{ON}, I_{OFF} and subthreshold characteristics have been presented; secondly, the plots related to energy band and Band to Band tunnelling (BTBT) are presented in sub-section B and manifestation of gate stacking has been claimed. Sub-section C at the end invokes the small signal features of the device by investigating the capacitances across electrodes defined in the model and discussion of transconductance parameter follows.

A. Subthreshold and I-V Characterization

The most significant current voltage (I-V) graph has been simulated and plotted in Fig. 3, where the experimental results from various references and similar works have been compared to enhance the accuracy of the extracted simulation data.



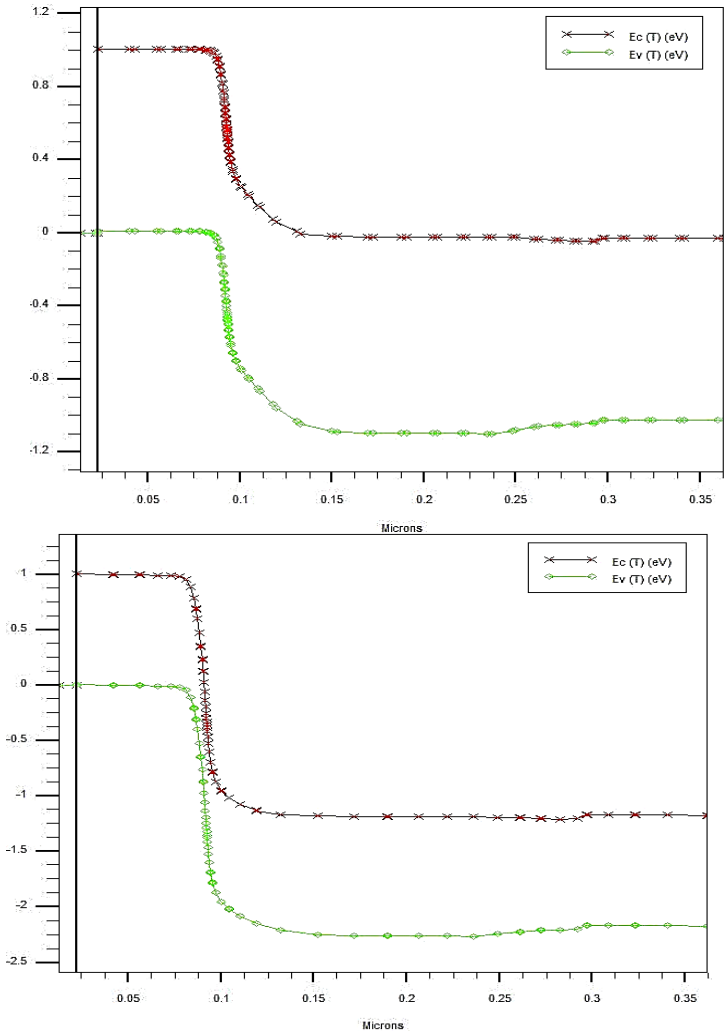
(a) **(b)**

Fig. 3. Simulation data of drain current (I_{DS}) versus gate-to-source voltage (V_{GS}) of the proposed HD B-Ph/Si Gate Stacked tunnel FET (a) Linear scale Id (b) Log-scale Id

The current values are appropriate and fit to the expected range. Current reaches to value as high as 250μA at a feasible gate drive of 0.7Volts, illustrating the excellent ON current drive capability. Gate turn on phenomenon also happens at a much lower gate voltage as compared to conventional FET counterpart, highlighting the feature of source region bandgap engineering. An excellent agreement has been obtained between the experimental data offered by Ganjipour et al. [22] and the simulation results of the present work. The electrical characteristics of the B-Ph/Si gate-stacked HD-TFET have been examined in the light of the calibrated results. A negligible OFF current (sub-threshold mode conduction) of the order 10^{-13}A is observed, which is attributed by the gate stacking with high-κ material (HfO_2 here).

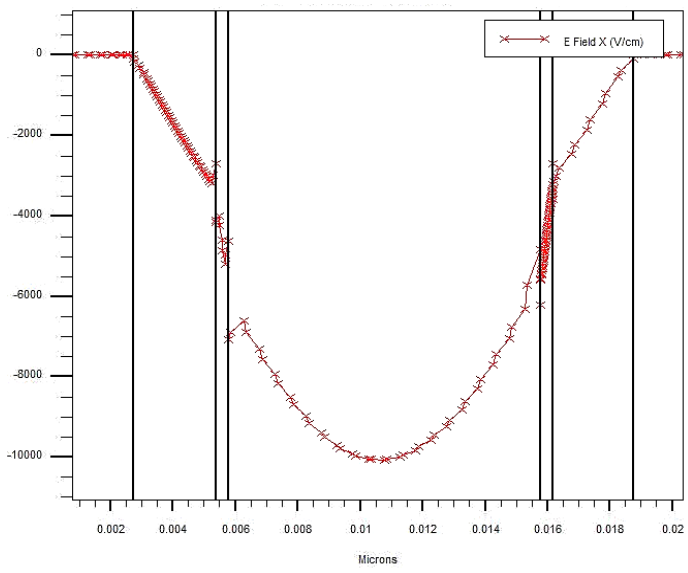
B. BTBT profiling with Energy bands

The energy-band diagram of the HD-TFET along the channel length direction in off-state as well as on-state is presented in Fig. 4. Note that, the bandgap of black phosphorus is much smaller than silicon. A pronounced band-bending can be observed inside and near the source region which results in a denser electric field and smaller tunnelling distance across the junction, rendering a large tunnelling current from source to channel [13, 16, 37]. The additional advantage of the proposed B-Ph/Si gate-stacked HD-TFET and gate stacking with high-κ material is the occurrence of BTBT tunnelling inside the low bandgap region (source), which makes the device an efficient choice. A significant variation in the band bending is clearly visible from Fig. 4(a) and (b), which respectively demonstrate the ON and OFF conditions of the device.



(a) **(b)**

Fig. 4. The energy-band diagram depicting conduction band (CB) and valence band (VB) profile across the source and channel interface at (a) $V_{GS} = V_{DS} = 0V$ (off-state) and (b) $V_{GS} = V_{DS} = 0.6V$ (on-state).



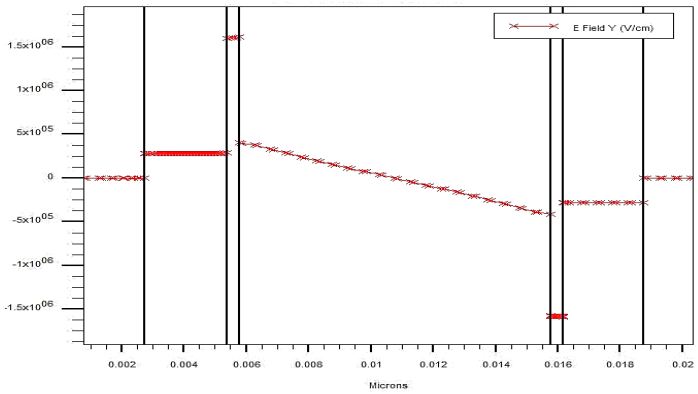
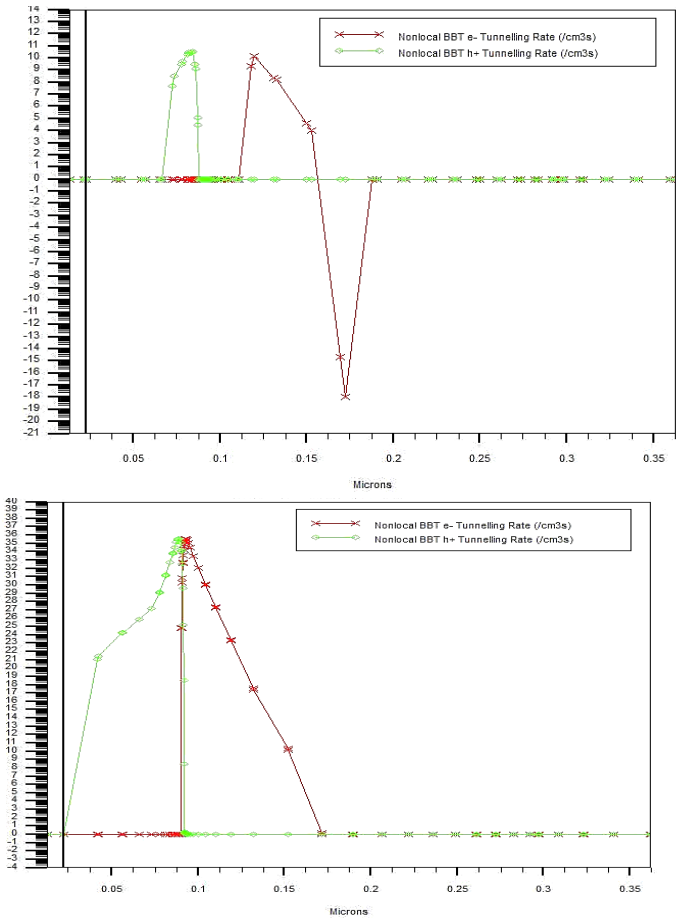


Fig. 5. The Electric field profile across the source and channel interface in (a) *lateral dimesion* (Ex) and (b) *vertical dimension* (Ey)

The variations of lateral (Ex) and vertical (Ey) electric fields with respect to channel position have been plotted in Fig. 5(a) and (b) respectively, for a fixed gate oxide thickness of 3 nm of either HfO_2 or SiO_2 and their combination in the form of a stacked oxide of 3 nm. The magnitude of both the electric fields are increased with the increase in the thickness of the high-k HfO_2. The negative electric field near the drain side will decelerate the carriers to reduce the ambiploar behavior of the device [18].

The transfer characteristics (i.e., Id versus V_{GS}) of the HD-TFET with SiO_2, HfO_2, and SiO_2/HfO_2 stacked gate oxide of fixed thickness of 3 nm shown in Fig. 3(a) confirm the increase in the drain current due to the increase in the high-k HfO_2 thickness. This is attributed to the increase in the electric field with the increase in the HfO_2 thickness, as demonstrated in Fig. 5(b). The drain current (Id) versus drain voltage (V_{DS}) relation for different gate voltage (V_{GS}) explains the increase in Id with V_{GS} due to the reduction in the source–channel barrier height.



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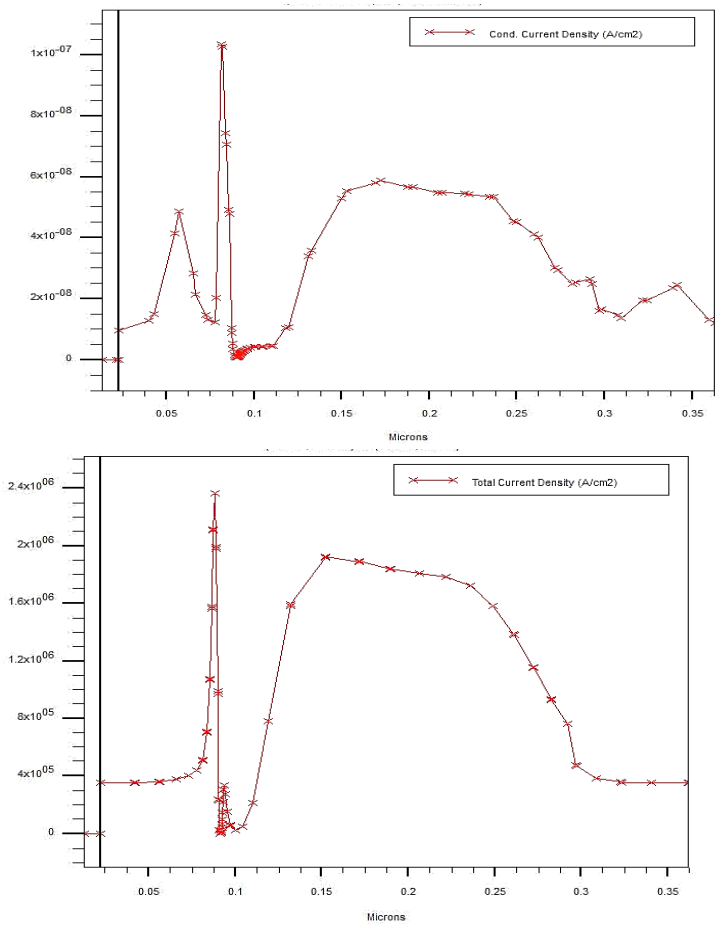


(c) **(d)**

Fig. 6. Plots of non-local BTBT rate in (a) OFF state, (b) in ON state and total current density in B-Ph/Si HD-TFET at (c) OFF state at $V_{GS} = V_{DS} = 0.05V$ and (d) ON state at $V_{GS} = 1V$

Fig. 6 confirms the claim and provides a better understanding into the source engineering of the HD-TFET. Fig. 6(a) represents the poor BTBT tunnelling probability near the source-channel interface due to OFF mode (Vd= Vg= 0.05V), whereas the tunnelling rate suddenly shoots up in Fig. 6(b) for the ON mode, and the plot of the nonlocal e-BTBT rates at $V_{GS} = V_{DS} = 1V$ establishes the claim that the maximum electron BTBT rate centres are positioned inside the source region. Such intense BTBT rate inside the source region is attributed to the use of the layered 2D material (B-Ph) of very small bandgap (E_g). Further, the BTBT rate in the Si-channel is found inferior owing to the presence of conduction band (CB) offset ($\Delta\chi$) caused by the electron affinity difference between the source material (B-Ph) and Si-channel. Moreover, the plot of total current density in Fig. 6(c) and (d) for OFF and ON modes respectively shows the tunnelling current confinement near the oxide/channel interface which indicates a good gate control over the channel region.

C. TFET Performance Estimation for Small-signal applications

This section assesses the small signal qualifications and characterization of the B-Ph/Si Gate-Stacked HD-TFET. The transfer characteristics of the HD-TFET is plotted for V_{DS}= 0.5V in Fig. 7, for channel lengths $L = 14nm, and\ 28nm$. The off-state current for all the channel lengths is found in the range of$10^{-16}A/\mu m$ which is due to the good gate control over the channel region as already mentioned above (refer to Fig. 3(a) and (b)) and attributed to the high-κ gate material. This value is far above the requirement stated by international technology roadmap for semiconductors (ITRS) for low-power applications, which sets the target for I_{off} at $10pA/\mu m$, with $\frac{I_{on}}{I_{off}} > 10^5$ [16].

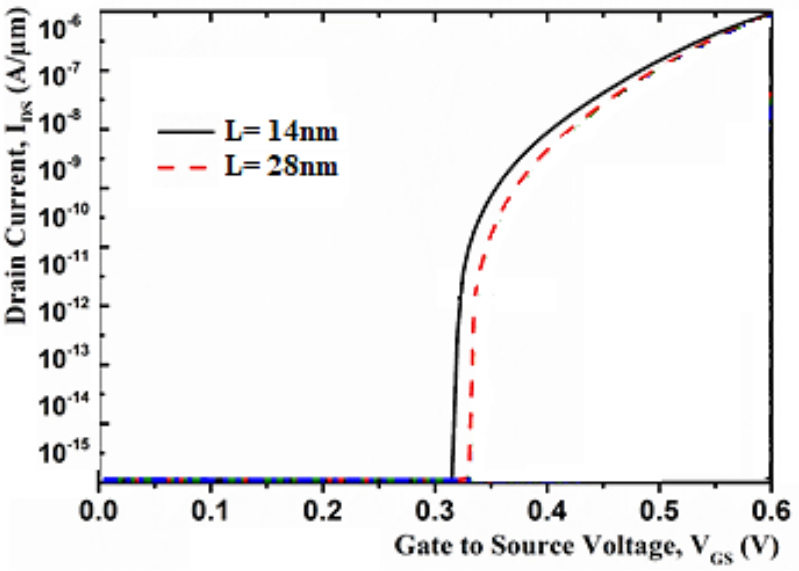
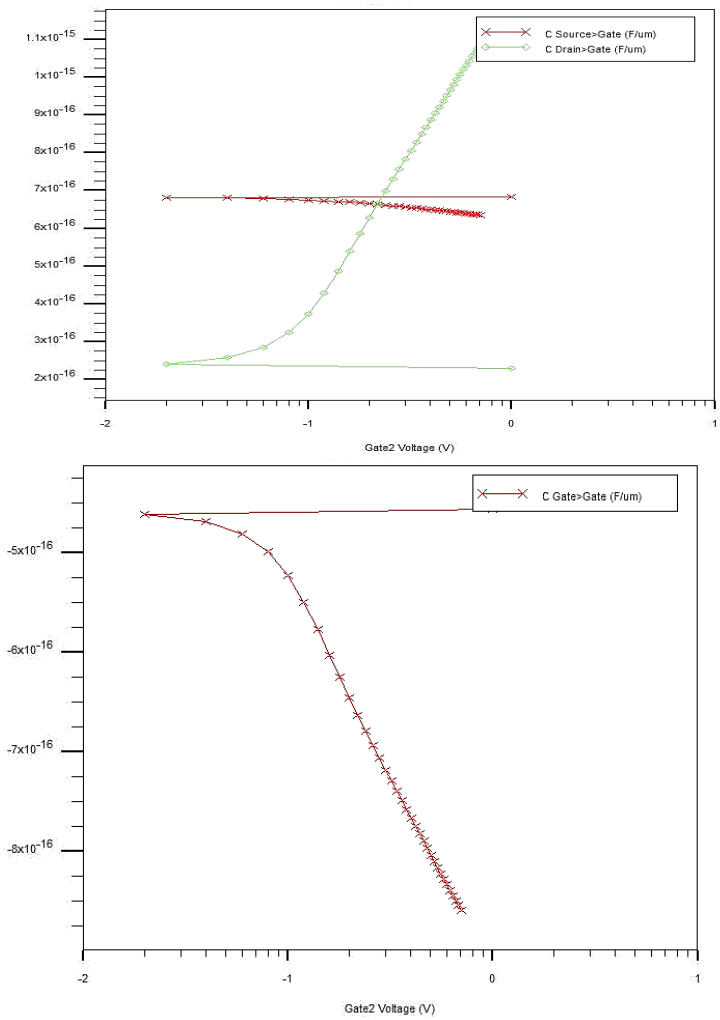


Fig. 7. Transfer characteristics of the proposed HD-TFET structure at $V_{DS} = 0.5V$ for four different channel lengths.

Further, the drain current can be seen rising up to $4.0\mu A/\mu m$, having the higher value in the HD-TFET for $L = 14nm$. Obviously, I_{off} increases exponentially as threshold voltage is decreased and the curve moves leftwards. Another noticeable point taken out from the logarithmic plot of the drain current is the variation of the same against gate voltage above $0.3\ V$. For the given value of gate voltage, e. g. $V_{GS} = 0.4V$, an increment in drain current of 25% for the $L = 14nm$is observed as compared to other channel lengths. The proposed source-engineered HD-TFET device can be seen having very fast on/off transition performance. For $L = 28nm$, the $SS = 1.8mV/Decade$ with the corresponding $\frac{I_{on}}{I_{off}} = 1.5 \times 10^8$; whereas for $L = 14nm$, the SS rises up to $1.97mV/Decade$ with the corresponding fall in $\frac{I_{on}}{I_{off}} = 0.4 \times 10^8$. The very low value of SS of the B-Ph/Si gate stacked HD-TFET can be attributed to the presence of extremely small energy window created by the junction of black phosphorus (B-Ph) and Si-channel. Such energy window causes energetic filtering by BTBT carrier injection in which the high-energy part of the source Fermi distribution gets effectively cut off [13].

The AC simulation of total gate capacitance (C_{GG}) has been performed by coupling an input small AC signal with DC bias at the gate terminal. Fig. 8(a) and (b) illustrate the variation of gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}) and gate-to-gate2 capacitance respectively as a function of gate voltage for the HD-TFET device. Because of doping-less region of channel and drain regions, the C_{GS} variation across off-state to on-state is almost unaffected from the gate voltage is $0.7\ fF/\mu m$. Further, wide variation in C_{GD} can be seen ranging from $0.3\ fF/\mu m$ to $1.1\ fF/\mu m$, however, more pronounced in the saturation region. Such low values of intrinsic capacitances are quite interesting from the circuit designer point of view. However, the graphical trends in C_{GS} and C_{GD}can be seen a bit differing from the traditional TFETs intrinsic capacitance plots [37–39]. The smaller capacitance reason is the source engineering in HD-TFET, where the low value of electron's effective mass in black phosphorus stimulates larger storage of electrons near the source-channel interface with increasing gate voltage.



(a) **(b)**

Fig. 8. Intrinsic capacitances (a) C_{GS} and C_{DS} as a function of gate voltage at $V_{DS} = 0.05V$ and (b) gate-to-back gate capacitance C_{GG}

As soon as the BTBT across the channel commences, the capacitances (C_{GS}, C_{GD}) tune themselves in parallel combination ($C_{GG} = C_{GS} + C_{GD}$) in the HD-TFET. The lower the total gate capacitance, the smaller will be the intrinsic delay of the device. The highest C_{GG} goes up to 0.8 $fF/\mu m$ and to a lowest value of 0.48 $fF/\mu m$. The important characteristics are compared and summarized in Table-2 depicts selected data of other reported tunnel FETs in literature.

Table-2: Comparative Analysis of present Work against some contemporary and similar efforts/works for reported heterojunction tunnel FETs

Devices/work	**Supply, Vdd (V)**	**SS (mV/Dec)**	$\frac{I_{on}}{I_{off}}$	g_m **(S/μm)**	**I_{ON} ($mA/\mu m$)**	TGF **(V^{-1})**	C_{GG} **($fF/\mu m$)**
DMG InAs TFET [4]	0.5	6	10^8	10^{-5}	2	-	-
DG-TFET with SiO_2/High-k [10]	1.5	-	-	-	4.7	-	3.2
InP-GaAs Hetero Tunnel FETs [22]	-	50	10^7	-	-	-	0.09
Graphene Vertical TFET [28]	1	-	100	-	2	-	-
InGaN GEDL-TFET [37]	-	7.9	10^{13}	10^{-4}	-	-	1.5

UL DG-TFET [38]	1.2	-	-	-	-	13	0.04
Hetero-Gate Dielectric TFET [39]	2	14.7	-	-	10		
This Work: Gate Stacked HD-TFET	**1.2**	**1.8**	**10^8 with I_{OFF} as low as 10^{-13}A**	**10^{-4}**	**2.4**	**10^5**	**0.48**

On the basis of Table-2, the proposed B-Ph/Si Gate-Stacked HD-TFET demonstrates a good digital performance and may be projected for ultra-low-power analog and digital applications at $V_D \leq 0.5V$.

5. Conclusions

A heterojunction tunnel FET with two major efforts of source bandgap engineering and gate-stacking (high-κ material) is proposed in which a 2-D analytical model for surface potential of DG TFET with HfO_2/SiO_2 stacked dielectric material has been developed by taking the source/channel and drain/channel depletion regions into consideration. A 2D material called black phosphorus has been used as source-material to engineer the bandgap and hence tunnelling probability at source-channel interface. *The electrical characteristics of* the B-Ph/Si gate-stacked HD-TFET are observed to deliver much better performance compared to traditional heterojunction TFETs. The work functions of the tunnelling and auxiliary gates of the DMG structure have been optimized to attain better results in terms of ION/IOFF ratio, ambipolar effect, and SS of the device. The leakage current (I_{off}) is found to be effectively suppressed below ($10^{-14}A/\mu m$) rendering much improved $\frac{I_{on}}{I_{off}}$ current ratio of the order of 10^8 with tremendously small subthreshold swing of 1.8 mV/Decade. The proposed B-Ph/Si gate-stacked HD-TFET demonstrates high transconductance factor with small gate capacitance (C_{GG}) of $0.48\ fF/\mu m$. Such low value of C_{GG} pushes the sourced-engineered HD-TFET to achieve lower F_t in the terahertz range approximately. The important device characteristics of the simulated proposed HD-TFET are summarized in Table-2, and comparisons are made with other reported tunnel FETs. The high value of $\frac{I_{on}}{I_{off}}$ current ratio, superb small signal characterization in terms of lower intrinsic capacitances even at 14nm of channel length indicates that the black phosphorus source engineered heterojunction doping-less tunnel FET embodies a competent candidate for high speed analog as well as digital applications. Model results are found to be in good agreement with the SILVACO ATLAS-based TCAD simulation data.

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