Assessment of Z-Source Based 7 level cascaded Multi Level Inverter for Induction Motor Control using Embedded Technique

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Abstract: In recent decades, an Induction Motor (IM) becomes more superior in the industrial drives because of its ruggedness, relatively inexpensive and of its reliability. Hence to control the operation of IM, conventional Voltage Source Inverters (VSI) are implemented. However they results in poor voltage and current at its output. Thus, an effective available alternate solution to control IM instead of traditional VSI is a Multilevel Inverter (MLI). The output voltage of the MLI is the summation of number of levels of DC voltage sources. Hence the output voltage of the inverter can be improved by increasing the levels of the DC source. It also has other advantages output voltage of the MLI includes low voltage stress, reduced harmonics distortion and lesser Electro Magnetic Interference (EMI) etc., However, the dependency of the output voltage on the input DC source is the major shortcomings of MLI. Hence to override this constraint, this work proposed a novel a Z-source based seven-level cascaded multilevel inverter for IM. In this work, a Z source network is introduced to step up /down the inverter voltage. Thus to examine the efficiency of the proposed system, simulation of proposed MLI is carried out in MATLAB. Simultaneously, experimental results of the proposed MLI were also provided to verify its efficiency practically.

1. Introduction

The traditional VSI that has been implemented for IM are insufficient to handle the widespread voltage change and so it needs an additive dc-dc converter to manage this situation. But his arrangement will experience high power loss and cost. Hence to overwhelm these limitations, a multilevel inverters is instigated.

Usually, the MLI's are classified into

- NPC,
- Flying Capacitor
- Cascaded H-bridge inverter (CMLI).

All these exhibit their own merits and demerits [1-4]. Out of these configuration, CMLI is considered to be best because it affords reduced harmonics, high di/dt protection, reduction in common mode voltage and less electromagnetic interference.

Regardless of these advantages, the output voltage amplitude of these multilevel inverters is limited by the input DC sources. Therefore to solve this problem, a novel Z-source inverter is introduced. The Z-source inverter make use of an intermediate Z impedance network between the DC source and inverter circuit to achieve the buck/boost operation. During shoot-through state, it boosts the input of inverter switches. Under this condition, both the switches of same phase leg remains "ON". These type of Z-Source inverters are lower in cost, more reliable, and has higher efficiency.

Muntean et al (2008) anticipated a closed loop operation of a z-source inverter to boost the level of input voltage. Gao et al (2009) have studied a performance a 5 level z source NPC with two intermediary z source networks which is connected in between the input sources and output inverter circuit. An isolated step up DC/DC converter with ZSI has been proposed [7]. Singh et al [8] studied an comparative analysis of PI and PWM control for induction motor. Sengolarajan et al [9] suggested a 3Φ 3 source MLI with multicarrier SPWM strategies. An extended inductor based quasi ZSI with high efficiency is presented in [10]. Bhujangaro et al analysed a performance different levels of Cascaded H-bridge inverter using sinusoidal PWM technique. Gaddafi Sani Shehu et al has made a review on multilevel inverter topology and its control techniques. Himanshu et al examined the various topologies of Z-source inverters. The operation states during shoot through and non-shoot through state of

ZSI is described in [13]. Balamurugan et al (2016) has made a review on modulation strategies of MLI. Thus, the performance of 3Φ asymmetrical MLI with reduced switches is analysed. Vijayalakshmi (2017) projected an embedded based controller for Z-source multilevel inverter.

Although, a numerous researches has been conducted to study the performance Z source inverter, the efficiency of the proposed topologies remains low in case of IM. Hence this work presents a novel the combined effect of multilevel inverter with Z source for Induction motor.

Numerous pulse width modulation patterns have been developed for MLI. Based on the selection of PWM topology, the period of switching pulses are altered in accordance with the presence of harmonic content. Thus the proposed topology consists of seven level cascaded multilevel inverter with Z impedance network to regulate the induction motor and modified Space Vector Modulation (SVM) was effected to generate switching pulses to VSI. Figure. 1 demonstrates the configurations of a proposed system.

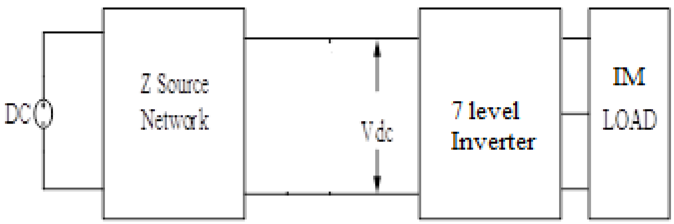


Figure 1. Configurations of the proposed system

Thus the proposed system consists of four parts namely, DC voltage, Z-Source network, a three-phase inverter bridge and a three-phase induction motor drive. Thus the boost function is accomplished by the Z-source network. The output of the Z cource network is fed into the multilevel inverter as depicted in figure 2.

2. Proposed Methodology

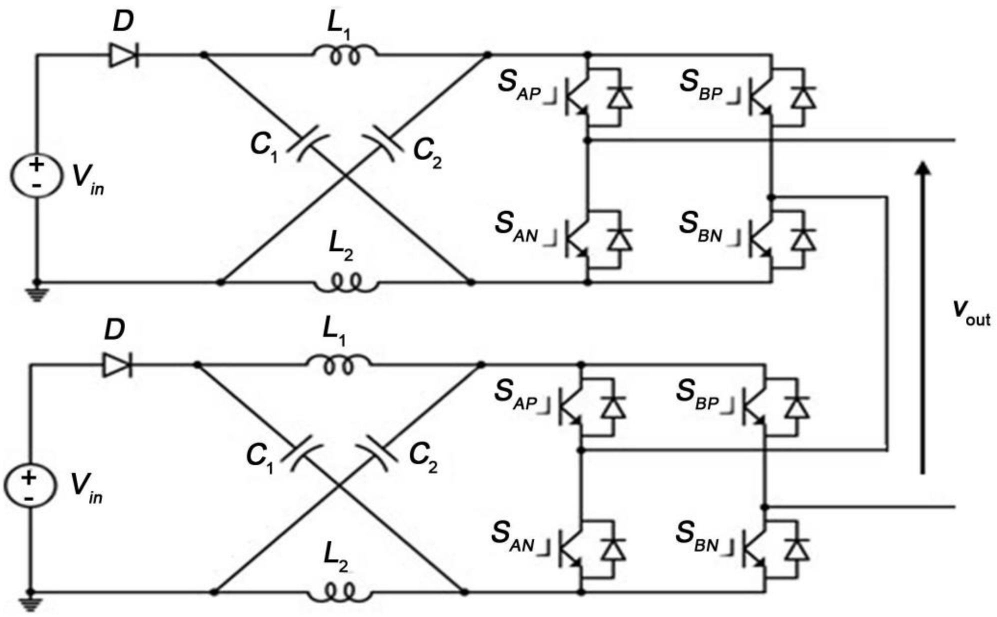


Figure 2. Anticipated Z source cascaded H bridge inverter.

It consists of an H bridge inverter units, Z impedances and DC voltage sources.

3. Design of Multilevel Inverter

Each H-bridge Z-Source inverter can generate three different output voltage +Vin, 0, -Vin. Thus the summation of all the discrete inverter outputs altogether forms the output voltage of MLI. In this cascaded type, each and every switching device will come into conduction stage at 180˚. Hence, this topology reveals equivalent current stress over the active device. So this topology becomes more popular in high voltage and power applications. Apart from this , it also results in reduced harmonic distortion with less switching frequency.

4. PWM Strategy

Space Vector Modulation (SVM)

The most commonly used techniques for effecting the pulse width modulation (PWM) control over the MLI's are SPWM and SVPWM. More number of techniques are available for executing SVPWM for multilevel inverters. In general, the SVPWM implementation involves the identification of sector, switching time calculation, switching vector determination, and optimum switching sequence selection for the inverter voltage vectors. This proposed scheme used sector identification for SVPWM implementation. A technique using the principle of mapping is utilized for generating the switching vectors for a multilevel inverter. This algorithm can also be implemented for any n-level inverter.

5. Simulation Results

The simulation results of propose ZS based cascaded H bridge multilevel inverter fed with induction motor load is shown below. Figure 3 and 4 displays the output voltage /current of the proposed Sven level inverter.

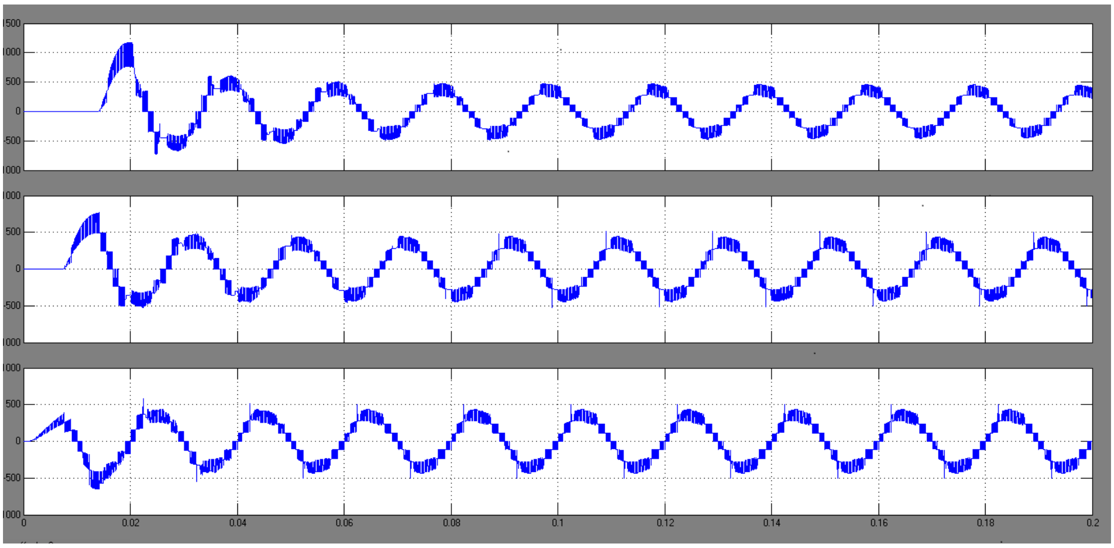


Figure 3. Output Voltage across the inverter

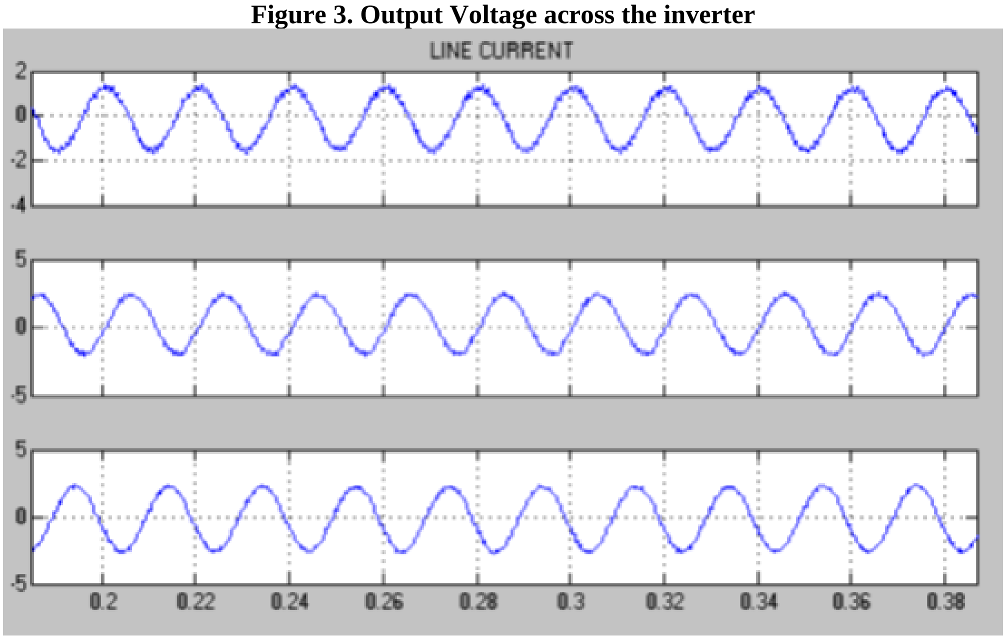


Figure 4: Current across the inverter

Figure 5 displays the speed and torque waveforms of the motor speed and torque obtained for proposed system. From the figure, it is observed that the motor attained it's maximum speed of 1200 in three seconds.

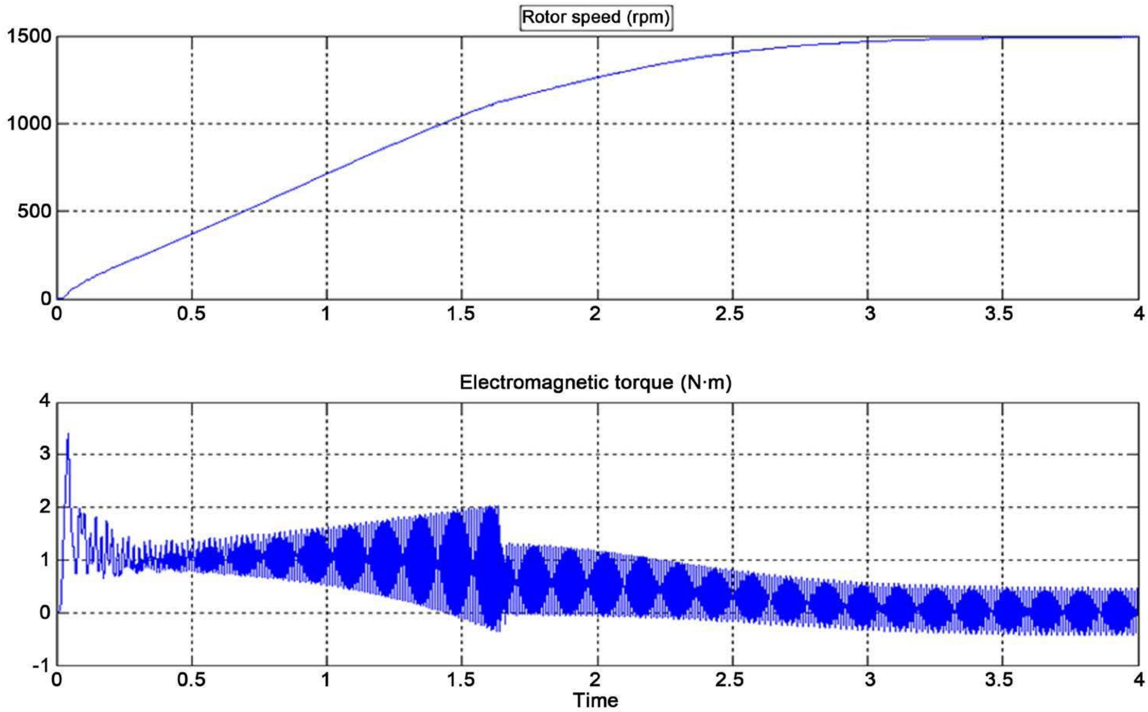


Figure 5. Motor speed and torque of ZS integrated seven level inverter

Performance Analysis

The efficiency of proposed system is analyzed in terms of order of harmonics, form factor and crest factor.

THD analysis:

THD of a signal is a measurement of the harmonic distortion present in the system. The Total Harmonic Distortion (THD) achieved for the proposed system is depicted in Figure 9,

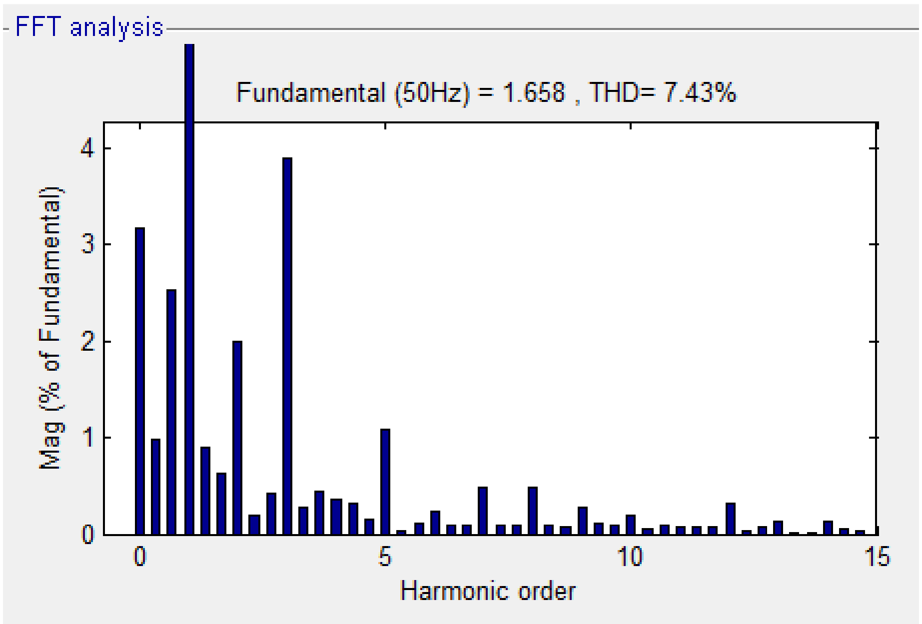


Figure 6. Total harmonic distortion of Z-source inverter

From the figure 6, the THD is found to be 7.43%. From the figure, it is obvious that the amplitude of the significant harmonics and its sidebands are reduced by the proposed modulation technique.

Experimental Results

After the simulation studies, an PIC microcontroller based seven-level inverter fed IM is fabricated and tested. The experimental validation includes the control circuit, the driver circuit and the power circuit. A. Control Circuit The control circuit was implemented using an ATMEL AT89S52 8-bit microcontroller. Reasons for choosing an ATMEL Microcontroller are as follows: 1) Self-sufficient standalone device (lC) 2) Cost- effective & less power consumption 3) Reliability of the system 4) Software protection 5) Wide availability The gate pulses are produced by the ATMEL AT89S52 Microcontroller. These pulses are amplified using the seven driver ICs 6N136.

B. Driver Circuit

The driver circuit describes about the isolation between the power circuit and the control circuit and the power supplied to the IGBTs.The circuit operates with the two transistor logic, the supply given to the driver circuit is 12V with the help of a transformer. The 5V supplied by the ATMEL AT89S52 microcontroller is sensed by the buffer IC and proceeds to the IGBTs through the isolation IC 6NJ 36 which is otherwise known as optocoupler.

C. Power Circuit

A power circuit was fabricated using seven IGBT ICs CT60. The IGBT has advantages of both MOSFET and BJT with lower power and no secondary breakdown phenomenon.

The experimental set up of the inverter realized in the laboratory which is shown in figure 7.

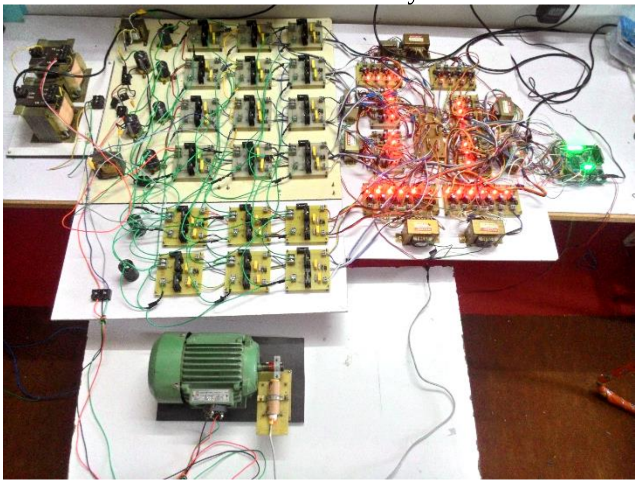


Figure.7. Experimental setup of Z source 7-level cascaded inverter

In figure 8, the output voltage of the proposed inverter is represented. From the figure, it is depicted that when the number of voltage levels is increased to seven, it achieves a more sinusoidal waveform.

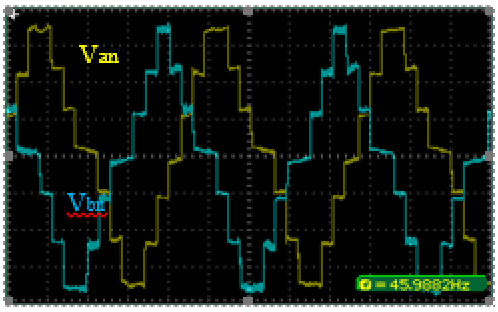


Figure.8a Output voltage response of proposed scheme (V_{an} and V_{bn})

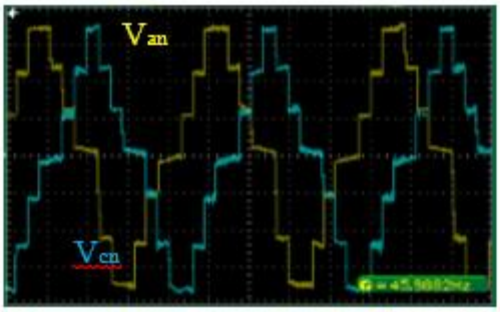


Figure.8b Output voltage response of proposed scheme (V_{an} and V_{bn})

The results obtained during non-shoot through mode is depicted in figure 9, and their corresponding inductor current and capacitor voltage is also displayed in Figures 10 and 11 respectively.

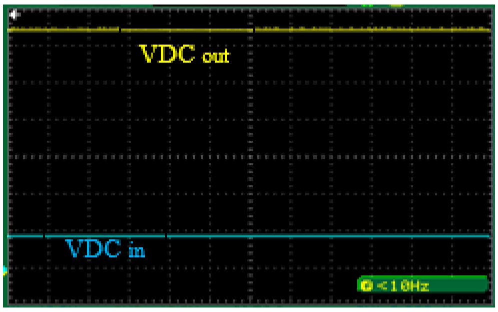
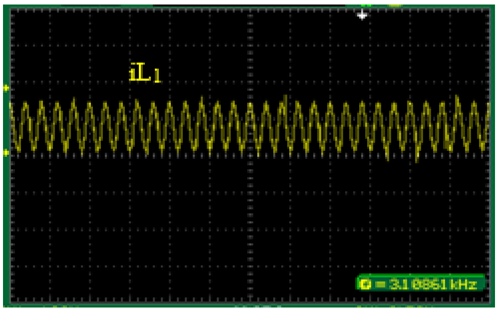
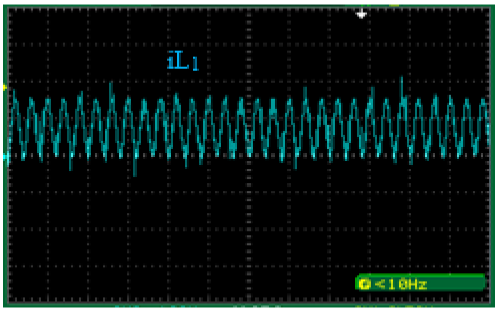


Figure 9. Input /output voltage (Z source network)



(a)i_{L1}



(b)i_{L2}

Figure 10. Inductor current (Z source network)

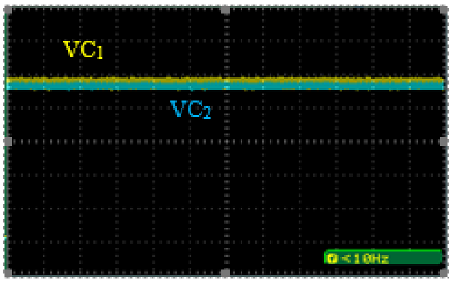


Figure.11. Capacitor voltage (Z source network)

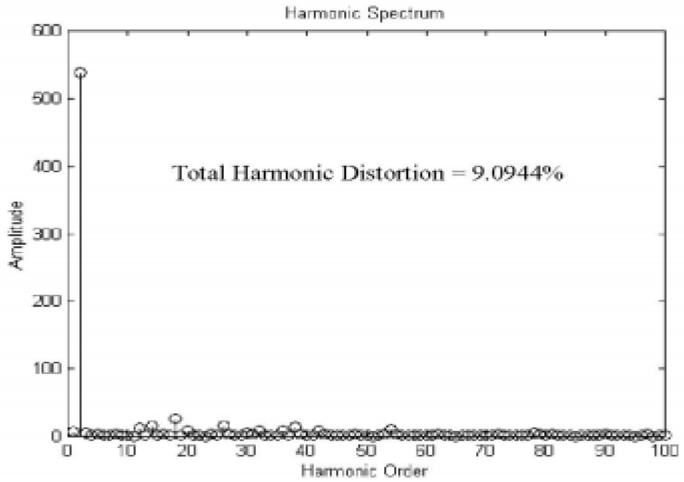


Figure 12. Total harmonic distortion of Z-source inverter

From the figure 12 , the THD is found to be 9.09%. From the figure, it is found that the proposed system is more efficient to reduce the THD level practically.

6. Conclusion

Multilevel Inverter (MLI) has been renowned as a most attractive technique for DC/AC conversion at high voltage applications. Thus the MLI's synthesize their desired voltage output from several levels of input DC sources. However, the major shortcomings of the MLI are its output voltage limitation by the input DC sources. To overcome this inadequacy of a conventional MLI, this work projected a novel seven-level cascaded multilevel inverter based Z-source inverter. In this proposed topology, a seven level cascaded multilevel inverter with Z impedance network is designed to regulate the induction motor and modified Space Vector Modulation (SVM) was stimulated to generate switching pulses to VSI. In the proposed scheme, the output voltage is boosted to the desired level using Z network under shoot-through (ST) state control. Apart from the boosted voltage, the proposed scheme has less THD, negligible commutation and passive element counts. With these advantages, it is proven that the projected topology can also be utilized renewable energy sources, EHEV vehicle control etc.,.

References

1. Nguyen M.K, Lim Y.C, Choi J.H, Two Switched Inductor Quasi Z-Source Inverters, IET Power Electronics. 2012; 5(7): 1017-1025.
2. Divya Subramanian, Rebiya Rasheed, Five Level cascaded H-Bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique, International Journal of Engineering and Innovative Technology, 2013; 3(1): 438- 441.
3. Dinakaran C, Panthee A.B, Eswaramma K, Modelling and Control of Quasi Z-Source Inverter for Advanced Power Conditioning of Renewable Energy Systems. International Journal of Advanced Research in Electrical, Electronics, and Instrumentation Engineering. 2014; 3(2): 136-141.
4. Farshad Khosravi., Naziha Ahmad Azli., Avin Kaykhosravi1., Design of a Reduced Component Count SinglePhase-to Three-Phase quasi Z-Source Converter, IET Power Electronics, 2014; 7(3): 489-495.
5. BOLDEA, I., ANTAL, R. & MUNTEAN, N. Modified Z-Source single-phase inverter with two switches. IEEE International Symposium on Industrial Electronics, 2008. ISIE 2008., June 30 2008-July 2 2008 2008. 257-263

6. F. Gao, P. C. Loh, D. Li, and F. Blaabjerg, "Asymmetrical and symmetrical embedded Z-source inverters," IET Power Electron., vol. 4, no. 2, pp. 181–193, Feb. 2011.
7. Chougule, G., Gaikwad, A., Simulation Study of Quasi Z-Source Inverter for Resistive and Inductive Load, International Journal of Innovations in Engineering Research and Technology, 2015; 2(6): 2-13
8. Rohitash Singh, Saurabh Kr. Bajpai, Harinder Singh Sandhu, Comparative Study of PWM Control and PI Control of Induction Motor, Bulletin of Electrical Engineering and Informatics (BEEI), 2015; 4(1): 53-58.
9. Sengolrajan T, Shanthi B, Arumugam M, Three Phase Trinary Source MLI Using Multicarrier SPWM Strategies, Indonesian Journal of Electrical Engineering and Computer Science (IJEECS), 2015; 13(3): 483-492.
10. Elakya, V.C., Aarthi., Teresa., V.V. High Performance Extended Switched Inductor Quasi Z-Source Inverter for Three Phase Loads, International Journal of Innovative Research in Science, Engineering and Technology, 2015; 4(4): 76-81
11. 10. Bhujangaro, Y., Bhavani, T., Implementation of Cascaded H-bridge Multilevel Inverter for Sinusoidal PWM Controller Fed Induction Motor Drive, International Journal of Advanced Technology and Innovative Research, 2016; 8(9): 1870-1876
12. . Gaddafi Sani Shehu., Abdullahi Bala Kunya., Ibrahim Haruna Shanono., A Review of Multilevel Inverter Topology and Control Techniques, Journal of Automation and Control Engineering, 2016; 4(3): 233-241
13. Himanshu., Rintu Khanna., Neelu Jain., A Survey on Various Topologies of Z-Source Inverters, International Journal of Electrical and Electronics Engineering, 2016; 3(7): 5-9.
14. Balamurugan, C.R, Natarajan, S.P, Bensraj, R, Shanthi, B, A Review on modulation Strategies of Multilevel Inverter, Indonesian Journal of Electrical Engineering and Computer Science (IJEECS), 2016; 3(3): 681 - 705.
15. Vijayalakshmi, K, Balamurugan, C.R, Z Source Multilevel Inverter Based on Embedded Controller, Indonesian Journal of Electrical Engineering and Computer Science (IJEECS), 2017; 6(1): 1-8.