Design and Implementation of low power Fault Tolerant Hybrid Full Swing Full Adder for Neural Network Applications

Devika K N[1], RajiC[2],Dr. S.N Prasad[3]

[1]School of Electronics and Communications Engineering, REVA University, India
[2]School of Electronics and Communications Engineering, REVA University, India
[3]School of Electronics and Communications Engineering, REVA University, India
[1]devikakn6@gmail.com, [2]raji.c@reva.edu.in , [3]prasadsn@reva.edu.in

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Abstract: Neural Networks (NN) are algorithms that can recognize relationships between data and can mimic the operation of the human brain. Some neurons are not fault free. Hence system that is fault tolerant is designed. Fault tolerance is one of the major factors that has to be considered while designing the VLSI circuit for critical applications. Implementation of a full adder using pass transistor logic has resulted in output degradation and CMOS logic has resulted in high power consumption. The fidelity of the sum output and carry output affects the fault tolerant capability of the full adder Hence the aim of this work is to design and implement hybrid low power full adder with full swing at carry out. The proposed full swing full adder will be used to implement fault tolerant Self Repairing full adder. Fault tolerant Self Repairing full adder helps to detect the fault in the circuit and resolve the single and double faults. For the proposed system, even though the number of transistors is increased by 4 for the Hybrid one bit full adder and 4 for the Self Repairing full adder, the output swing is maintained as per the requirement but the power consumed is reduced by 15.4% for Hybrid full adder and 27.4% for self-repairing full adder.

Keywords: HybridFullAdder,faulttolerance, SelfRepairingFullAdder

1. Introduction

Fault is defined as the physical defect present in the circuit. This leads to improper functionality of the system. In orderto avoid the damage, circuits are built that are fault tolerant in nature. This reduces the failures in the system but itimpossible to completely eradicate the fault from the systems. Neurons are not inherently fault free. In order to make asystem fault free, neuron that constitutes of adder and multiplier should be made fault free[1]. Larger number ofhardwarefaultsresultsintransientfaults.Itisaddressedusinganyoftheredundancyschemes:timeredundancy,spacere dundancy, or information redundancy[2] along with polling logics, with power, area and delay overhead.Manymethods are used for hardware fault detection and its recovery in digital circuits. To improve the yield of digital IC, theredundancyisusedtoachieveoptimizedarea.Dependingonthedurationthefaultmanifests,itcanbefurthercategorized as permanent, transient and intermittent faults.Transient faults contribute majorly to the hardware faultswhich may be due to alpha particles, Gaussian noise in channel, corrosion, electromigration etc. This paper presents theimplementation of 8-bit fault tolerant multiplier using the proposed full adder, mainly focusing on well-establishedcircuit to improve by design and to reduce the area and power. The proposed full swing full adder will be used toimplement fault tolerant Self Repairing full adder. Many approaches are available for Self Checking and Self Repairingfulladder.There are advantagesanddisadvantagesinall theapproaches.

2. Literaturereview

2.1 Redundancy

2.1.1 Timeredundancy

Self Checking full adder requires redundancy. Here the redundancy check is performed by the original modulealong with the duplicate module [3]. Delay clock is being introduced in order to establish the difference in time intervalfor the duplicate module. The two outputs obtained at the different time intervals is compared to determine the fault inthe systems. If the two outputs are same, then the system is fault free. If the two outputs are different, then there ispresence of fault. Since similar operations are performed at different time interval, this helps to reduce the cost of thedesignandarea.

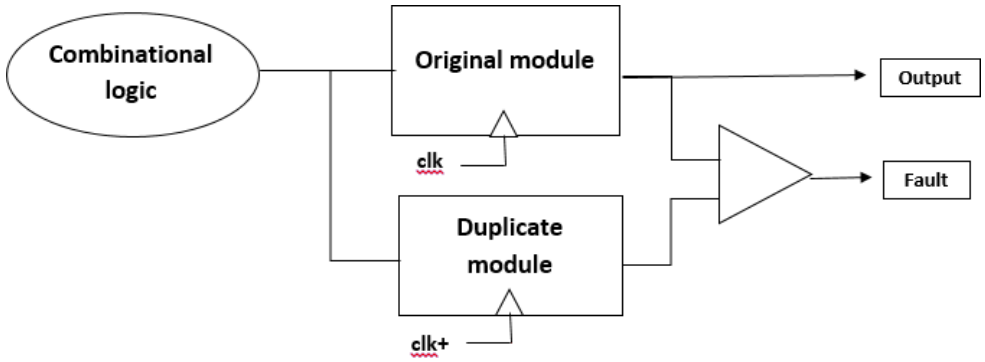

Figure1:TimeRedundancyfaultdetectiontechnique

2.1.2. HardwareRedundancy

In hardware redundancy, one or more duplicate circuit is used to produce outputs[3]. Here fault and fault freecondition are determined by comparing the outputs obtained from the original and duplicate hardware module thoughtheyperformsame operation.

2.1.3. Informationredundancy

This method could be used for detecting real time faults. Error detection codes, predicted parity bits could be usedfor fault detection in combinational logic. The major drawback of area overhead can be solved by using multiple paritygroups[3].

2.2 LowPowerFullAdderImplementations

The full adder described in [4],[5] uses 16 transistors is a very prospective design for the application proposed inthis paper as it has good output fidelity and has low power dissipation. It proposes GDI full swing method withoptimized powerdissipationandarea.

The 18-T full adder described in [6] exhibits full swing at sum output but not at the carry out.14 transistorimplementation in [8] usesmore than one style, and a hybrid pass transistor approach is adopted in [9]. Many lowpower adders that uses pass transistor logic, gate diffusion input and transmission gate [10] consumes larger power andresults in output degradation .The 10-T full adder described in [11-12] exhibits degradation of output levels at bothcarry and sum. Even the Gate Diffusion –Input (GDI) based adder which has very low power dissipation also have verylowoutputlevels.These
Designs
Lacks
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gcapabilities.Lowstaticpowerdissipationcanbeachievedthroughbranchbasedlogic andpass-transistorproposedin[13] uses23 transistors.

For any arithmetic, logical unit and neural networks adders and multipliers are the building Blocks.An Hybrid 20-TFull Adder that produces Full Swing at both the sum and Carry out is implemented in order to maintain the fidelity oftheoutput. Several Implementationsofone bitFullAdderaredone overyears[14-17].

3. Problemstatement

In the existing architectures [4][6], it is found that there is no full swing at the carry output which results in improperoutputfortheproposeddesign.Inordertoovercomethisproblem,aHybridFullAdderthatproducesfullswingatthecarry output with low power is implemented. The Self Repairing fault tolerant full adder is implemented using thishybrid fulladder.

4. Proposeddesigns

4.1 Proposed20-THybridfulladder

An adder is the basic module to construct the multiplier circuit. An adder performs the arithmetical and logicaloperations. A full adder is a adder that performs addition of 3 inputs which results in 2 outputs. It adds thefirst 2 inputs‘a’ and ‘b’ along with the third input ‘c’ to obtain the ‘sum’ and ‘cout’ outputs. The XNOR gate

and the 2:1 multiplexerare the building blocks in this full adder design. The multiplexer is used in the design to generate the 'cout' output. 2:1multiplexer isusedfor the followingreasons:

1. Itspeedsupthepropagationofcarry.
2. Itimprovestheoutputvoltageswing.

The full swing for carry out had been attained with 20T hybrid full adder. Hybrid full adders are built usingpass transistors and CMOS. The sum output is built using two 6 T XNOR gates and the carry output is built usingmultiplexerfollowed by buffer. The proposed full adder is used to design fault tolerant Self Repairing full adder thathas less power consumption. The expressions for the carry and sum outputs of the full adder is shown in equation (1)and (2)

sum=axnorb xnorcin..... (1)
cout=ab +bcin+cin..... (2)

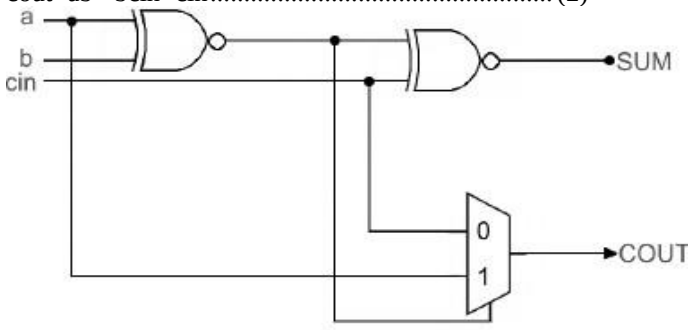

Figure2:ProposedHybrid20-TFullAdder

4.2 SelfCheckingfulladder

The Self Checking adder along with two MUX and two inverters are used to implement the Self Repairingadder circuit. The proposed Self Checking full adder is used for detection of the faults with an exact location indication.The 'sum' and 'cout' are checked individually to detect the fault. The equivalent functional unit and xnor gates are usedto identifythefaultatthecarryoutput. To detectthe faultatthe cout,Fc canbe computedas

G1=(coutxnorcin).....(3)
F1=(a'b'c+abc').....(4)
Fc=(G1xnorF1).....(5)
Todetectthefaultatthesum Fs,canbecomputed as
G2=(axnorb)'.....(6)
G3=(sumxnorcin)'.....(7)
Fs=(G2xnorG3)'.....(8)

Forfaultfreecondition,Fs=1,andFc=0.Thecomplementaryvaluesofthesesignalswillindicatefaultycondition.Fault locationcanbedetermined bythevalueofthesetwo outputs.Bothsingleand doublefaultscanbedetected.

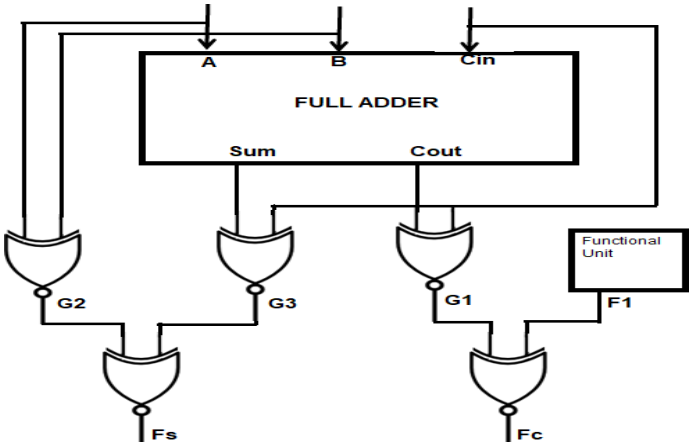

Figure3 :BlockDiagramofSelfCheckingFull Adder

4.3 SelfRepairingfulladder

The proposed Self Repairing full adder design is used for repair the faults that is detected in the Self Checkingfull adder. The fault tolerant Self Repairing full adder should have the ability to resolve fault permanently and make theadder faultfree.

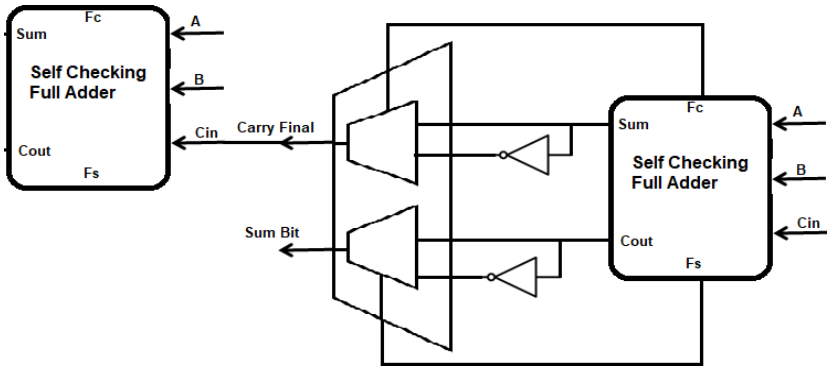

Figure4:BlockDiagramofSelfRepairing FullAdder.

5. Implementation

Thedesignisimplementedusing usingtheCadenceVirtuosoToolofgpdk45nmtechnologynode.

5.1 Proposed20T1-BitHybridFullAdder

The Hybrid full adder is implemented using 20T as shown in below figure 5. There are two 6T XNOR gates andone 2x1 Mux followed by buffer. Transmission gate is used as 2:1 multiplexer. Multiplexer followed by buffer givescarryoutputwithfullswing.

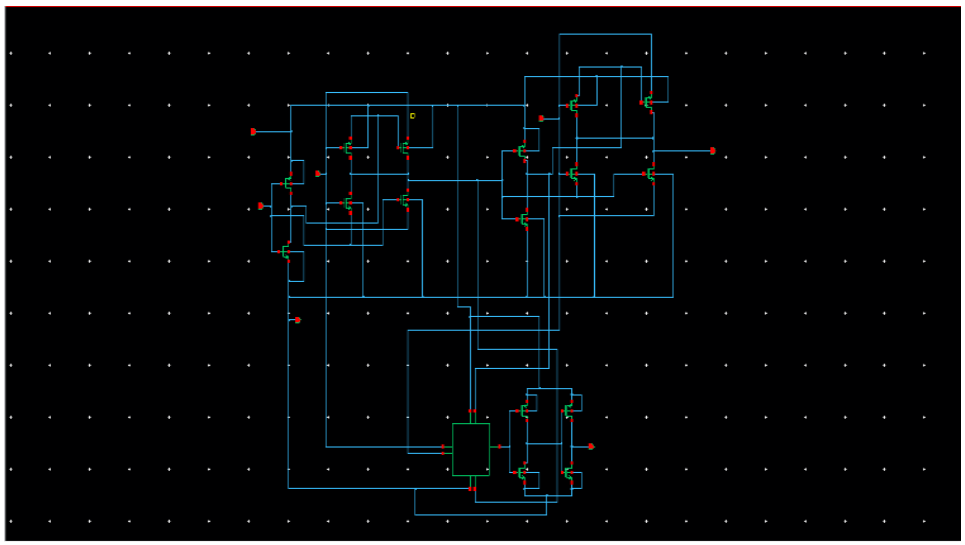

Figure5:SchematicofHybrid20TFullAdder

5.2 SelfCheckingFullAdder

It is built using one 20 transistor full adder, five XNOR gates (6 transistor) and a functional unit implemented using14 transistorsisshown infigure6.Thetotalnumberoftransistorsused inthisimplementationis64.

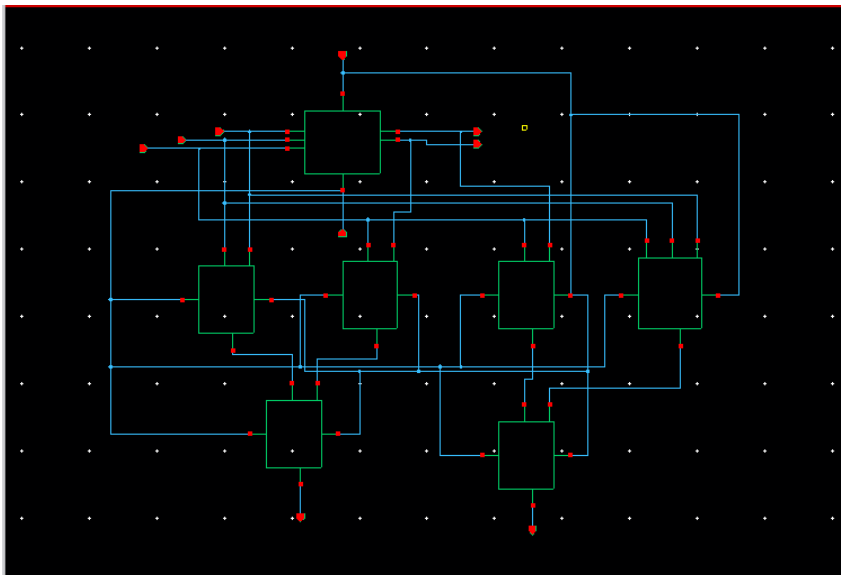

Figure6:SchematicofSelfCheckingFull Adder

5.3 SelfRepairingFullAdder

If fault occurs, it is corrected using multiplexer for both carry and sum outputs from the Self Checking process. TheSelf Checking adder along with two MUX and two inverters are used to implement the self-repairing adder circuit asshown infigure 7.The total transistorcountfor thisdesignis80.

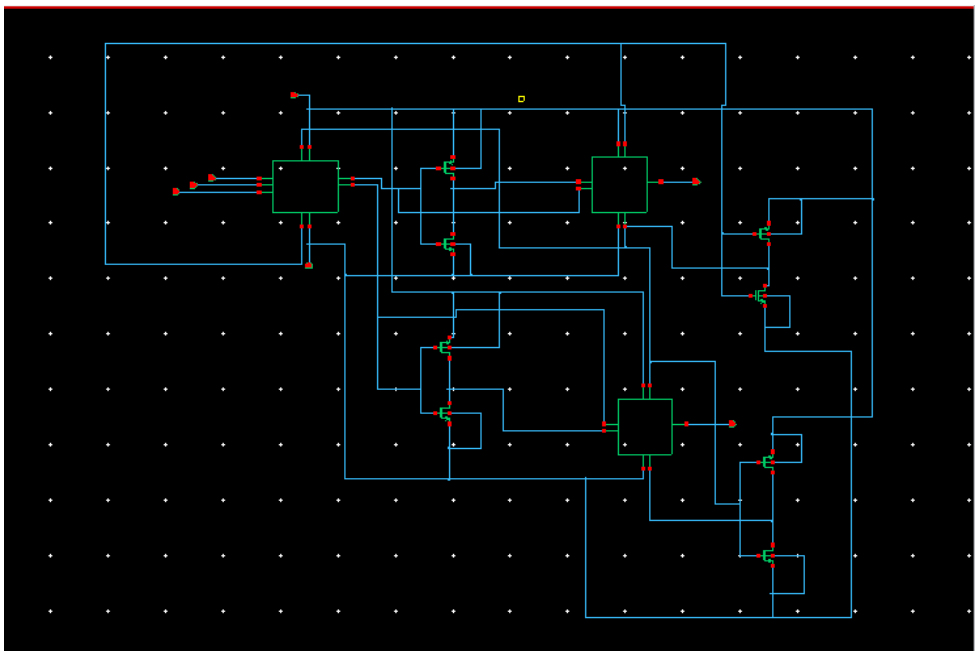

Figure7:SchematicofSelfRepairingFull Adder

6. Resultandwaveform

6.1 Proposed20T1-BitHybridFullAdder

The proposed design was designed in 45nm gpdk technology node and simulation is done using spectrecadence simulator. the size of pmos is twice that of nmos to get better delay and power performance (wp/l = 240/45,wn/l = 120/45). The supply voltage is kept at 1V andfrequency is maintained at 100MHz. figure 12 shows thesimulation result of hybrid full adder which includes xnor gates and 2:1 mux of 20 transistors. The full swing operationisobtainedfor bothsumand carryoutputsat 1V eachrespectively.

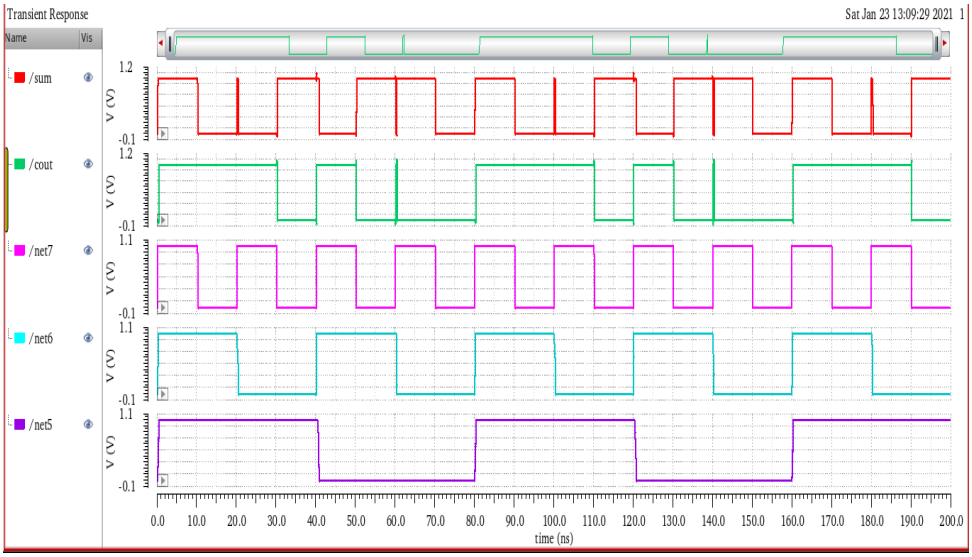

Figure8:SimulationResultofHybridFull Adder

6.2 SelfCheckingfulladder

Since there are no faults introduced during simulation of self-checking full adder, signal Fs=1 and signal Fc=0 as showninfigure 9.

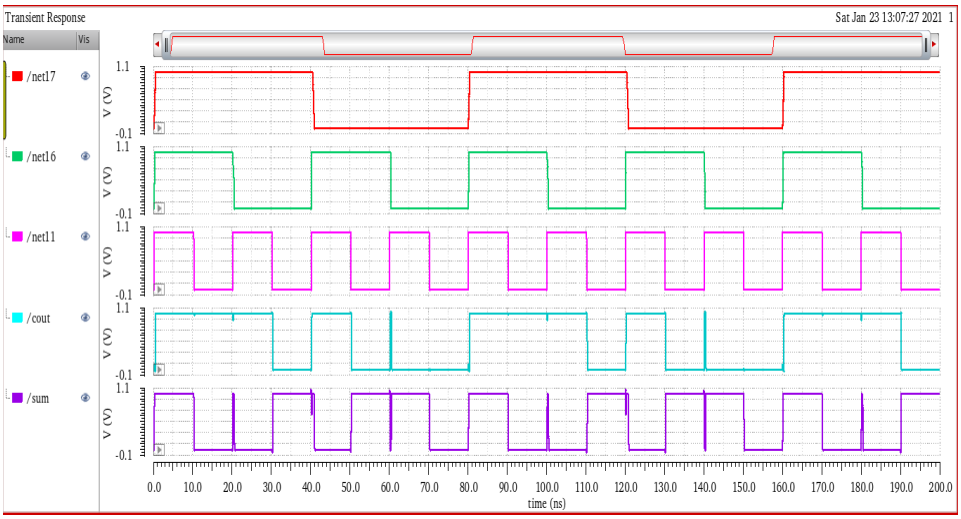

Figure9:SimulationResultofSelfChecking fulladder

6.3 SelfRepairingfulladder

Thefaultsoccurrediscorrectedusing multiplexerforbothcarryandsumoutputsfromtheSelfChecking process**.**

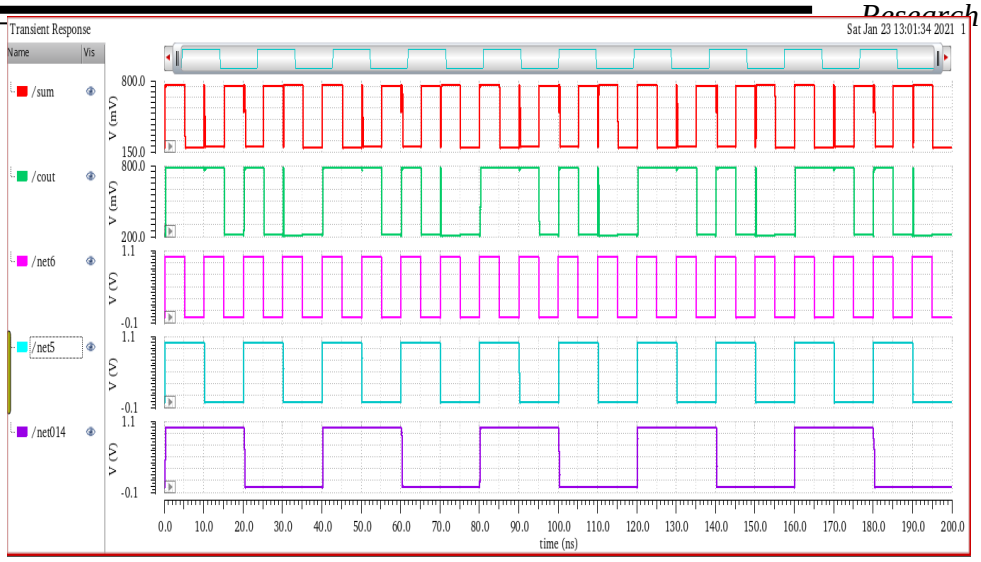

Figure10:SimulationResult of SelfRepairingfulladder

7. Comparisons

The various designs are compared in terms of the number of gates used and the total number of transistors used forimplementing the designs as shown in Table 1. It is evident that the design proposed in this paper has a clear advantageonthe total numberoftransistorsused. Comparisonofpower isgiveninTable 2.

Table1:Comparisonofnumber oftransistorsused

DesignName	List of gates	Numberofgates	Numberoftransistors used	Total
Self repairing	Fulladder	1	28	138
	XNOR	5	60	
	Functionalunit	1	28	
	NOT	2	4	
	MUX	2	20	
Selfrepairingfulladder [6]	Fulladder	1	16	76
	XNOR	5	30	
	Functional unit	1	14	
	NOT	4	8	
	MUX	2	8	
Selfrepairingfulladder [7]	Fulladder	1	114	138
	NOT	2	4	
	MUX	2	20	
Selfrepairingfulladder (GDI)[3]	Fulladder	1	18	96
	XNOR	5	40	
	Functionalunit	1	22	
	NOT	2	4	
	MUX	2	12	
Selfrepairingfulladder (Proposeddesign)	Fulladder	1	20	80
	XNOR	5	30	
	Functionalunit	1	14	
	NOT	4	8	
	MUX	2	8	

Table2:ComparisonofPower

DesignName	No:oftransistor	Powerdissipation	Technologynode
Existingfull adderDesign [6]	16	59.01nW	45nm
Existing FullAdder(GDI) Design[7]	18	693.5nW	65nm
Existing Selfrepairing fulladderDesign[6]	76	97.803uW	45nm
Proposed HybridfulladderDesign	20	49.994nW	45nm
Proposed SelfRepair AdderDesign	80	70.683uW	45nm

8. Conclusion

Even if Neural Network is considered asfault tolerant, they are not inherently fault tolerant. Implementation of faultfree Self Repairing full adder can result in aneural network architecture that is faultfree. The proposed full adderdesign with Self Repairing capability can identify and repair single fault and double fault at the same time. The aim offault-tolerant circuit isto reduce the probability of failures. The desired outputwaveforms are obtained, hence thedesign can be further extended for neural network applications. The area and power consumption. Is reduced using theabove design methodology. The transient faults occurring in critical applications which are crucial are solved by thisproposed method. The total power consumed by the Hybrid Full Adder is 49.994nW and Self Repairing Full Adder is70.683uW. The above comparison shows that the power consumption of proposed method is much more reducedcompared to the existing method. A Hybrid 1-bit Full adder is designed with 15.4% decrease in the power consumptionand Self Repairing full adder by 27.4% compared to existing Full Adder[4] even though the number of transistor isincreased by 4. Though thenumber of transistors used in proposed system is more than the existing design[4], thepower consumption is reduced comparatively. The degraded carry output[4] at the full adder end is propagated to thecarry out of Self Checking full adder which results in high degraded output. This disadvantage of degraded output inpaper [4]hasbeen mitigated.Thecarryoutand sumoutputofproposed fulladdersarebothareat 1V.

9. Futurescope

Multipliers can be implemented using Proposed Self-Repairing adders. This can reduce the hardware redundancy that is usedin rail checking circuits which can be used in conventional fault tolerant mechanism. Implementation of 8-bit Multipliersusingaddersresultsinpower reductionthatcanbe used inlowpower neuralnetworkautomotiveapplications.

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