

Performance Analysis of UPFC Embedded with Five Level Cascaded H Bridge Inverter with SPM and SVM Techniques and ANN Controller

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Abstract: Experimentation procedures in the design of Advanced Controllers for stabilizing the power system operation has gained great importance as the complexity of the power system network is increasing at a rapid pace. Dependence on microcontroller based controllers is slowly taken over by the application of artificial intelligent and meta-heuristic technique applications and the conventional 6/12/24/36/48 level transformer based converters are getting replaced by the multilevel inverters. Also the procedures adopted for generating the sinusoidal voltage waves i.e., with the help of the PWM techniques, at the output terminals of the MLIs has gained utmost importance. The methods adopted are chosen in such a way that the output to input voltage ratio produced by the inverter is more, the application is more compatible to a variety of multilevel systems and computer programmable, involves in the reduction of harmonic levels , i.e., less THD. More importantly the MLIs used must have faster response rate, must withstand high power ratings and must be robust and the PWM technique adopted must allow for flexibility in the output voltage wave with reference to the controllability of magnitude and its corresponding phase angle. This paper emphasizes on the importance of the use of the sinusoidal pwm (SPM) technique and the space vector pwm (SVM) technique. The multilevel inverter used is a 5 level Cascaded H Bridge Inverter. It also emphasizes on the application of an ANN technique used for controlling the different electrical parameters in the electrical network used. To observe the relative performance capabilities of an SPM based and an SVM based UPFC, controlled by an ANN controller, an IEEE 5 bus system is chosen. The Performance improvement of the novel UPFC (incorporating an ANN Controller, a 5 level CHB Inverter and SPM , SVM techniques), with reference to the Transient Stability and Dynamic stability enhancement is analysed. This aspect is shown by calculating the times like settling time for the transient power wave in the cases of faults like LG and LLL and also even when the loads are changed from normal to highly Inductive and highly capacitive. The ANN Controller based UPFC helps the Power System Network to restore normalcy in a less time when the space vector pwm technique is used than when the sine triangle pwm technique is used. To test this aspect the UPFC is connected to the IEEE 5 bus system between the buses 3 and 4. The faults LG and LLL are created near bus 4 in the line 3-4 and the load variations are done at bus number 4. The Simulations are carried out using MATLAB Software.

Keywords – AC Transmission, FACTS, UPFC, IEEE-5 BUS System, Shunt Line Faults, Power Flow Control, Cascaded H Bridge (CHB) Inverters, SPM, SVM, ANFIS Controllers, Rise Time, Settling Time.

I. INTRODUCTION

The Unified Power Flow Controllers were basically proposed for real time control and dynamic compensation of the ac transmission system parameters and for obtaining more flexibility in solving the problems faced by the utilities. An earnest effort towards achieving the above goals is made here especially to improve the sensitivity of the device, the quality of output of the device, the response time of the device and also the controllability of the device by making the device to act like a self thinking machine. The Unified Power Flow Controller has two converters, one a shunt converter (converter 1), connected in shunt with the transmission network and other a series converter (converter 2), connected in series with the Transmission Network. These two converters are connected to each other by a common DC link capacitor. The presence of a common DC link enables the transfer of real and reactive power to flow between the two converters thereby enabling the absorption and injection of voltages and currents from and to the transmission network respectively. Each of the converters can independently generate and absorb real and reactive power at their respective ac terminals. The basic function of the Shunt converter (converter 1) is to supply the real power it can also supply or absorb reactive power. The series converter (Converter 2) provides the main function of the UPFC by injecting an ac voltage of requisite magnitude V_{pq} ($0 \leq V_{pq} \leq V_{pqmax}$) and phase angle δ ($0 \leq \delta \leq \delta_{max}$) at power frequency in series with the transmission line voltage. The idea of the work is test the capabilities of a UPFC when it is using a 5 level Cascaded H Bridge Inverter , sinusoidal pulse width

modulation technique and space vector pwm techniques. The results are explained in terms of the settling times of the power wave in the line to which the UPFC is connected. For this a standard IEEE bus is chosen. The UPFC is proposed to be connected in the line 3-4. This line is said to be the line carrying maximum power in the entire network. Therefore any kind of a disturbance in this line will create huge power oscillations. Protection of the transmission system and restoration of normalcy in a minimum possible time after the clearance of a fault or disturbance is a challenging task.

Terminal Voltage Regulation is done with UPFCs wherein the required voltage of change required on the Transmission line say, ΔV (V_{inj}), is injected either in-phase or in anti-phase mode with the existing voltage V_o on the Transmission line.

Series Capacitive Compensation is done where the required value of voltage say, V_{inj} , is injected in Quadrature with the Line Current.

Phase Shifting or Transmission Angle Regulation is done by injecting a voltage of V_{inj} in an angular relationship with V_o to get the required Phase Shift (Advanced or Retarded) in the Line output voltage without change in the Magnitude of the Line output voltage.

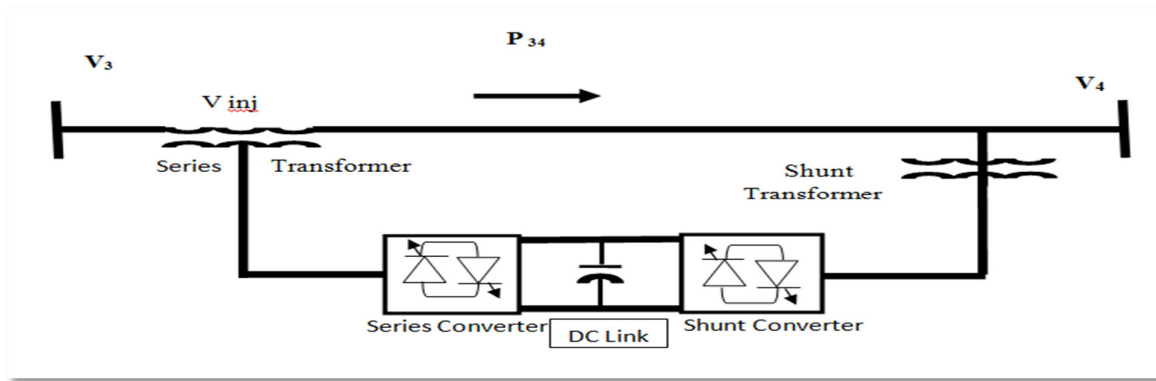


Fig.1. Line diagram of Five Level CHB Based UPFC for IEEE-5 Bus system connected in the line 3-4

Figure 1 shows the line diagram of the 5 level CHB inverter based UPFC connected in the line 3-4 of the IEEE 5 bus system. The shunt converter is connected towards the 4th bus and the series converter near the 3rd bus. All the test conditions viz., shunt faults and over loading conditions are executed near bus number 4, being the heavily loaded bus.

The following formulae is used to execute the solution technique [1]

$$P = \frac{V_3 V_4}{X_{34}} \sin \delta_{34} \quad (1)$$

In the explanation that follows, the importance of using the ANN Controllers, 5 level CHB Inverter, SVM technique, in UPFC to enhance the controlling capabilities of UPFC are clearly explained. The UPFC is connected in the system between bus number 3 and 4. The test conditions include (i) under voltage compensation (created by adding an additional 100MVAR inductive load), (ii) over voltage compensation (due to light load conditions or due to capacitive overloading created by adding an additional capacitive load of 100MVAR capacitive) (iii) transient stability enhancement capabilities when the IEEE-5 Bus system is subjected to different Shunt Faults like LG and LLL Faults at Bus No. 4. The immediate changes in the network conditions, more importantly, at the point of connection of the UPFC are detected and appropriate corrective actions are initiated by the ANN Controllers. The advantage with the CHB Inverters is made use of in improvising the Performance of the UPFC there by improving the protection levels offered to the Power System Network when the Power System is subjected to Certain Adverse and Abnormal Conditions. One of the most widely used software MATLAB is used for simulating the said test conditions.

II. THE 5 LEVEL CASCADED H BRIDGE INVERTER

One of the outcomes of the Research on the attempt to improvising the Output Voltage of an Inverter through Modifying Network/Circuit configurations of an Inverter is the Cascaded H Bridge (CHB) Inverter. The low switching voltage stress and modularity has made the Multi Level Inverters (MLIs) gain more attention. The user desired MultiLevel voltage is obtained by using different and separate voltage sources like Batteries, Fuel cells, Solar Photo Voltaic (PV) Cells, Capacitors etc., The major Advantages with Multi Level Inverters are their Minimum Harmonic Distortions in the Output Voltage, Low Electro Magnetic Emissions, High Output to Input Ratios i.e., High Efficiency and More Importantly their High Voltage Withstanding and Operating Capability and Modularity. The MultiLevel Inverters have found great applications in the areas of Drive Controls, Uninterruptible Power Supplies and Static Volt Ampere Reactive Generators (SVG). In general MLIs are divided in to three categories as Diode Clamped, Flying Capacitor and Cascaded Bridge Inverters. One of the advantages of MLIs over the Two Level Inverter is that they reduce the Common Mode Voltage causing the breaking leakage Current in Multi Drive Systems of High Power Ratings (Greater Than 250KW) based Vehicles.

The Circuit Topology of Cascaded H Bridge Inverter

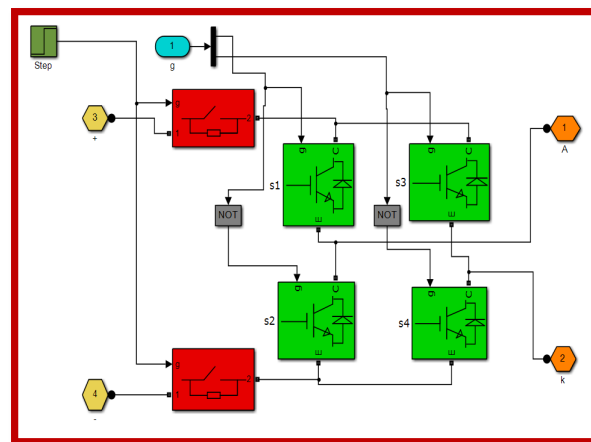


Fig.2. Basic Circuit of a CHB Inverter used in this Simulation

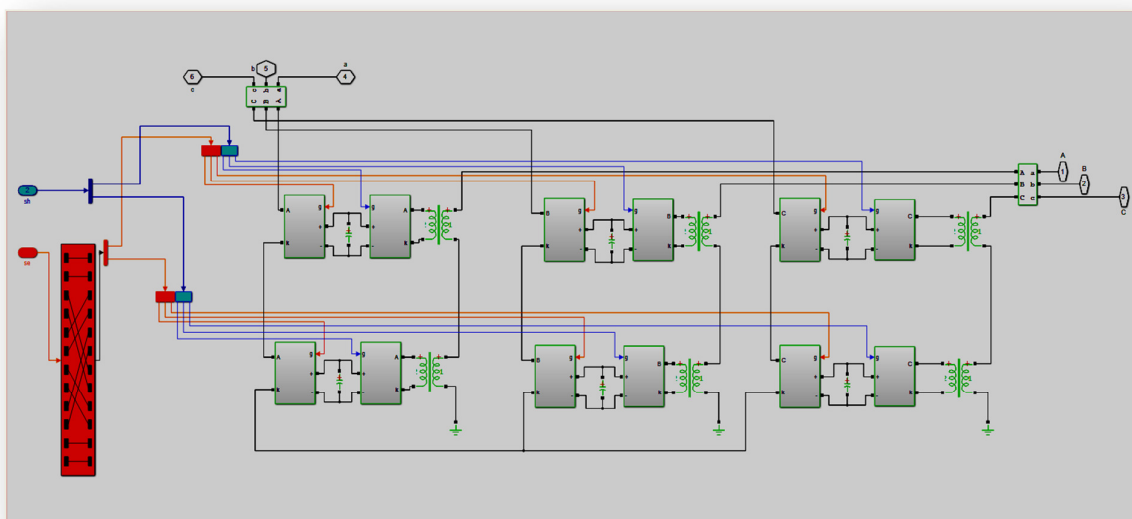


Fig.3. The 5 Level Cascaded H Bridge Inverter used in this Simulation

Figure 3 shown above details the connections of the shunt and the series converters used in the UPFC converters. In each of the phase 5 level Cascaded H Bridge Inverters are connected It can be observed that the series and the shunt converters are connected back to back by a strong DC link. The converters can be seen to be connected to the transmission line via their respective isolation transformers. Gate pulses generated using the SPM technique and SVM technique are given to the two converters according to the requirement. Gate pulse connections to the series converter are indicated using red cable and to the shunt converter using blue colour cable.

The equations of the CHB Inverters are written below

The generalized equation for an n level CHB Inverter (for one phase)

$$V_a = V_{a1} + V_{a2} + V_{a3} + \dots + V_{an} \quad (2)$$

Where

$V_a = V_{a1} + V_{a2} + V_{a3} + \dots + V_{an}$ are the voltages of each of the levels of the CHB inverter .

The Fourier series equation of the output vector wave of the CHB inverter

$V_a(\omega t)$ is given by

$$V_a(\omega t) = \left(\frac{4 V_{dc}}{2\pi} \sum_{n=1,2,3,\dots}^{\infty} \frac{1}{n} (\cos n\theta_1 + \cos n\theta_2 + \cos n\theta_3 + \dots \cos n\theta_n) \sin n\varphi \right) \quad (3)$$

Where

V_{dc} is the value of the DC input given to the inverter

n is the Harmonic number

$\theta_1, \theta_2, \theta_3, \dots, \theta_n$ are the reference switching angles for each of the levels

$\varphi = \omega t = 2 * \pi * f * t$

$f = 50 \text{ Hz}$

For a 5 level CHB Inverter the output voltage is given by

$$V_a(\omega t) = \left(\frac{4 V_{dc}}{2\pi} \sum_{n=1,2,3,\dots}^{\infty} \frac{1}{n} (\cos n\theta_1 + \cos n\theta_2) \sin n\varphi \right) \quad (4)$$

The Modulation Index is given by

$$m = \frac{V_{a1}}{\frac{4 V_{dc}}{2\pi}} \quad (5)$$

It can be seen from the equations numbered from 1 till 5, that as the level of the CHB Inverters increases the output changes i.e., the magnitude increases also the percentage closeness of the shape of inverter AC wave to the reference sinusoidal wave will be more.

IV. THE PWM TECHNIQUES

The commonly used modulation schemes for multilevel inverters are the carrier-based sinusoidal pulse-width modulation (SPWM) and the space vector modulation (SVM) schemes. SPWM schemes are easier to implement and provide almost the same results as far as total harmonic distortion (THD) in the output is concerned. However, from the perspective of obtaining a more Fundamental Output Waveform and Digital Implementation, the SVM scheme as compared with SPM, provides flexibility in optimising the switching pattern design. For this reason most of the industrial applications prefer the SVM schema.

IV (a) The SPM technique

The sinusoidal pulse width modulation techniques as applied to the UPFC converters is explained in the following section

The figures 4(a) and (b) depicted below are the blocks designed to implement the sinusoidal pwm technique required for the 3 level Cascaded H Bridge Inverter.

The fundamental principle used for the SPWM technique is derived from the following equations

V^{ctrl} = The reference sine voltage or the control voltage magnitude

Defined as

$$V^{ctrl} = (V_{ctrl}) * \sin(\omega t) \quad (6)$$

V_{tr} = The Triangular Carrier Wave, shown as CW in fig. 4(b)

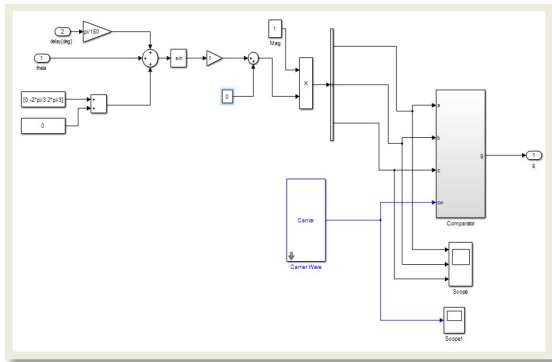


Fig.4 (a). The Sinusoidal PWM Block

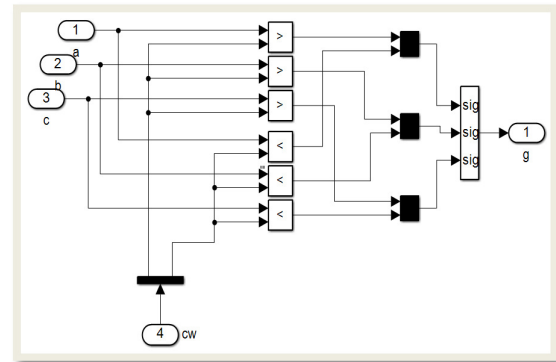


Fig.4 (b). The Comparator of the Sinusoidal PWM Technique Block

The modulation index value is given by

$$m = (V_{ctrl}) * \sin(\omega t) / V_{tr} \quad (7)$$

where $0 \leq m \leq 1$

The value of the fundamental component of the output voltage of the spwm technique is governed by the relation

$$V_{o1} = m * \left(\frac{V_{dc}}{2} \right) \quad (8)$$

Where V_{dc} is the value of the dc capacitor voltage the inverter input

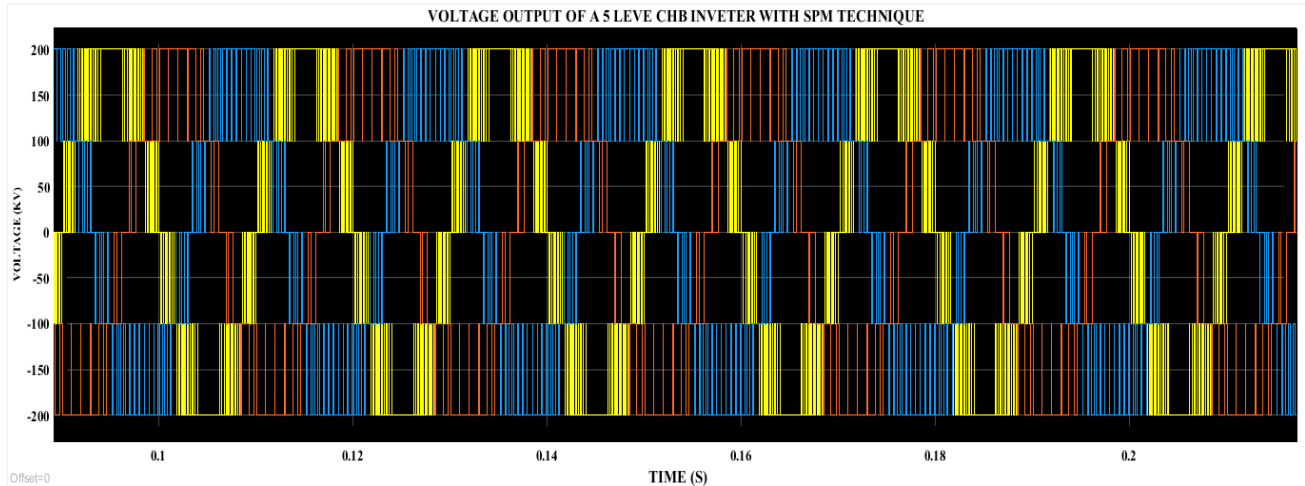


Figure 5. Three Phase Voltage Output of the 5 level CHB Inverter using the SPM technique

IV (b) The SVM Technique

The Space Vector Pulse Width Modulation Technique implemented is explained here

The 5 level CHB Inverter has 5 possible output voltage levels for each phase, ranging from $+2E$ to $-2E$, resulting in $5^3 = 125$ possible space vectors for the inverter.

Out of these, the number of independent or fundamental space vectors is

$$(3n^2 - 3n + 1) = ((3 \cdot 25) - (3 \cdot 5) + 1) = 61 ;$$

where $n = 5$ for a 5-level inverter.

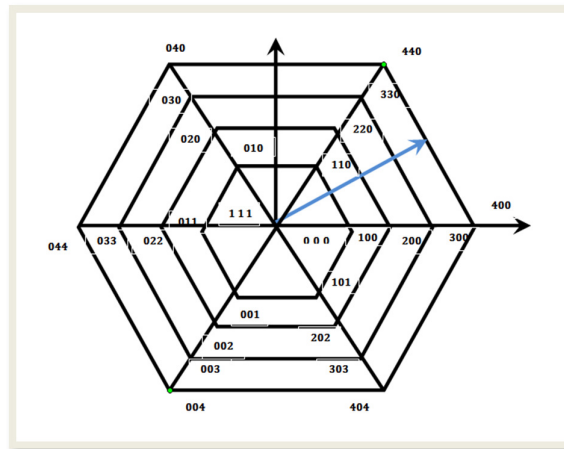


Fig.6(a) Switching States of 5 Level Cascaded H Bridge Inverter with Equal Voltages using SVM Technique

Figure 6(a) above indicates the switching states of the 5 level Cascaded H Bridge inverter using the SVM technique. The switching states depend upon the location of the voltage vector in the specific sector where Sector I ranges from 0° to 60° , Sector II ranges from 60° to 120° , Sector III ranges from 120° to 180° , Sector IV ranges from 180° to 240° , Sector V ranges from 240° to 360° .

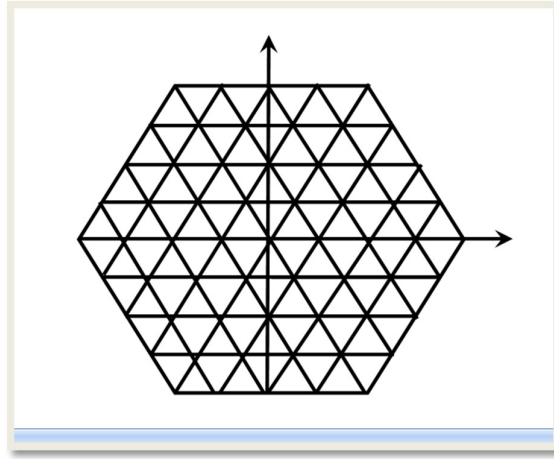


Fig.6(b) Sectorization of the switching states of 5 Level Cascaded H Bridge Inverter with Equal Voltages using SVM Technique

There are $(n - 1) = (5-1) = 4$ layers and

$(n - 1)^3 = (5-1)^3 = 64$ triangles in the Space Vector Diagram shown in the above figure 6(b)

“Depending upon the Requirement of output given by the Comparator in the Controller of the UPFC the SVM selects the Sector of the Voltage to be generated say **Vref** in which the required voltage lies and Pulses are generated accordingly.

The widths of the pulses are given by the following Volt – Second balance equations for one sector is given by

$$V_{ref} * T_s = V_1 T_a + V_2 T_b + V_0 T_0 \quad (9)$$

Where T_s is the sampling interval; and T_a, T_b, T_0 are the respective dwell times for the vectors V_1, V_2 and V_0 .

The values of T_a, T_b and T_0 are given in [2] “re written here

$$T_a = T_s * m * \sin(60 - \theta_2)$$

$$T_b = T_s * m * \sin(\theta_2)$$

$$T_0 = T_s - T_a - T_b$$

$$m = (\sqrt{3} * V_{ref})/E \quad (10)$$

The Series Injection Transformer is designed to a Transformation ratio of 1:1. Therefore the value of V_{out} of the CHB Inverter will be equal to the value of voltage injected in series with the line, V_{inj}

Therefore

$$V_{ref} = V_{inj} = V_{out} \quad (11)$$

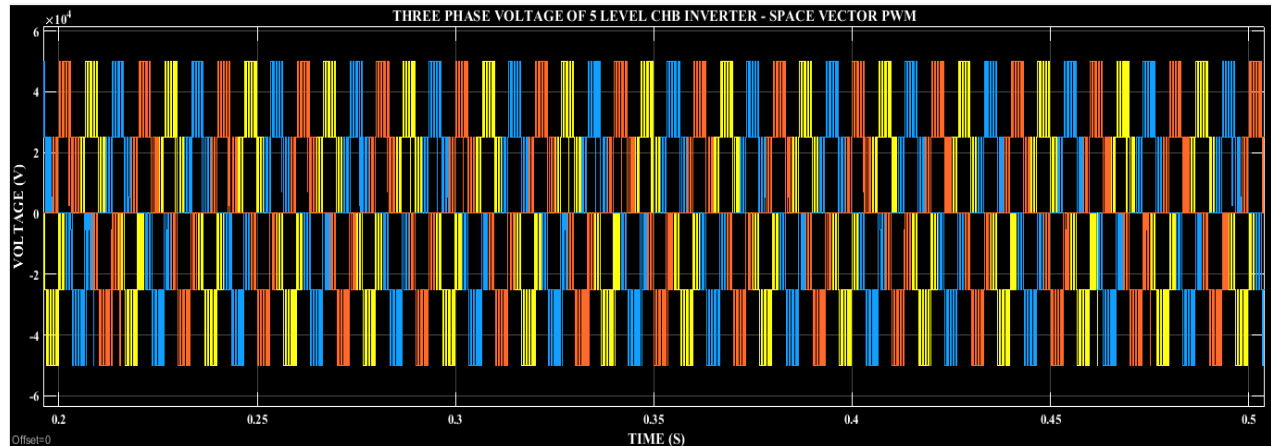


Figure 7 Three Phase Voltage output of the 5 level CHB Inverter using SVM technique

Figure 7 shows the three phase output of the 5 level CHB inverter when the space vector pulse width modulation technique is used. The average value of the output is more when compared to the output given by the inverter when SPM technique is used.

V. THE CENTRAL CONTROL SYSTEM

The following figure numbered 6 details the entire control structure of the UPFC. The control structure comprises of the shunt controller controlling the DC voltage at the capacitors terminals connecting the two converters. The central controllers also has a series controller used for producing the voltage to be injected in series with the line 3-4 for balancing the voltage and also for controlling the power travelling through the line. Both the shunt and series controllers are equipped with the Artificial Neural Network (ANN) controllers which operate individually. The central control system is also included with pwm technique implementation blocks individually for the shunt and the series controllers for generating the source synchronized pwm pulse trains for the 5 level Cascaded H Bridge Inverters. Initially the SPWM technique is used and then it is replaced by the SVM technique for comparing the UPFC's performance.

V (a) . THE ARTIFICIAL NEURAL NETWORK (ANN) CONTROLLER(S)

The Artificial Neural Network controller of the shunt converter takes into consideration the voltage and current conditions on the line 3-4 and the dc voltage across the capacitors at the dc link between the two converters. The inputs also include the reference voltages to be maintained on the line 3-4 where the UPFC is connected and where the test conditions are executed. As soon as the test conditions are initiated the error value (reference value – measured value) is processed for sterilization and range testing. This error is fed to the ANN system where proper weights and bias are calculated and are added in layer 1 and layer 2, shown in figure 6(b), to process the output using the tansig transfer function method. The output is properly processed through the PID controller system and discretized to get the value of angle in degrees. This angle is input to the control system and pulse generator block, shown in figure 7, wherein the process of producing the firing pulses is executed. A sinusoidal wave with the reference angle specified by block 7 is generated and is compared with a triangular wave in case of SPWM technique and the reference angle is used to produce a pulse train for 5 level Cascaded H Bridge Inverter. For the case of the SVM technique a program is written using the MATLAB function block which coordinates with the other Simulink blocks.

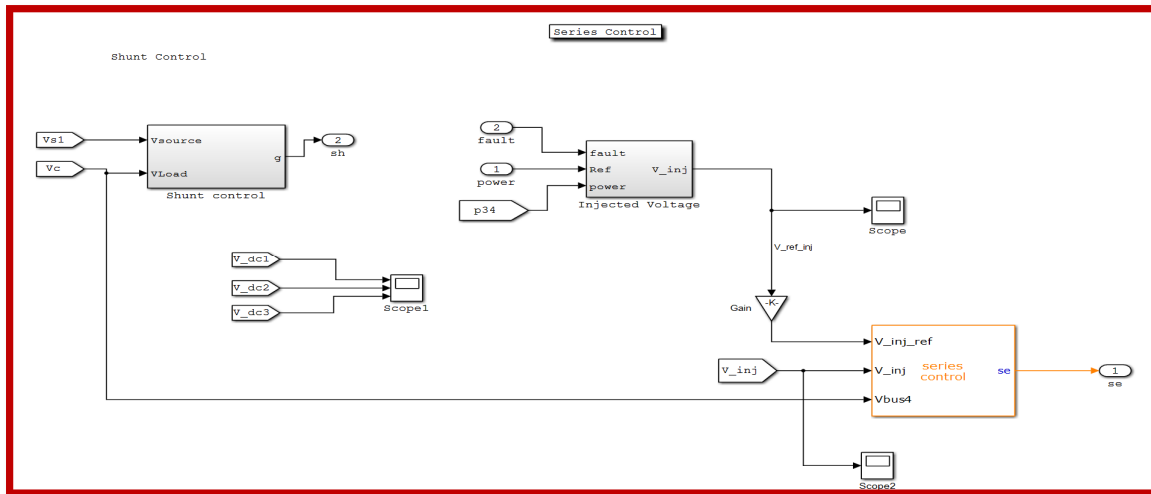


Fig.6. The Central Control System Comprising of the Series and Shunt Controllers where the SPM and the SVM blocks are incorporated. It also has the Pulse Generator block

The operation of ANN in the series converter controller will be on similar line to the ANN controller in the shunt system but with a difference that the series control system takes input the reference power values and continuously measured values of power on the line 3-4. The comparators in the series controller calculate the error and processes through the double layer 1 and layer 2 of the ANN system, to control the value of direct injected to be produced by the series controller by way of producing appropriate firing angle control technique.

The weight adjustments in the ANN controller in layer 1 are done using the following equations

The weight function for an input x

$$Wfcn(x) = (w1 * x1 + w2 * x2 + w3 * x3 + \dots + wn * xn) \quad (11)$$

for an n numbered input system

A proper bias is added depending upon the requirement

$$x' = Wfcn(x) + bias \quad (12)$$

The tansig function used

$$F_{\text{tansig}} = \frac{\text{Gain}}{e^{-2x'} + 1} - \text{constant} \quad (13)$$

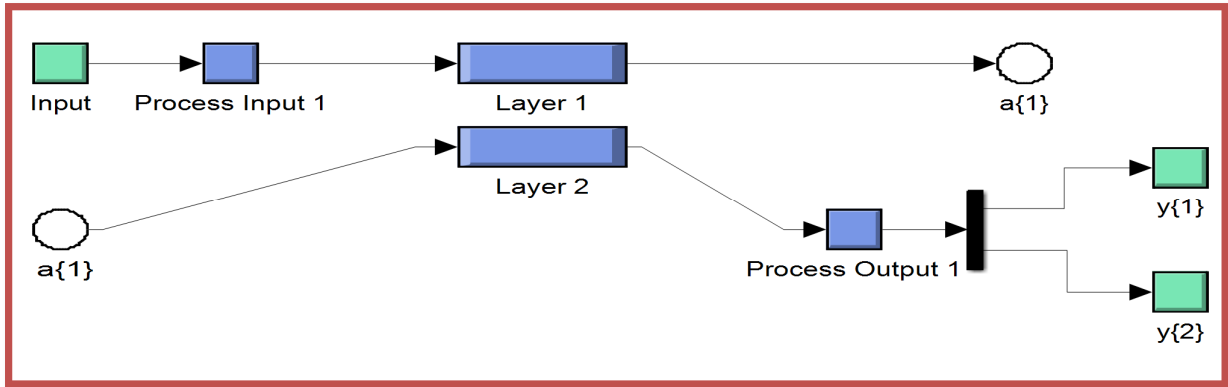


Fig.7 (a).The layer structure of the ANN Controller

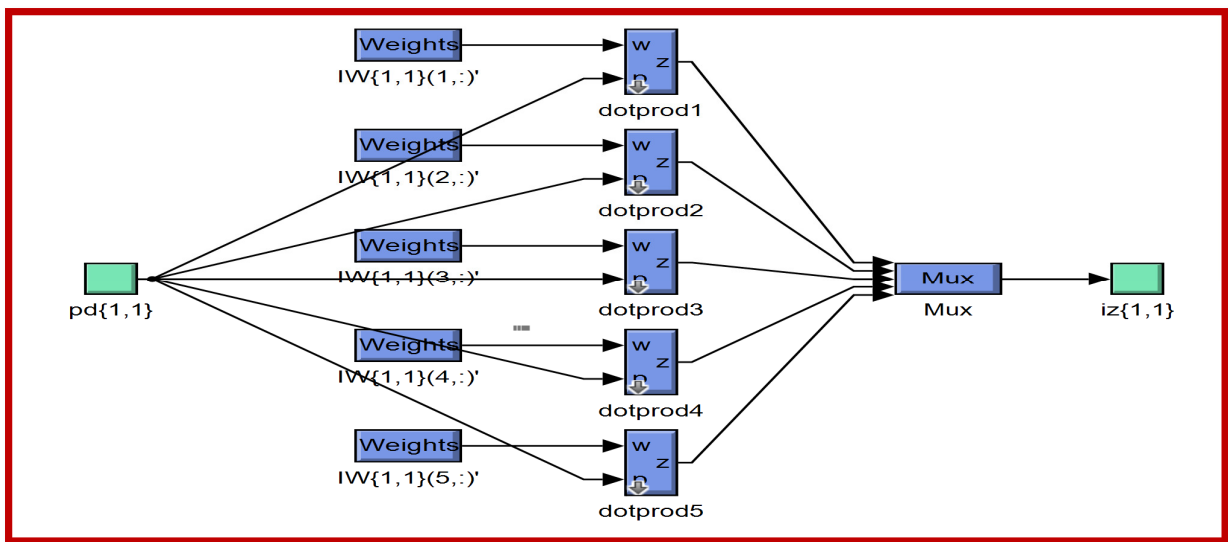


Fig.7 (b). The Internal Structure of the ANN Controller Layers

Figures 7(a) and 7(b) give the internal structure of the ANN controller. The input to the ANN controller will be the processed error difference between the reference voltage and the measured value of voltage in line 3-4 .

Figures 7(a) and 7(b) exhibits in detail the internal structure of the ANN controller designed for controlling the voltage and current parameters injected by the Shunt controller and the Series controller respectively. The error difference (ΔV) on the voltages in the line 3-4 are fed as inputs to the ANN controller following proper conversion procedures. Depending on the changes in the values of the voltages in the transmission line and in accordance with the equations depicted in the equations 11 to 13 the weights are adjusted to obtain the final output. But the initial guess of the weights is made on expertise and random basis. The results obtained through the initial guess made are fair in acceptance levels and the performance of the ANN is well within the expected regions.

The detailed results are explained in the following section. At each point of the disturbance the ANN controller responds properly in accordance with the changing conditions.

VI. THE TEST SYSTEM and THE TEST CONDITIONS

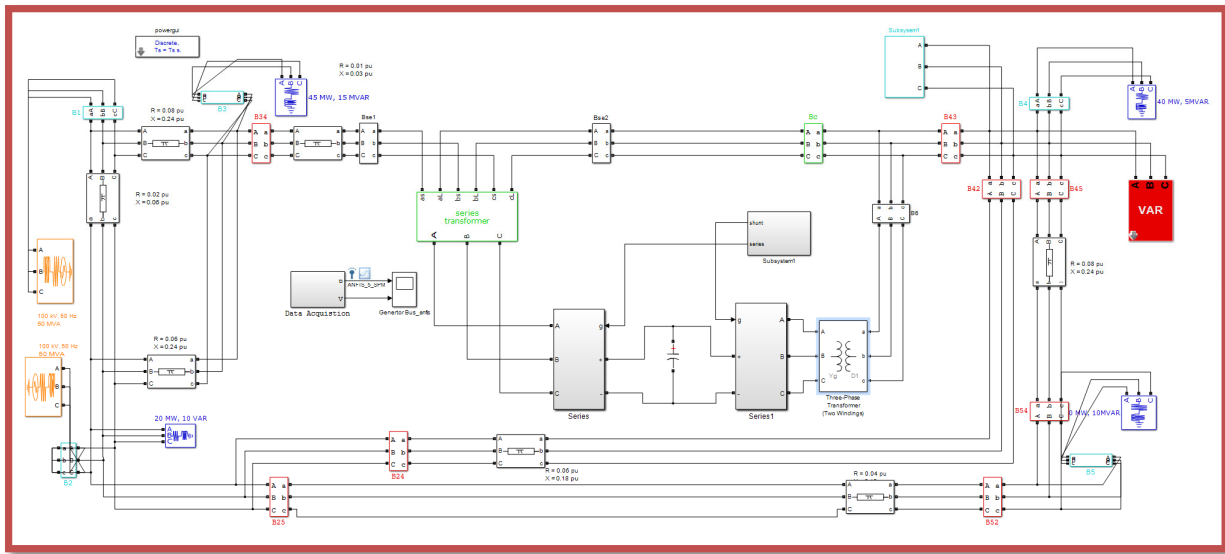


Fig.8 Simulink diagram of the complete IEEE 5 bus system connected with a 5 level CHB inverter based UPFC

The test system chosen is an IEEE 5 bus system. The system consists of 5 buses denoted from B1 to B5, coloured in cyan. Two generators are present in the system at bus numbers 1 and 2 each rated with 50MVA and 100KV. The load at bus 2 is 20MW + j10MVAR (inductive) at bus 3 is rated as 45MW + j15MVAR inductive, at bus 4 it is 40MW+ 5MVAR (inductive), at bus 5 it is 60MW+j10MVAR (inductive). The details of the line impedances are illustrated in the appendix. The above figure 7 gives an exhaustive description of the IEEE 5 bus system. It can be clearly seen that a 5 level CHB inverter based UPFC is connected between the buses 3 and 4. All the test conditions proposed are executed in the line 3 - 4 i.e., the inductive over loading and capacitor over loading conditions are created at bus number 4 between the time intervals 30 to 30.5 s and 35 to 35.5 s respectively. Shunt faults are created in the line 3 - 4 near bus number 4, which are explained in detail in the results and discussions section.

VII. SIMULATION RESULTS and DISCUSSIONS

(i) The complete power wave

The following figure 8 shows the complete pattern of the power wave in the line 3 – 4 when the line is subjected to inductive overloading, capacitive overloading, and shunt faults.

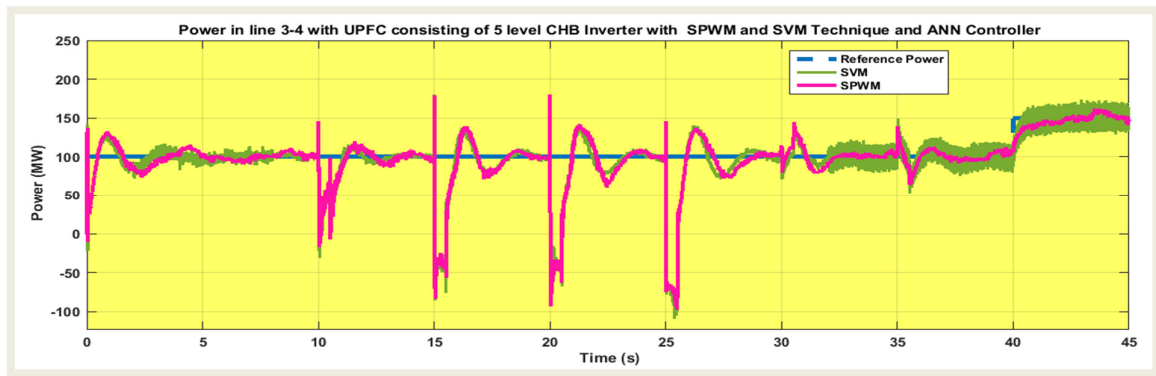


Fig. 8. The Complete Power Transferred through the Line 3-4 under different Test Conditions Using ANN Controller and SPM and SVM techniques

(ii) The initial power swing

The following figure 9 indicates the influence of the 5 level CHB inverter based UPFC in supporting generators by way of injecting additional power in the line 3-4 in reaching the designated power level of 100MW from initial state when SPWM technique is and when the SVM technique is used by the converters. It can be clearly observed that the power wave in the line 3 – 4 when a SVM technique used 5 level CHB inverter incorporated UPFC is used makes less oscillations and also reaches the designated 100MW mark in a less amount of time than the one with 3 level CHB inverter based UPFC. With SVM technique the power wave takes **6s** to reach the stable state while the one with the same ANN controller and SPM technique UPFC takes **8.0s** to reach the stable 100MW mark.

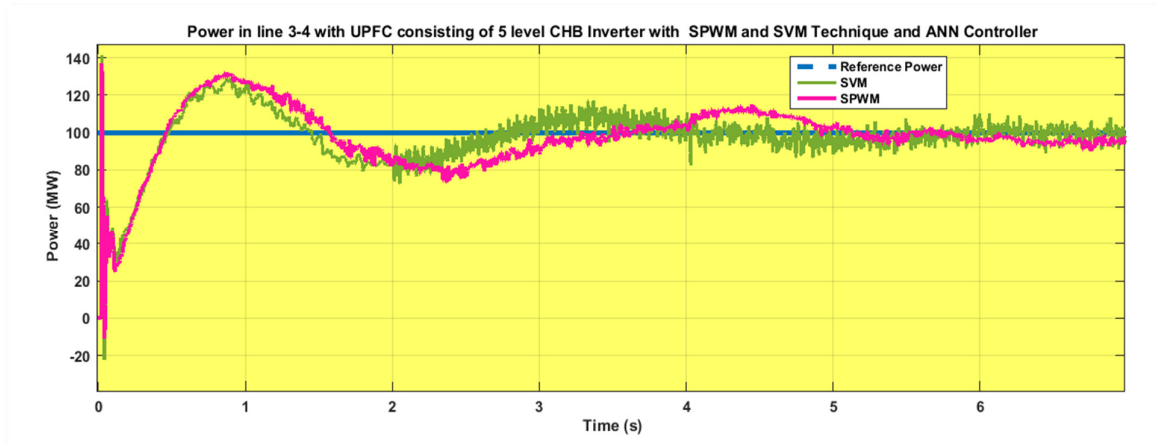


Fig.9. The Initial Power Swing through the line 3-4 using ANN controller and when SPM and SVM techniques are used

(iii) Single line to ground (LG) fault in line 3 - 4 near bus 4

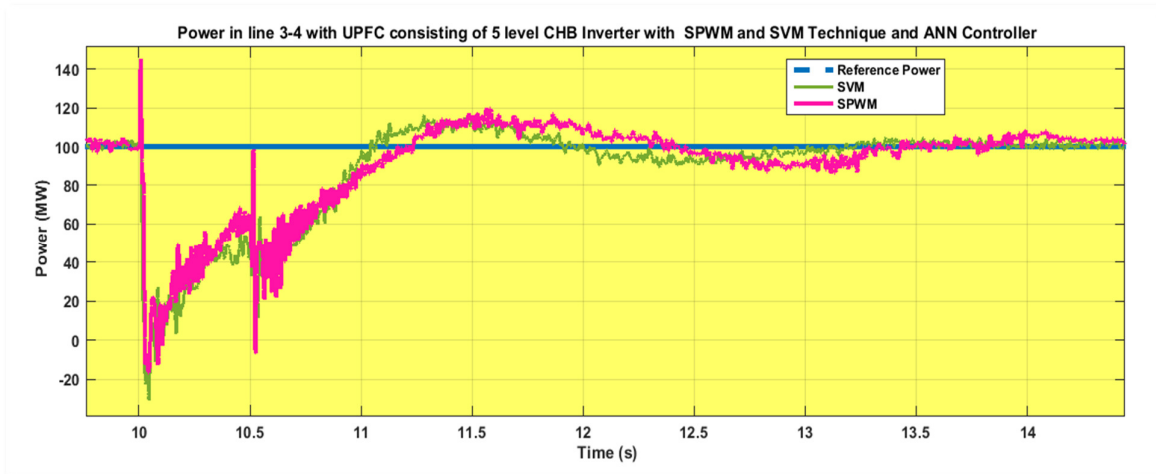


Fig.10. The Power Transferred through the Line 3-4 during LG fault conditions using SPWM and SVM techniques and an ANN controller

An LG fault is created in the line 3 – 4 near to the bus number 4 at 10th second and lasts up to 10.5 seconds. As soon as the fault is initiated the shunt and the series controllers initiate their respective corrective actions wherein the shunt controller adjusts the DC link voltage and the series controller the voltage to be injected by the series converter. But the capability of the UPFC when a 5 level CHB Inverter using SVM technique is more than when the SPWM technique is used. This fact is proved from the response time and the settling time depicted in the figure numbered 10. The time taken by the power wave to get settled at the normal / stable 100MW level from the point of initiation of fault is **3.25** seconds with SVM technique and it is **4.2** seconds with SPWM technique.

(iv) Triple line fault

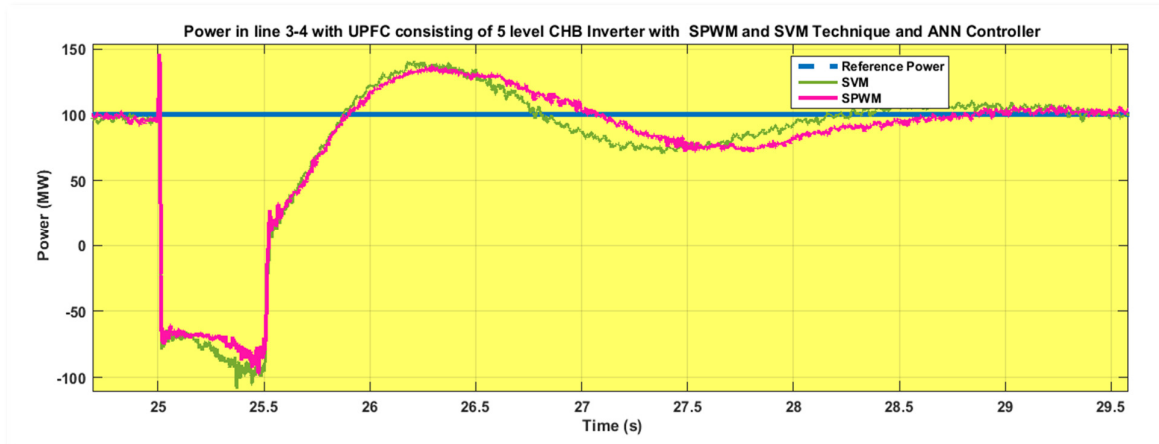


Fig.11. The Power Transferred through the Line 3 during LLL fault conditions using SPWM and SVM techniques and an ANN controller

Very similar to the LG fault conditions discussed above, an LL fault is created in the line 3 – 4 near to the bus number 4 at 25th second which lasts up to 25.5 seconds. As soon as the fault is initiated the shunt and the series converters are initiated by the ANN controllers in the two converters. As can be seen from the figure 11, the capability of the UPFC when a 5 level CHB Inverter with SVM technique is used in the UPFC is more than that when the 5 level CHB Inverter with SPWM technique is used. The time taken by the power wave to get settled at the normal / stable 100MW level from the point of initiation of fault is **3.1 seconds** with a 5 level SVM CHB Inverter and when a 5 level SPWM CHB Inverter is used it is **4.5 seconds**

(v) Voltage sag conditions due to inductive overloading at bus number 4

The capability of the UPFC for stabilizing the power system oscillations due to dynamic changes in the loading conditions is tested. Apart from the existing load of (40MW + j15MVAR) inductive at bus number 4, an excess inductive load of 50 MVAR inductive is added at the 30th second. The sudden dip and the successive oscillations made by the power wave in line 3 - 4 can be witnessed from the following figure 12 starting from the 30th second. These oscillations are successfully sustained by the ANN controller based UPFC when a 5 level CHB inverter using SVM technique and a 5 level CHB inverter using SPWM technique used, but with different settling times. The UPFC while using SVM technique brings the power wave to settle at 100MW targeted value within a period of **2.0 seconds** and while using SPWM takes **2.5 seconds**.

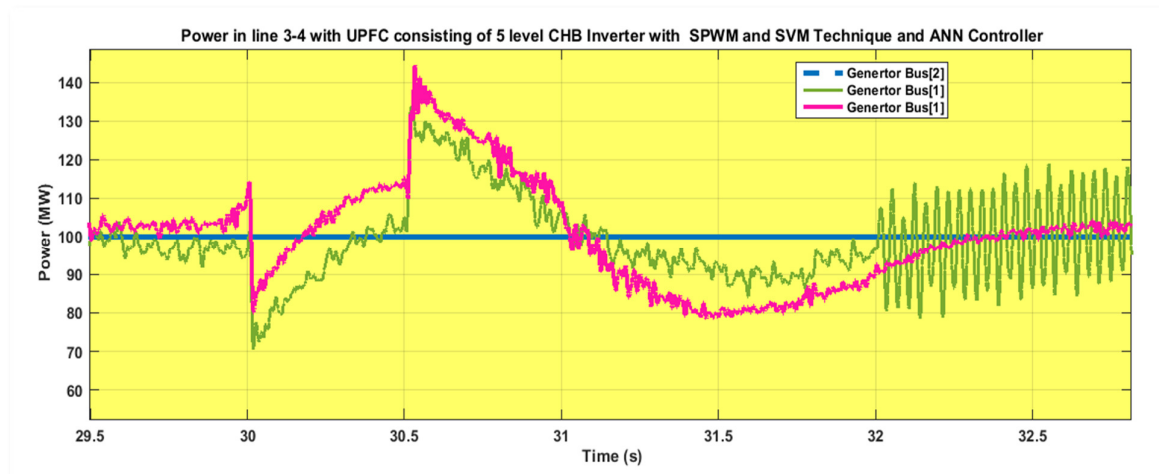


Fig.12. Power transferred through the line during Sag i.e., INDUCTIVE OVERLOADING

(iv) Voltage swell conditions due to capacitive overloading at bus 4

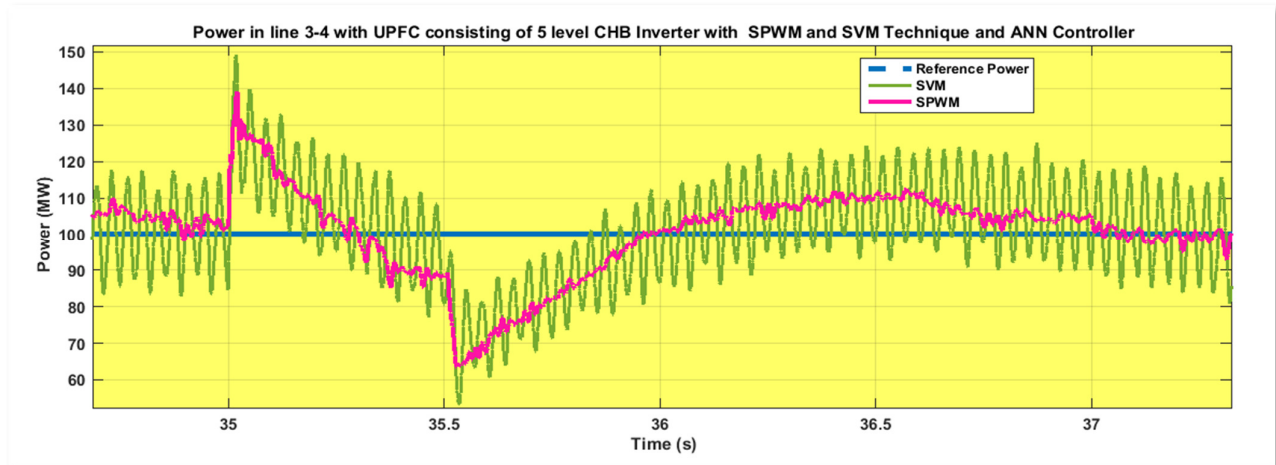


Fig.13. Power transferred through the line during Voltage Swell i.e., CAPACITIVE OVERLOADING

To test the capability of the UPFC for stabilizing the power system oscillations due to capacitive overloading, the loading conditions at bus number 4 are altered. Apart from the existing load of (40MW + j15MVAR) inductive, an excess load of 100 MVAR capacitive is added at the 30th second. The sudden swell and the successive oscillations made by the power wave in line 3 - 4 can be witnessed from the figure 13 starting from the 35th second. These oscillations are successfully sustained by the ANN controller based UPFC when a 5 level CHB Inverter is used in the UPFC but with different settling times when SVM and SPWM techniques are used. The UPFC using SVM technique makes the power wave to settle at 100MW targeted value within a period of **0.9 seconds** and when SPWM technique is used it takes **1.0 seconds**.

VIII RESULTS TABULATION

S.No	Type of Disturbance	Duration of disturbance in Seconds	Settling time is seconds ANN CONTROLLER	
			SPM	SVM
1	Initial Swing		8	6
2	Line to ground fault	0.5 (10 to 10.5)	4.2	3.25
3	Three Phase faults	0.5 (25 to 25.5)	4.5	3.1
4	Voltage Sag	0.5 (30 to 30.5)	2.5	2.0
5	Voltage Swell	0.5 (35 to 35.5)	1.0	0.9

Table 1: Settling times of the power wave during shunt faults and load disturbances

The above Table 1 shows clearly the times taken by the power wave to settle down to normal value of 100MW during different disturbances when the 5 level CHB inverter based, ANN controller incorporated UPFC uses SPM technique and SVM technique for its series and the shunt converters

IX. CONCLUSIONS

It can be concluded that the UPFC embedded with an ANFIS controller with an SVM technique has a faster response rate. Also the vulnerability to oscillations during the controlling state is more when SPM technique is used. This is because of the fact that the SPM technique uses approximate values or large intervals of pulse widths when compared to the SVM technique. The replication of the desired V_{ctrl} in case of SPM or V_{ref} in case of SVM, though both are to be produced by the Series Converter (where in actual $V_{ctrl} = V_{inj} = V_{ref}$) is more accurate with SVM technique. The settling times as read from the figures 8 to 13 are detailed in the Table 1. The ANN controller with SVM technique helps the power wave to settle 2 seconds in advance during the initial charging of the line and 1.05 seconds in advance during LG, 1.4 seconds in advance during the most severe of the shunt faults, the triple line fault, 0.5 seconds in advance during voltage sag and 0.1 seconds in advance during voltage swell conditions. It can be observed that also the computation time required by the SPM technique than the SVM technique is more. This Phenomenon can be observed from the fact that the Settling Time for Restoration of Normalcy during the occurrence of Different Kinds of Disturbances, like Voltage Sag, Voltage Swell or Faults like LG and LLL is lesser when SVM technique is used

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APPENDIX

IEEE-5 Bus System

NUMBER OF LINES = 7
NUMBER OF BUSES = 5

In all these BUS DATA's type-3 indicates slack bus, type-2 indicates PQ / load bus, type-1 indicates PV / generator bus.

LINE DATA

SB	EB	R (p.u)	X (p.u)	Ys	Tap
1	2	0.02	0.06	0.03	1
1	3	0.08	0.24	0.025	1
2	3	0.06	0.18	0.02	1
2	4	0.06	0.18	0.02	1
2	5	0.04	0.12	0.015	1
3	4	0.01	0.03	0.01	1
4	5	0.08	0.24	0.025	1

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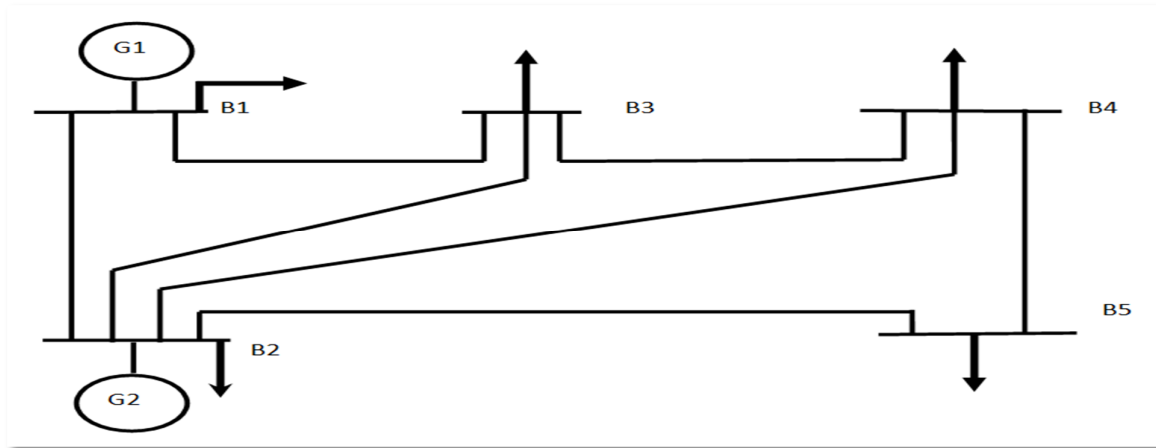


Figure : Line Diagram of the IEEE 5 Bus System

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