Performance Analysis Of A Transmission Line Connected With Upfc Designed With Three Level Cascaded H Bridge Inverter With Generalized Svpwm Technique Using Pi, Fuzzy Logic, Ann And Anfis Controllers

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Abstract*:* Power System Networks when subjected to faults behave in an abnormal pattern which could be called Non Linear behaviour. Conventional or traditional Controlling methods offer limited support to the controlling units like the FATCS devices in making the Power System network less effected by the faulty conditions and also in regaining normalcy. Artificial Neural Networks are Non Linear information processing devices, which are built from interconnected elementary processing devices called neurons. A Fuzzy Logic system is based on a mathematical formulation that takes in analog input values in terms of logical values and processes them. In general Fuzz Logic Controllers work on the If - Then Rule of Computations. The Performance improvement of UPFC with reference to the Transient stability and Dynamic stability enhancement incorpoating ANFIS, ANN, Fuzzy Logic and a PI controller is analysed. The UPFC is embedded with a 3 level cascaded H Bridge inverter. The Response time taken by UPFC with ANN, Fuzzy controller and PI Controller are computed. Cascaded H Bridge Inverters offer high level of Voltage Support, Low Switching Stress and Good Modularity. The system response to the Reference commands or the correction commands is very faster in ANN than in Fuzzy Logic based and PI controller based UPFC. This aspect is shown by calculating the times like settling time in all the four cases of faults like LG, LL, LLG, LLL and also even when the loads are changed from normal to highly Inductive and highly capacity. The UPFC is connected to the IEEE 5 bus system between the buses 3 and 4 for checking its capabilities. The improvement in the performance of UPFC with ANN Controller over the Fuzzy Logic based and the conventional PI controller based UPFC is depicted in the end result. Simulations results prove that the ANFIS controller based UPFC overperforms ANN Controller , the FUZZY LOGIC Controller Based and PI Controller based UPFC.The Simulations are carried using MATLAB Software

Keywords: UPFC, IEEE-5 BUS System, Shunt Line Faults, Power Flow Control, Cascaded H Bridge (CHB) Inverters, SVPWM, ANFIS Controller, ANN, FUZZY LOGIC and PI Controllers, Settling Time.

1. Introduction

The Unified Power Flow Controllers were basically proposed for real time control and dynamic compensation of the ac transmission system parameters and for obtaining more flexibility in solving the problems faced by the utilities. In the very introduction by Narain G Hingorani, the UPFC was able to control the power flow in the transmission line using the phase shifter technique and the transformer tap changing/setting technique [1]. But this method could not cater to the power systems where there was increase in loading conditions and the network complexity. With the advent of the power electronic converters, with high voltage and high current bearing capabilities, it slowly became feasible to obtain more flexibility in achieving control on the transmission line parameters, thus leading to the introduction of the concept of FACTS. Gyugyi and Hingorani proposed a UPFC with the aim of controlling the parameters on the transmission line viz., impedance, phase angle and voltage, simultaneously or selectively [2]. L. Y. Dong et al in 2002 proposed a model of the UPFC wherein the UPFC has voltage control capabilities. Besides that it has the capabilities of improving transient stability, mitigate system oscillations [3]. A simulation model of UPFC based on a twelve pulse converter was presented by Zheng et al. The UPFCs characteristics are investigated under normal and extreme disturbance conditions [7]. It is depicted in the paper that the UPFC can control voltage and power flow in the transmission line. N. F. Mailah et.al, in 2008 proposed a three phase multilevel inverter based UPFC in which theSTATCOM is designed using a traditional 6 pulse, three phase bridge topology, consisting of one rectifier and one inverter. The SSSC is a three level structure using IGBTs.

An earnest effort towards achieving the above goals is made here especially to improve the sensitivity of the device, the quality of output of the device, the response time of the device and also the controllability of the device by making the device to act like a self thinking machine. The Unified Power Flow Controller has two converters, one a shunt converter (converter 1), connected in shunt with the transmission network and other a series converter (converter 2) , connected in series with the Transmission Network These two converters are connected to each other by a common DC link capacitor. The presence of a common DC link enables the transfer of real and reactive power to flow between the two converters thereby enabling the absorption and injection of voltages and currents from and to the transmission network respectively. Each of the converters can independently generate and absorb

real and reactive power at their respective ac terminals. The basic function of the Shunt converter (converter 1) is to supply the real power it can also supply or absorb reactive power. The series converter (Converter 2) provides the main function of the UPFC by injecting an ac voltage of requisite magnitude Vpq ($0 \leq Vpq \leq Vpqmax$) and phase angle δ ($0 \leq \delta \leq \delta$ max) at power frequency in series with the transmission line voltage.

2. The test system and the test conditions

The test system chosen is an IEEE 5 bus system. The system consists of 5 buses denoted from B1 to B5. Two generators are present in the system at bus numbers 1 and 2 each rated with 50MVA and 100KV. The load at bus 2 is 20MW + j10MVAR (inductive) at bus 3 is rated as 45MW + j15MVAR inductive, at bus 4 it is 40MW+ j5MVAR (inductive), at bus 5 it is 60MW+j10MVAR (inductive).

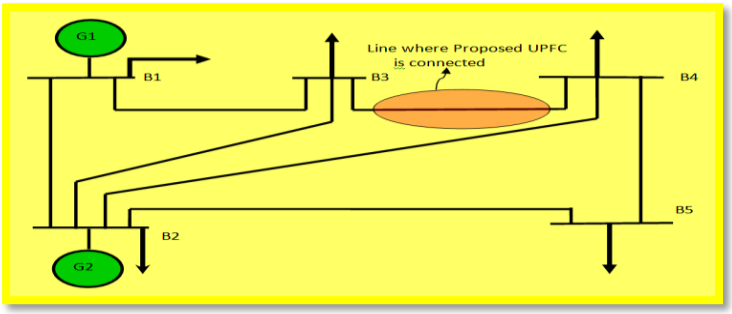

Fig.1 The IEEE 5 bus system used for testing the proposed UPFC model

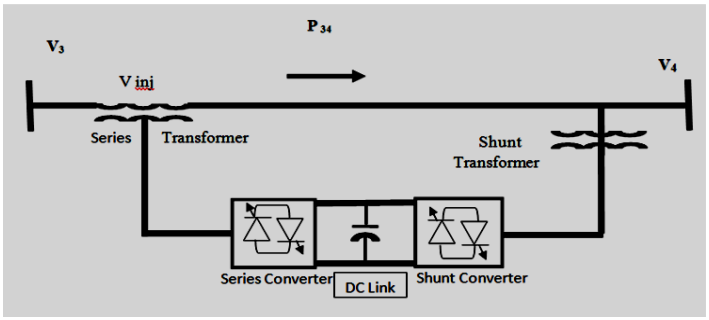

Fig.2 Three level CHB inverter based UPFC for IEEE-5 bus system

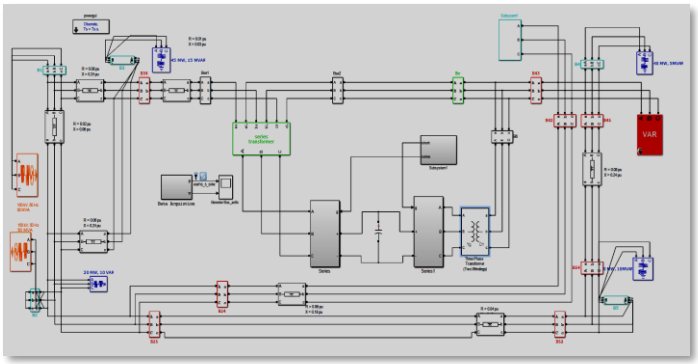

Fig.3 Simulink model of the entire test system

The details of the line impedances are illustrated in the appendix. The above figure 3 gives an exhaustive description of the IEEE 5 bus system developed in Matlab - Simulink. It can be clearly seen that a 3 level CHB inverter based UPFC is connected between the buses 3 and 4. All the test conditions proposed ((i) under voltage compensation (due to Increase in Inductive Load), (ii) over voltage compensation (due to Capacitive over Loadings), (iii) Transient Stability Enhancement Capabilities when the IEEE-5 Bus system is subjected to different Shunt Faults like LG (10 to 10.5 s interval), LL (15 to 15.5 s interval), LLG (20 to 20.5 s interval) and LLL (25 to 25.5 s interval) Faults at Bus No. 4, are executed in the line 3 - 4 i.e., the inductive over loading and capacitor over loading conditions are created at bus number 4 between the time intervals 30 to 30.5 s and 35 to 35.5 s respectively. Shunt faults are created in the line 3 - 4 near bus number 4, which are explained in detail in the results and discussions section.

Voltage Regulation is done with UPFC wherein the required voltage of change required on the Transmission line say ($\overline{V_3}$ ~ ($\overline{V_4}$)) = $\overline{\Delta V}$ or Δe (i.e., $\overline{V_{inj}}$), is injected either in-phase or in anti-phase mode with the existing voltage $\overline{Vo}$ or $\overline{V_{meas}}$ on the Transmission line.

Series Capacitive Compensation is done where the required value of voltage say, $\bar{V}_{\text{inj}}$, is injected in Quadrature with the Line Current ($\bar{I}_{34}$).

Phase Shifting or Transmission Angle Regulation is done by injecting a voltage of $\bar{V}_{\text{inj}}$ in an angular relationship with $\bar{V}_{\text{o}}$ to get the required Phase Shift (Advanced or Retarded) in the Line output voltage without change in the Magnitude of the Line output voltage.

3. The 3 level cascaded h bridge inverter

One of the outcomes of the Research on the attempt to improvising the Output Voltage of an inverter through Modifying Network/Circuit configurations of an Inverter is the Cascaded H Bridge (CHB) Inverter. The low switching voltage stress and modularity has made the Multi Level Inverters (MLIs) gain more attention. The low switching voltage stress and modularity has made the Multi Level Inverters (MLIs) gain more attention. The user desired Multi Level voltage is obtained by using a separate voltage sources (here capacitors). The major Advantages with Multi Level Inverters are their Minimum Harmonic Distortions in the Output Voltage, Low Electro Magnetic Emissions, High output to Input Ratios i.e., High Efficiency and More Importantly their High Voltage withstanding and Operating Capability and Modularity.

The Circuit Topology of 3 level Cascaded H Bridge Inverter Used

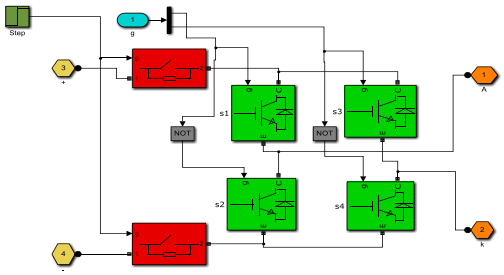

Fig.4 Basic Circuit of a CHB Inverter used in this Simulation

The equation for the output wave of the Cascaded H Bridge Inverter is given by

$$\bar{V}_{ac} = \bar{V}_{out} = \bar{V}_{ref} =$$

$$\frac{4}{\pi} * \frac{V_{dc}}{2} * \sum_{n=1,3,5,}^{\infty} \frac{1}{n}(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4) + \dots\dots\dots + \cos(n\theta_n)) * \sin n\varphi \quad (1)$$

Where n= Harmonic Number

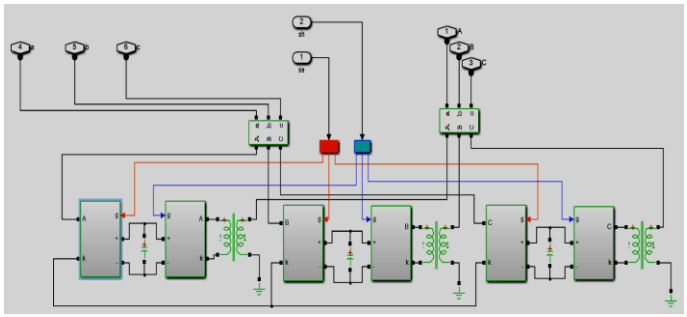

Fig.5 The 3 Level Cascaded H Bridge Inverter used in this Simulation

The equation for the fundamental wave is given by (for n=1)

$$\frac{4}{\pi} * \frac{V_{dc}}{2} * \sum_{n=1,3,5,}^{\infty} \frac{1}{n}(\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \dots\dots\dots + \cos(\theta_n)) * \sin\varphi \quad (2)$$

4. Design analysis of the controllers

IV.1 THE DESIGN OF PI CONTROLLERS USED

The Proportional Integral (PI) Controller designed here is supposed to maintain the Output voltage and Power Flow to be intact with the reference values defined by the user.

The PI controllers used here are two in number

(i) The DC Capacitor Voltage (E_{dc} or V_{dc}) Controller (Shunt controller)

(ii) The Injected Voltage Controller ($\bar{V}_{inj}$) (Series Controller)

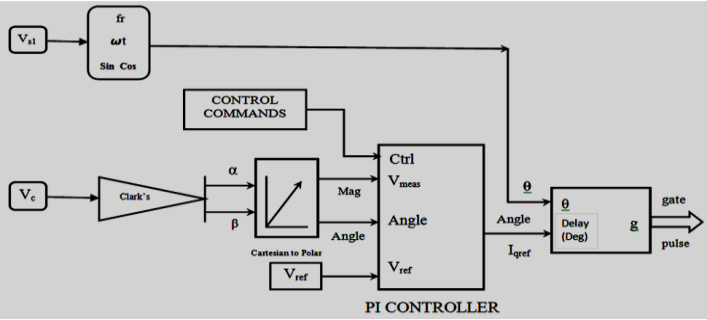

Fig.6 The initiation circuit of the PI controller

The initiation circuit, shown in figure 6, of the PI Controller takes inputs from the IEEE 5 bus system's 4th Bus i.e., the Load Bus for us, and the DC capacitor voltage at the DC Link, continuously and compares it with the Reference values ($\bar{V}_{ref}$) defined by us and processes it for further correction initiation action by the Shunt Converter. The Capabilities of the PI Controller Tested here are for the problems that occur at the Bus 3-4, like (i) change of Nature of Load from normal to Highly Inductive (ii) normal to Highly Capacitive (iii) during the occurrence of faults like LG, LL, LLG and LLL.

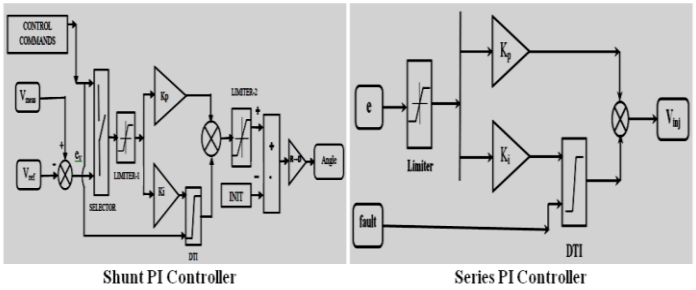

Fig.7 The internal structure of the shunt and series PI controllers

The controllers are designed to track the voltage on the line to be equal to 100KV and power in the line to be 100MW

5. 2 the fuzzy logic controller design

The following figure 8 shows the initiation circuit of the fuzzy Logic controller, where the voltages measured on the line 3-4 of the IEE 5 bus system are continuously monitored. The values of the reference voltage $\bar{V}_{ref}$ of 100KV is fed. Also the control commands which activate the controller for every change i.e., over load, faults can also be seen.

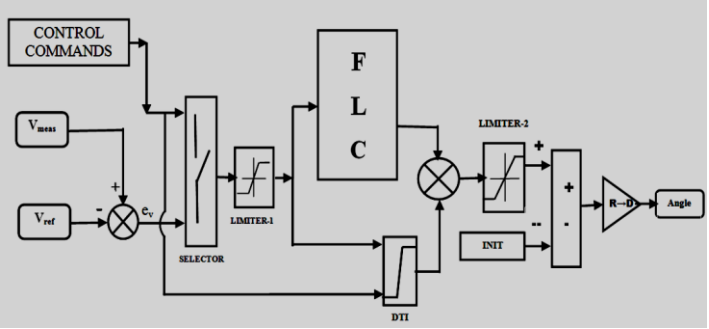

Fig.8 The initialization Circuit for the Fuzzy Logic Controller

The notation used:

e (k) : input error
ref (k) : reference signal
ϕ (k): output signal
Δe (k) : change in error

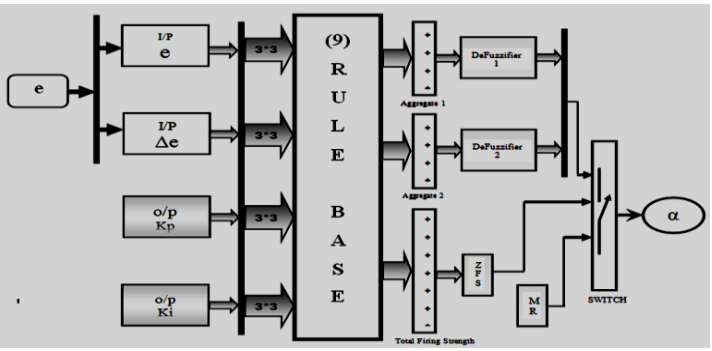

Fig.9 The Fuzzy Logic Controller

Figure 9 shown gives the details of the procedure followed for calculating the angle required for injecting the voltage., for controlling the Two input signals, the error in voltage ($e=\bar{V}_{ref} - \bar{V}_{meas}$), difference Δe, are modified to fuzzy numbers in fuzzifier.

" The solution of an integrator given by **Euler's Integration** as,

$$\phi(k) \square\square \phi(k \square 1) \square\square \Delta\phi(k) \ldots\ldots\ldots\ldots\ldots (3)$$

the term Δ **α** (k) is expressed as:

$$\Delta\phi(k) = K T_s e(k) \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

As shown in Fig10, there are two inputs to the fuzzy inference system (i) the control error **e(k),** (ii) the change in this error **Δe(k).**

$$e(k) = ref(k) - \phi(k) \ldots\ldots\ldots\ldots (5)$$
$$\Delta e(k) = e(k) - e(k-1) \ldots\ldots\ldots\ldots (6)" [16,17,18]$$

The fuzzy rule base, shown in figure 10,
The most convenient way of expressing the membership functions is the triangular mf
"Therefore the following function is used to represent the fuzzy triangular membership functions.

$$\mu(x) = \max\left[\left(\min\left(\frac{x-x_1}{x_2-x_1}, \frac{x_3-x}{x_3-x_2}\right), 0\right]\right] \ldots\ldots (7)$$

NB: Neg Big, NS Neg Small Z: Zero
PB: Pos Big, PS: Pos Small."[16,17,18]

Table 1: The fuzzy rule decision table

	Δ_e

		NB	NS	ZZ	PS	PB
e	PB	Z	p	p	p	P
	PS	N	Z	p	p	P
	ZZ	N	N	Z	P	P
	NS	N	N	N	Z	p
	NB	N	N	N	N	Z

6. DEFUZZIFICATION

The **center of area** calculation procedure is used in fuzzy logic application.

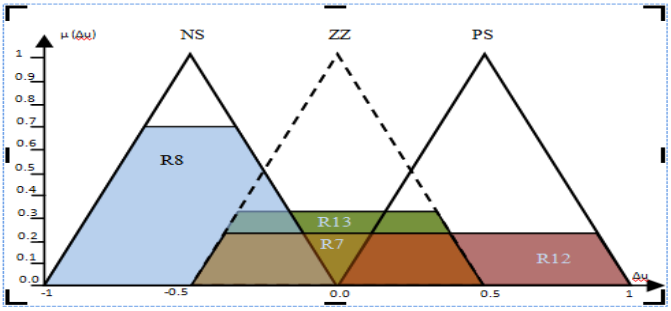

Fig. 10 M Fs representing fuzzy partitions the universe of $\Delta\boldsymbol{\phi}$.

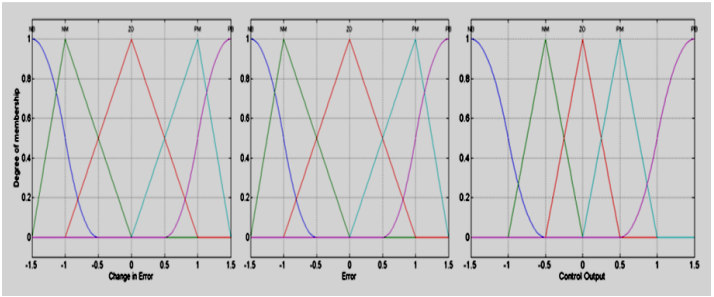

Fig. 11 Graphs indicating the relation between Degree of Membership and (i) change in error (ii) error and (iii) control output.

$$\Delta\phi_R(k) = \frac{\sum_{i=7,8,12,13} \mu_{R_i}(\Delta\phi_R)\,\Delta\phi_R(Ri)}{\sum_{i=7,8,12,13} \mu_{R_i}} \ldots\ldots\ldots\ldots (8)$$

$$\Delta\phi_R(k) = \frac{0.7(0.05)+0.2(-0.05)+0.3(0.0)+0.2(0.0)}{0.2+0.7+0.2+0.3} = -0.178 \quad \ldots . (9)$$

"Where, Δϕ(Ri) is the crisp, Δϕ value corresponding to the maximum membership degree of the fuzzy set that is an output from the rule decision table for the rule Ri."[17,18].

3 artificial neural network (ann) controller design

"Artificial neural networks (ANN) are nonlinear data/signal processing devices. Neural Networks have remarkable ability to derive meanings from complicated/ imprecise data.." [19,20,21]. In fig 12, gating signals are generated based on the reference angles supplied by the MATLAB simulated , ANN control system. As can be seen from figure 13, the load voltage that is the voltage at 4^{th} bus (V_{load}) is measured (it is also referred to as V_{meas}) and is fed as one of the inputs to the ANN controller. The other input is the reference voltage value (V_{ref} = 100KV).

The difference of the signals is the error signal written as

$$e_v = \overline{V}_{ref} - \overline{V}_{meas} \ldots\ldots\ldots\ldots\ldots (10)$$

(Here the value of V_{ref} = 100 KV)

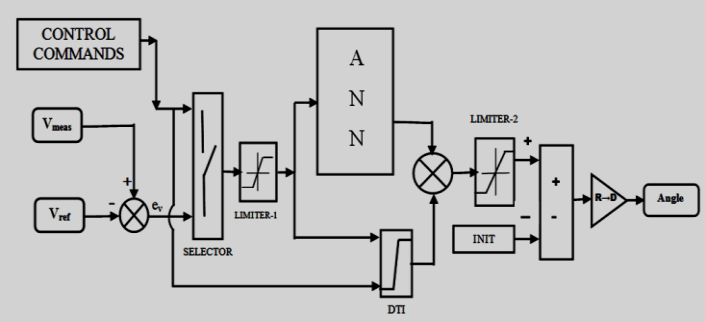

Fig.12 The initialization circuit of the ANN controller

The neural signal generator is simple two layer network with ten hidden neurons. The model of neural network and the blocks in that are shown in the following figures 14, 15 and 16. He outputs of the ANN controller will be the magnitude and angle of the voltage that is to be produced b the 3 level CHB Inverter.

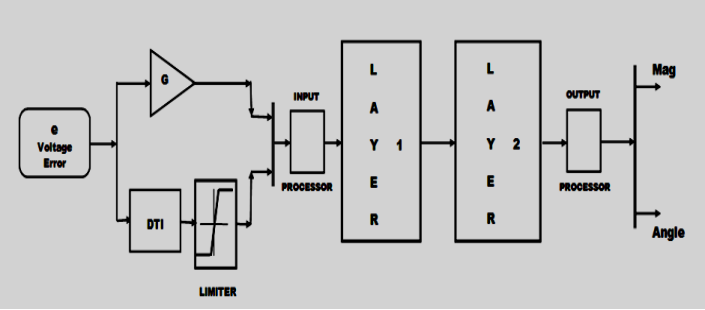

Fig.13 The internal circuit of the ANN controller with two layers

The numbers of layers for the proposed neural schema are chosen to be two. There are no hard and fast rules or any mathematical based restrictions/analysis proposed in the literature for choosing the number of layers, here the choice is made based on the efficiency of the 2 layers to give the root mean square value of the voltage error [RMS (e_v)] and power error [RMS (e_p)] quickly. The second layer is added to increase networks prediction capability as the nonlinearity increase due to different faults (LG, LL, LLG, and LLL) created in the line 3-4.

$$\mathbf{e_p = P_{ref} - P_{meas}}$$

The stages of ANN procedure are listed hereunder

1. Weights are initialized
2. Data pertaining to the inputs and outputs are scaled
3. Network structure selection –Two layers and 5*5 weights
4. Training pair is selected from the training set.
5. Network output is calculated based on the weights and initial input set.
6. Errors e_v in case of voltage and e_p in case of power are calculated.
7. Error is propagate backward and weights are adjusted till the error is minimized..
8. Steps 5 till 8 are repeated until the error value is minimized to the desired minimum value

The weights defined are given below

$$\begin{bmatrix} \mathbf{W(1) = -0.00091616482794267906} & \mathbf{-0.0038954121128581898} \\ \mathbf{W(2) = 0.073232638075405698} & \mathbf{0.07197822846703536} \\ \mathbf{W(3) = 0.073232638075405698} & \mathbf{0.07197822846703536} \\ \mathbf{W(4) = 5.3927848742317011} & \mathbf{19.628567578558297} \\ \mathbf{W(5) = 0.0020571246610299452} & \mathbf{0.0079557556765511885} \end{bmatrix}$$

The bias defined is given below

$$\begin{bmatrix} \mathbf{6.999991349213313} & \mathbf{-0.0031854924848694548} \\ \mathbf{0.0013053422218281478} & \mathbf{4.4885160183711683} \\ \mathbf{-6.9999619861075493} & \end{bmatrix}$$

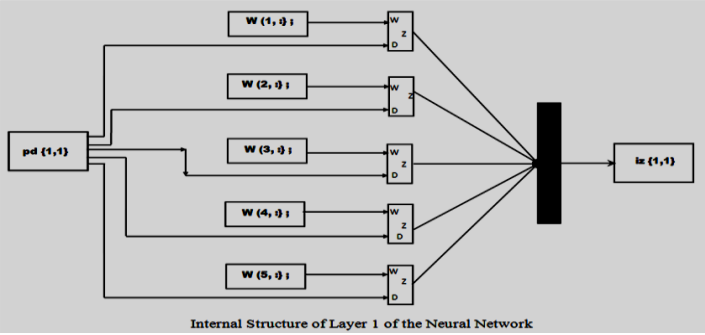

Fig.14 The ANN controller's internal structure of Layer 1

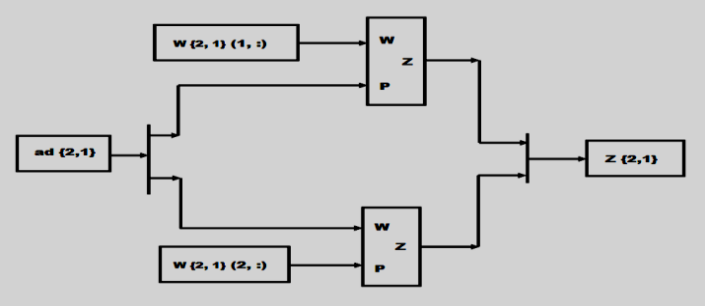

Fig.15 The Internal Structure of Layer 2 of the ANN Controller

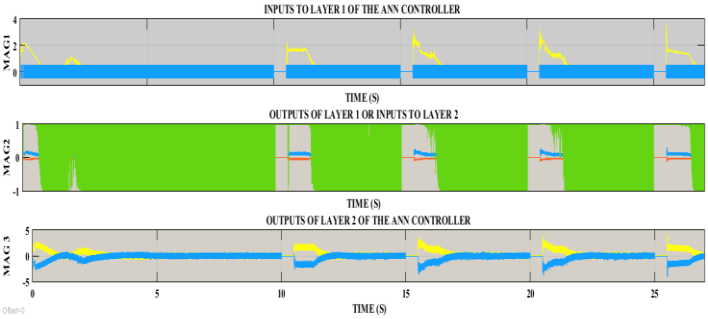

Fig.16 The inputs and outputs of layers 1 and 2 of the Series ANN controller

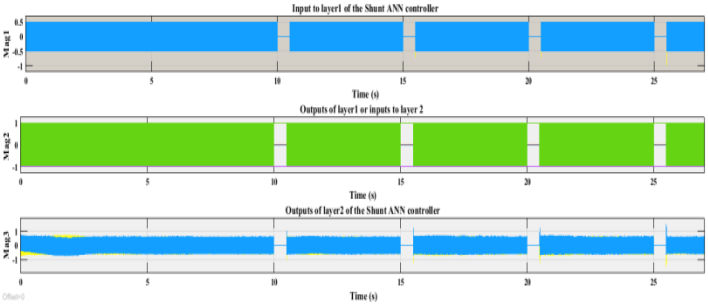

Fig.17 Inputs and Output of layers 1 and 2 of the shunt ANN controller

4 anfis controller

The ANFIS controllers used in the series and the shunt converters are depicted in the following figures and are explained in detail

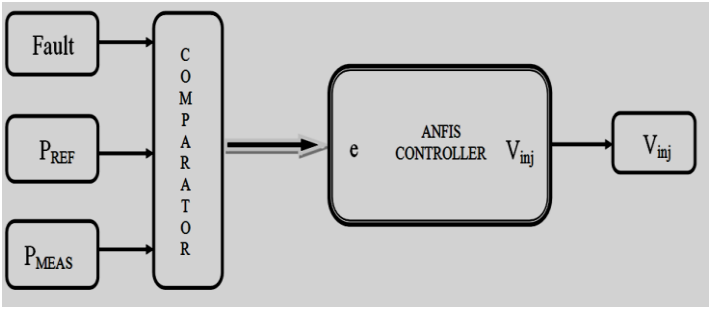

Fig.18 The series converter's ANFIS Controller

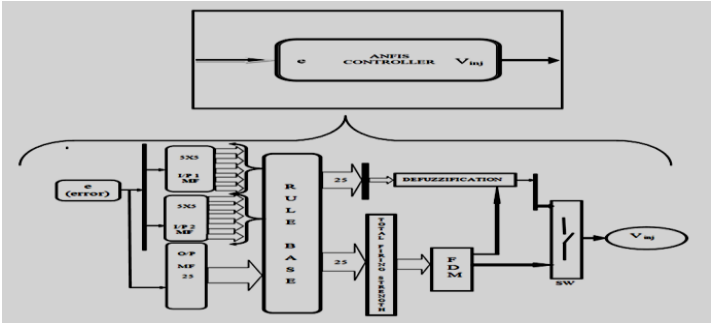

Fig.19. The Block diagram of the ANFIS Controller

ANFIS architecture consists of five layers with the output of the nodes in each respective layer is represented by $O_{l,i}$where *i* is the i^{th} node of layer *l*.

7. The rule based block (layer1 & layer2)

In Fig.20 the Δe membership function generator consists of five sub blocks that generate membership function from NB, NS, ZZ, PS, PB subsets and is located in horizon and is upper block. The vertical block generates the membership functions from subsets belonging to the e. Each membership generated by NB(Δe), NS(Δe), ZZ(Δe), PS(Δe), PB(Δe) is comparing peer to peer with each membership generated by NB(e), NS(e), ZZ(e), PS(e), PB(e), then the minimum value of each pair will be used for calculation of final fuzzy value. The 25 rules base fuzzification is used for processing the input.

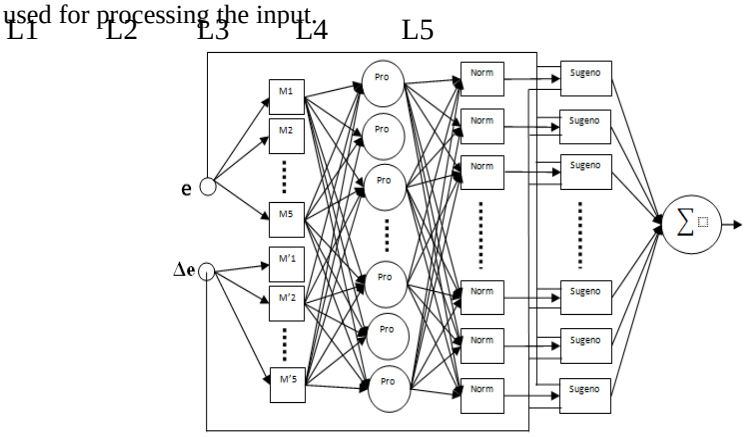

Fig.20 The architecture of the ANFIS controller implmented

"LAYER 1:

Every node i in this layer is an adaptive node with a node function
$O_{1,i} = \mu_{Ai}(x)$ for i = 1, 2, or
$O_{1,i} = \mu_{Bi-2}(x)$ for i = 3, 4
• X (or y) is the input node i and A_i (or B_{i-2}) is a linguistic label associated with this node
• Therefore $O_{1,i}$ is the membership grade of the fuzzy set (A_1,A_2,B_1,B_2).

LAYER 2:

In this layer the output of each node is product of input signals, be expressed as :
$O_{2,i} = w_i = \mu_{Ai}(x) \cdot \mu_{Bi}(y)$, i = 1, 2
And in this layer each node represents the firing strength of the rule.

LAYER 3:
In this layer the i[th] node calculates the ratio of the i[th] rule's firing strength to the sum of all rule's firing strengths.

$$\overline{w_i} = \frac{w_i}{w_1 + w_2 + \cdots + w_n}$$

The outputs are called normalized firing strengths.

LAYER 4:
Every node i in this layer is an adaptive node with a node function:

$$O_{4,i} = \overline{w_i} f_i = \overline{w_i}\,(p_i x + q_i y + r_i)$$

Where w_i is the normalized firing strength from layer 3, and $\{p_i, q_i, r_i\}$ is the parameter set of this node, that we referred them as **consequent parameters**.

LAYER 5
This layer computes the overall output as the summation of all incoming signals. It can be expressed as following:

$$\boldsymbol{O_{5,i} = \sum_i \overline{w_i} f_i = \frac{\sum_i w_i f_i}{\sum_i w_i}}$$

The learning rule which is applied to this project is Hebbian learning rule which is an unsupervised learning method.

$$\boldsymbol{w_i(new) = w_i(old) + x_i y}$$

The changes in connection strengths in the neural network are calculated using the "Hebbian learning rule", in which a change in the strength of a connection is a function of the pre and post synaptic neural activities. Here y_j is the output of the pre-synaptic neuron, x_i the output of the postsynaptic neuron, and w_{ij} the strength of the connection between them, and γ learning rate, the one form of a learning rule adopted is:

$$\boldsymbol{\Delta W_{ij}(t) = \gamma(x_i)(y_j)}$$

A more general form of a hebbian learning rule would be:

$$\boldsymbol{\Delta W_{ij}(t) = F(x_j, y_j, \gamma, t, \theta)}$$

in which time and learning thresholds can be taken into account."[20,21,22].

The space vector pwm technique

Ref [26] has explained in detail the new space vector PWM technique which can be applied for enhancing the capabilities of the UPFC.

The 3 level CHB Inverter has THREE possible output voltage levels for each phase, ranging from $+V_{dc}$ to $-V_{dc}$, resulting in $3^3 = 27$ possible space vectors for the inverter.

Out of which, the number of independent or space vectors is
$(3n^2 - 3n + 1) = ((3*9)-(3*3)+1) = 20$
Where **n = 3** for a Three level inverter.
There are **$(n - 1) = (3-1) = 2$** layers and
$(n - 1)^3 = (3-1)^3 = 8$ triangles in the Space Vector Diagram.

Depending upon the requirement of output given by the Comparator in the Controller of the UPFC the SVPWM selects the Sector of the Voltage to be generated say V_{ref} in which the required voltage lies and Pulses are generated accordingly.
The widths of the pulses are given by the following Volt – Second balance Equations for one sector is given by

$$\boldsymbol{V_{ref} * T_s = V_1 T_a + V_2 T_b + V_0 T_0} \qquad \textbf{(5)}$$

Where T_s is the sampling interval; and T_1, T_2, T_0 are the respective dwell times for the vectors V_1, V_2 and V_0. The values of T_1, T_2 and T_0 are given in [2]

$$T_1 = T_s * m * Sin (60–\alpha)$$
$$T_2 = T_s * m * Sin (\alpha)$$
$$T_0 = T_s – T_a - T_b$$
$$m = \frac{\sqrt{3} * V_{ref}}{E_{dc}}$$

The Series Injection Transformer is designed to a Transformation ratio of 1:1 Therefore the value of V_{out} of the CHB Inverter will be equal to the value of voltage injected in series with the line, V_{inj}

Therefore

$$V_{ref} = V_{inj} = V_{out}$$

Reference voltage Decomposition in linear modulation region ($0 \leq MI/Mi \leq 0.907$)

"In this mode, the V_{ref} moves on a circular trajectory as shown in Fig. 7. As the locus is within the hexagon, the MI can be controlled linearly. The decomposition (of Vref) into m–n axis, for a three level CHB inverter can be obtained using the following equations

$$V_{RefN} = \frac{2(3-1)\,V_{ref}}{\sqrt{3}\,E_{dc}}\ sin\,\alpha \qquad (1)$$

$$V_{RefM} = \frac{2(3-1)\,V_{ref}}{\sqrt{3}\,E_{dc}}\ \sin\left(\frac{\pi}{3} - \alpha\right) \qquad (2)$$

$$M_i = \frac{0.907 * V_{ref}}{0.866 * E_{dc}}\ \sin\alpha \qquad (3)$$

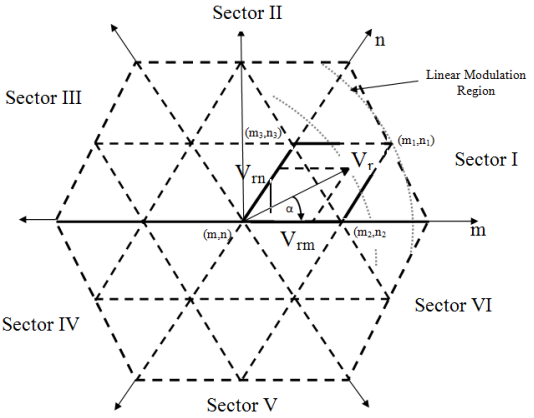

Fig.7 Representation of nearest 3 vectors in linear mode

$$n_1 * T_1 + n_2 * T_2 + n_3 * T_3 = T_s * V_{refn} \qquad (4)$$

$$m_1 * T_1 + m_2 * T_2 + m_3 * T_3 = T_s * V_{refm} \qquad (5)$$

$$T_1 + T_2 + T_3 = T_s \qquad (6)$$

Over-modulation mode I ($0.907 \leq MI/M_i \leq 0.953$)

This mode is identified by the inequality as ($V_{refm} + V_{refn}$) > M−1 (for an M-level inverter) , is depicted by a non-linear curve, which is simplified by the approximation techniques.

Over-modulation mode II ($0.935 \leq MI/M_i \leq 1.0$)

For [$\alpha_h < \alpha < (\pi/3–\alpha_h)$]:The magnitude of the Vref crosses the hexagon (where $V_{refm} + V_{refn} > M−1$) and the reference must be modified appropriately to mode I

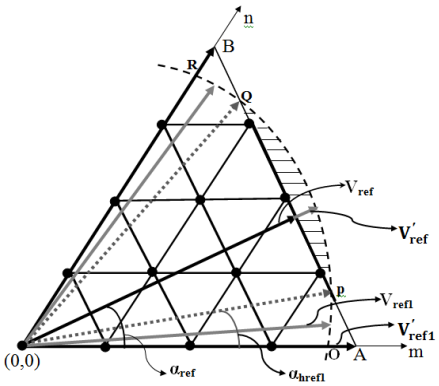

Fig. Modified Reference Vector in over modulation mode II

Important observation to be noted is that the over modulation modes I and II enhanced the voltage magnitude injection range of the UPFC without using extra components. With the help of extended voltage range, the UPFC's power controllability on the transmission line also increased."[26].

8. Results and discussions

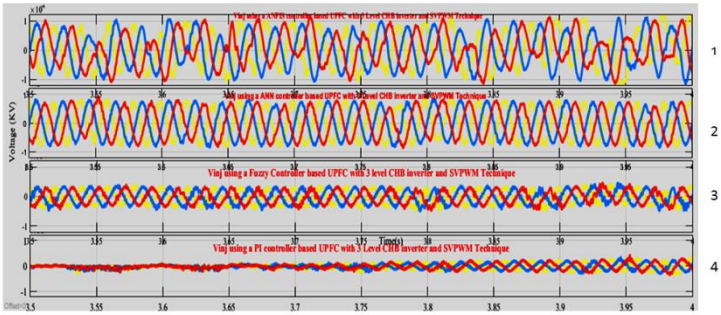

Fig. The Vinj value between the intervals 3.0 s to 4s by the (1) ANFIS, (2) ANN, (3) FL and (4) PI Controller based UPFC

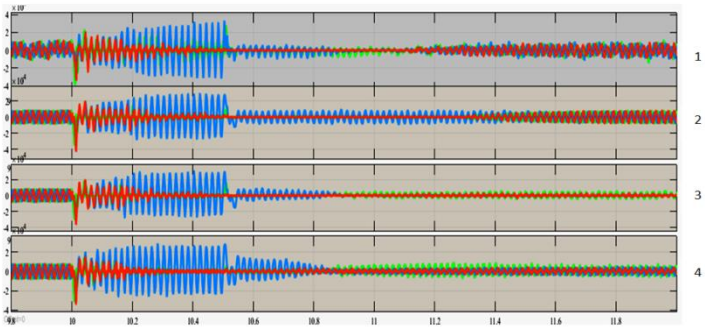

Fig. The Vinj value between the intervals 9.8s to 12s by the (1) ANFIS, (2) ANN, (3) FL and (4) PI Controller based UPFC

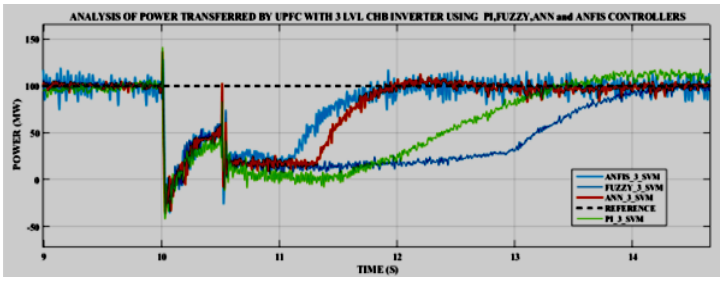

Fig.12. Power Transferred Through the Line during LG Fault with a PI, FUZZY LOGIC, ANN and ANFIS Controller

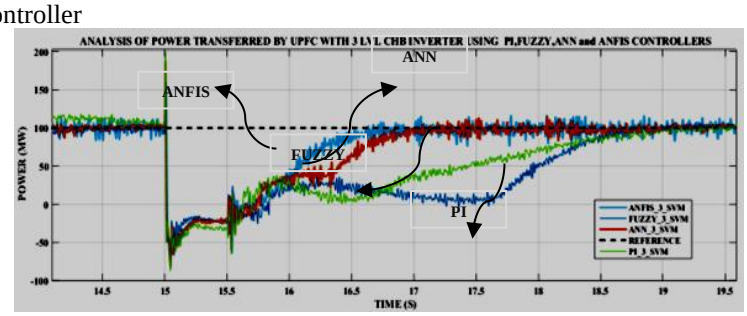

Fig.13. Power Transferred Through the Line during LL Fault with a PI, FUZZY LOGIC, ANN and ANFIS Controller

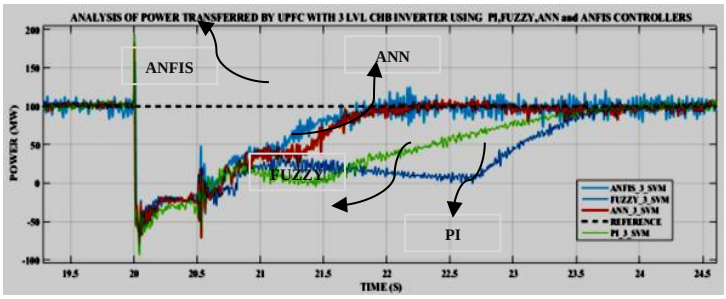

Fig.14. Power Transferred Through the Line During LLG Fault with a PI, FUZZY LOGIC, ANN and ANFIS Controller

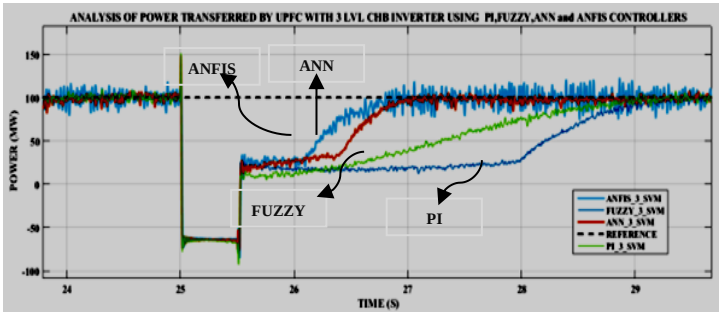

Fig.15. Power Transferred Through the Line during LLL Fault with a PI, FUZZY LOGIC, ANN and ANFIS Controller

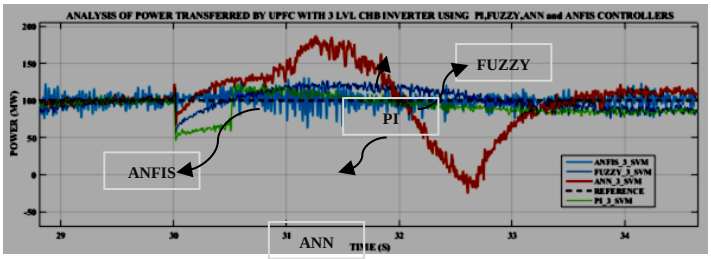

Fig.16. Power Transferred Through the Line during INDUCTIVE LOADING, with a PI, FUZZY LOGIC, ANN and ANFIS Controller

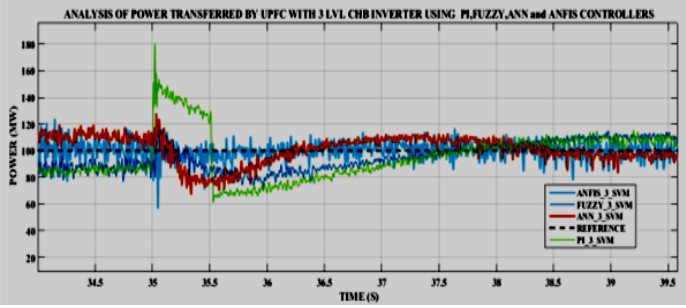

Fig.17. Power Transferred Through the Line During CAPACITIVE OVER LOADING with a PI , FUZZY LOGIC, ANN and ANFIS Controller

Table 2: RESULTS TABULATION

S.No	TYPE OF DISTURBANCE	DURATION OF DISTURBANCE IN SECONDS	SETTLING TIME IN SECONDS (EXACT TIME)			
			PI	FUZZY LOGIC	ANN	ANFIS
1	INITIAL SWING		9.5	8	3.5	1.5
2	LINE TO GROUNG FAULT	0.5 (10 to 10.5)	3.0	4 (at 14.5)	(11.5) 12	1.7 (11.57)
3	LINE TO LINE FAULT	0.5 (15 to 15.5)	4.5	3.5 (at 19)	2 (17.5)	1.75 (16.75)
4	LINE TO LINE TO GROUND	0.5 (20 to 20.5)	3.5	3.5 (at 24)	2.0 (22.5)	1.8 (22)
5	THREE PHASE FAULT	0.5 (25 to 25.5)	4.0	3.8 (at 29.3)	2 (27.5)	1.85 (27)
6	VOLTAGE SAG	0.5 (30 to 30.5)	2.7	2.5 (at 32.0)	2.3	0.5 (30.5)
7	VOLTAGE SWELL	0.5 (35 to 35.5)	3.1	2.8 (at 37.5)	2.5 (36.5)	0.6 (35.5)

9. Conclusions

From The detailed analysis of the simulation results it can be concluded that the combination of 3 Level CHB Inverter with ANFIS Controller in a UPFC has a faster performance when compared to the combination of 3 level CHB Inverter with ANN, FL and PI Controllers. The above Table Number 2 indicates that the UPFC embedded with a ANFIS controller has a faster response and hence is the most apt combination of (Hardware) Inverter and a Soft Computing technique. This Phenomenon can be observed from the fact that the Settling Time for Restoration of Normalcy during the occurrence of Different Kinds of Disturbances, like Voltage Sag, Voltage Swell or Faults like LG, LL, LLG, and LLL, is lesser when ANFIS controller is used than the settling time taken by a UPFC with a ANN,FL and PI Controller.

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