Turkish Journal of Computer and Mathematics Education Vol.12 No. 10(2021),6035- 6045

Research Article

Efficient Non-Isolated DC-DC Converter Using Variable Switching Frequency Control

Praful V. Nandankar [a], Prashant P. Bedekar [b] and Prashant Kumar V. Dhawas [c]
[a] Electrical Engineering Department, Govt. College of Engineering, Chandrapur, India, pppful@gmail.com
[b] Electrical Engineering Department, Govt. College of Engineering, Chandrapur, India, ppbedekar@gmail.com
[c] Electrical Engineering Department, Govt. College of Engineering, Chandrapur, India, prashantdhawas1@gmail.com

Article History: Received: 11 January 2021; Revised: 12 February 2021; Accepted: 27 March 2021; Published online: 28 April 2021

Abstract: A load adaptive high efficiency dc-dc converter with optimized switching control is proposed in this paper. The converter is controlled through the switching frequency auto-tuning over a full range of load changes. The load current tracking using a single current sensor is implemented with real-time computation of the desired switching frequency. It presents the latest algorithm to adopt the loading condition while keeping the output voltage constant. The algorithm is employed with a low-cost microcontroller having the capability to maintain dynamic performance through DPWM operation. In different operational conditions and with varying parameters, the converter continually retains the higher switching frequency. This proposed AFO (Adaptive frequency Optimization) controller performance is presented through simulation using MATLAB/SIMULINK and results are verified on a 100W DC-DC converter.

Keywords: Variable frequency, Switching loss, Efficiency, DC-DC converter, Adaptive control.

I. INTRODUCTION

In the academic world as well as the industry of power electronics, the DC-DC converter has steadily gained interest [1]. The DC-DC converter may be isolated or non-isolated depending on the use. The high-frequency transformer is the best candidate to attain load-source isolation. However, the non-isolated dc-dc converters are far better for increasing their size, cost, and weight. The non-isolated DC-DC converter offers a simple topology as well as control.

The converter works in DCM (discontinuous conduction mode) to obtain high efficiency as well as high power density. When the converter works in DCM mode, the inductor size may be reduced. Since the DCM operation leads to high-frequency switching-current ripples. The primary benefits of the DCM procedure are low diode reverse recovery and zero turn-on loss. The main switch has been switched off twice or higher the load current, which raises the turn-off loss of the DCM operation. It induces parasitic ringing of the current inductor [2] since the inductor oscillates during turning-off times with the system output capacitance. With all the side effects of DCM, efficiency can be affected. And if the lossless snubber capacitor may be applied across the switch to the soft turnoff, the energy contained in the capacitor has to be discharged before the system is triggered. Both turn-on, as well as turn-off soft-switching, is done.

Optimizing the DC-DC converter's design needs the optimal selection of various parameters to maximize performance and efficiency. Some of the parameters depend on load, components, temperature, and/or input/output voltage. The design of such parameters will increase the efficiency of the single design point for a particular load, input/output, component, and operating temperature, while not achieving maximum efficiency when the load varies. Due to the variations in temperature, operating points, and components [3]-[4], the line conditions do not ensure the improvement at that design phase. One significant parameter for a non-isolated converter that needs to be optimized is the switching frequency for improving light load efficiency.

The lower switching frequency dc-dc converter implies less switching loss. Switching loss is increased at high switching frequency as conduction loss rises at high load current. Increased efficiency is important in all operating conditions, in particular in light loading conditions, for ensuring an improved battery life as well as energy savings [3-6]. The [5] and [6] approaches that non-linearly vary the switching frequency by regulating the peak inductance current, to increase efficiency at light load when preserving output.

The algorithm proposed was applied using fixed-step-size functions in previous works [8]-[9], which includes increasing and decreasing the auto-tuned variable value. In such cases, the designer must select either a smaller step-size (both of which the hardware resolution is limited) resulting in long conversion time to achieve the value of optimum parameter but have greater precision, or a larger step-size which results in less convergence duration to achieve the value of optimum parameter but have less accuracy. For an auto-tuned power controller, the convergence rate is significant since it must be compatible with variations that result in an optimal new value of a parameter and it influences the efficiency of conversion over a span in different conditions. Convergence speed must be increased, but accuracy and reliability should be maintained.

In discontinuous mode, the ZVS ("Zero-Voltage Switching") state is attained. The efficiency improvement is obtained only on the CCM-DCM boundary state. When the converter is operated in CCM mode ("Continuous Conduction Mode"), the switching losses are increased whereas the high frequency switching current ripples rise during DCM mode ("Discontinuous Conduction Mode"). The converter is worked on the boundary of CCM-DCM to remove the current ripple as well as switching loss affects the from the converter.

In this article, the adaptive digital loop controller is introduced for optimization and adjustment of the converter switching frequency automatically over different operational conditions This automated controller constantly controls the maximum performance point through nonlinear adjustment of the switching frequency. This frequency has been varied as per the load current. An AFO adjusts the switching frequency to minimize the overall conduction as well as switching losses and this leads to obtaining greater power conversion efficiency. The switching frequency range is maintained at kHz, otherwise, the converter switches on two or three different frequencies to prevent problems of limit cycle oscillation. The complexities of a slower convergence rate are therefore eliminated in the suggested closed-loop controller. This is carried out on an inexpensive microcontroller. MATLAB simulation presents the dynamic performance and the 100W laboratory prototype is verified.

II. EFFICIENT DC-DC CONVERTER

A. Proposed Topology

Figure 1(a) indicates the simple non-isolated dc-dc converter. S_1 is the primary switch on the buck converter, S_2 is the synchronous rectifier (SR-MOSFET). It is the most basic non-isolated DC-DC converter topology, however, unfortunately, when it operates at CCM-DCM boundary in high voltage applications, it is suffering from reverse-recovery SR-MOSFET body diode problem [10]. This triggers the problems of very high voltage and current surges, switching losses, and EMI (electromagnetic interference) noises. An appropriate solution is to substitute the MOSFET by integrating a switch, as illustrated in Fig. 1(b), to solve the reverse-recovery problem. For example, the Schottky D_1 diode is used in series S_1 to avoid the body's diode from driving the S_1 and the D_3 diode in parallel to that of the S_1 to freewheel the current with better reverse recovery characteristics. This means that the body diode MOSFET is not forced into conduction. The freewheel current is controlled by a fast recovery diode that removes the shoot loss problem.

B. *Effect of Switching frequency on losses*

There are two kinds of losses in MOSFET: conduction loss that is the load current function and switching loss which is the switching frequency function. The switching loss relies on the switching frequency of the switch (f_{sw}) and junction capacitance (C) of the switch. The conduction power loss is the resistive parasitic function (R) in the power converter component as well as a trace. These are a rms current function in a power converter with square values (I^2_{rms}) in various branches. Because in every component, the current waveform shape is different. Every component also has a different resistive parasitic value. The power loss of the gate drive is due to the consumption of power to drive every MOSFET gate. This is based on V_g (gate-driven voltage), f_{sw} (switching frequency), and MOSFET gate charge value (Q_g).

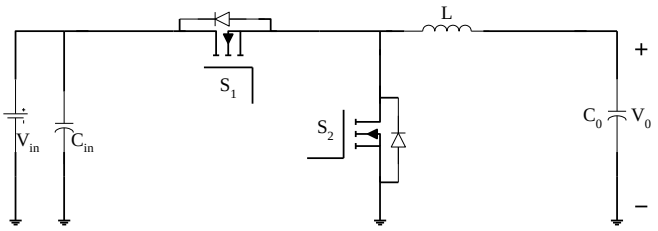


Fig. 1 (a) : Non-isolated dc-dc buck converter

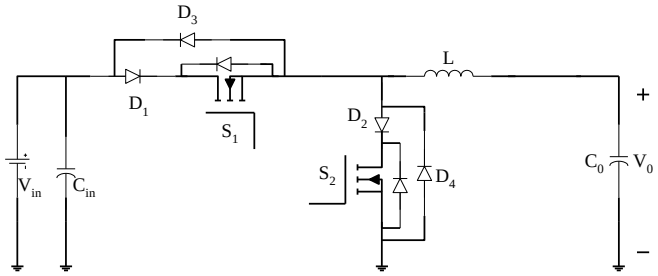


Fig. 1(b) : An enhanced non-isolated DC-DC buck converter

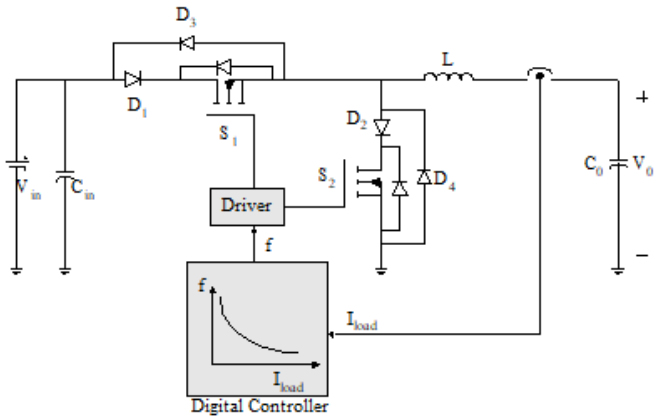


Fig. 1 (c) :Digital controller non-isolated dc-dc buck converter

MOSFET's power losses are defined as given below:

$$P_{driving} = V_g \times I_g \times f_{sw} \quad (1)$$

$$P_{conduction} = I_{rms}^2 \times R_{ds\_on} \quad (2)$$

$$P_{switching} = f_{sw} \times C \times V_g{}^2 \times I_{rms} \quad (3)$$

In the power converter, higher switching frequency offer fewer rms current and thus leads to fewer conduction losses. However, switching as well as gate-driven power losses are risen because of the higher switching frequency. In the lower switching frequency, the reverse behavior is seen. The optimal switching frequency value causes low total loss when one loss increases and other decreases with the variations in switching frequency.

The optimized switching frequency, which results in the least overall conduction as well as switching losses, is linked to several non-linear variables which distinguish f_{swo} ("Optimized switching frequency") under various conditions. To monitor the optimum switching frequency, a digital controller can be used that adapts f_{sw} in the range depending on variations of certain non-linear parameters.

C. Inductor Selection

The lowest inductance has been measured so the converter can be operated at the boundary of DCM mode and CCM mode [11]. The relation between I_{peak} (inductor peak current), I_{min} minimum current, as well as I_{rms} inductor rms current ("Root Mean Square") is represented in (4)-(9), where the load current is I_{load}, the switching period is T_{sw}, load power is P, and inductor current ripples are ΔI.

$$\Delta I = \frac{1}{2}.\frac{V_{in} - V_o}{L}.\frac{V_o}{V_{in}}.T_{sw} \quad (4)$$

$$I_{load} = \frac{P}{V_o} \quad (5)$$

$$I_{peak} = I_{load} + \Delta I \quad (6)$$

$$I_{\min} = I_{load} - \Delta I \quad (7)$$

$$I_{rms} = \sqrt{I_{load}^2 + \frac{\Delta I^2}{3}} \quad (8)$$

For the critical inductance value, I_{min} is reduced to zero. The critical inductance value enables the converter to operate between the CCM and DCM boundary conditions.

$$L_{crit} = \frac{R(1-D).T_{sw}}{2} \quad (9)$$

$$f_{sw} = \frac{(1-D)V_{out}}{2LI_{load}} \quad (10)$$

It is obvious from equation (10), that the switching frequency is inverse in relation to load current. To get optimized switching frequency of a certain load current value a non-linear correlation between load current & switching frequency is established and it is given as:

$$f_{sw} = k \times I_{load}^{-\alpha} \quad (11)$$

For device parameters defined in Table II where k=19394, α =1.045.

Fig. 2 indicates an optimized switching frequency for various loads with maximum efficiency. The non-linear relationship was given in eq. (11) which was driven by eq. (10). Load current versus switching frequency has one local lowest which is attained at the boundary condition of CCM-DCM. Taking the differentiation in equation (10) with respect to load current to achieve the local minimum for an optimum switching frequency. Thus, the value of optimal switching for the load current is evaluated.

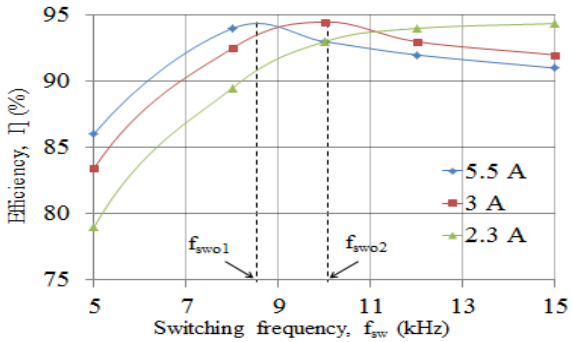


Fig. 2 : Optimized switching frequency for different loads with peak efficiency

III. CONTROL ALGORITHM

A. Traditional Control Schemes and its Drawbacks

The traditional control has used functions of fixed-step-size as defined in [3] and [4] to implement the algorithms. With a fixed-step-size function, optimum parameter variance is not practical. The parameter value is either higher or lower than the optimal value. Furthermore, for the auto-tuned power controller, the convergence speed is also significant as it must be compatible with the variations that lead to a new parameter optimum value. This also influences the efficiency of the power conversion in various conditions over the duration of converter operation. Therefore, the designer should choose a large step size that will affect the switching frequency for a short convergence duration. Larger step sizes give the optimized switching frequency with less accuracy. To improve the convergence speed while maintaining acceptable reliability and accuracy, the controller needs to be calibrated. The variable switching frequency was used in past as the synchronous buck converter, which varies at all times based on load current in the DCM. Though, DCM induces a higher frequency switching current ripples that decrease the efficiency of the DC-DC converter in a single phase.

B. Proposed Control Scheme

Implementing the synchronous buck converter in the suggested control scheme at the CCM-DCM boundary state. The boundary operation removes the ripple content that was caused by the DCM operation. Whenever the nonlinear parameter variation occurs, this digital controller adapts f_{sw}. In a non-linear variation of the switching frequency that varies depending on the load current, the optimal switching frequency is continuously monitored. Fig. 3 presents the AFO algorithm implementation flowchart. The algorithm will be enabled periodically or run between iterations constantly with precise delay. N samples I_{load}, which are stored as well as averaged to produce I_{load} (n), are recorded by ADC ("Analog to Digital Converter"). The load current is inversely related to switching frequency, so I_{load} can be employed to evaluate the optimum efficiency of the adaptive loop switching frequency of the digital controller. The load current versus switching frequency has a local minimum to be achieved on the CCM-DCM boundary condition. Certain variables such as I_{ll}, ΔI, f_{min}, I_{ul}, f_{max} are initialized by an AFO program. The initial switching frequency and load current values are saved in f_{old} and I_{old} temporary variables. These variables often substitute the newly modified values for their values. The newly updated switching frequency and load current values are saved into f_{old} and I_{old} variables that substitute the previous initial values during an AFO algorithm operation. The latest sensed value would be verified at first, then at the same time below the upper limit value is greater when compared with initial value. The initial switching frequency is reduced by Δf whereas the initial load current is improved by ΔI when the requirement is fulfilled. Now, the new switching frequency values, and load current, will be saved in f_{old} and $I_{old.}$ After updating the switching frequency and load current values, the check has been made again. Until the condition is violated, it exists in the same loop. The control is entered into the second loop when the first loop exits. It then confirms that the load current is below I_{old} as well as above the lower limit value. The switching frequency is enhanced by Δf whereas the load current is fallen by ΔI when the requirement is fulfilled. Such recently modified values are saved in f_{old} & I_{old} until this operation is conducted. The loop is continued until some condition has been violated. Then the control examines whether the modified switching frequency exceeds the lower or upper limits. If the updated switching frequency reaches any limit, then lower or upper switching frequency is used directly to optimize switching frequency. The I_{load} is then replicated and the AFO process repeats after many (M) switching cycles (sufficient to reach a stable state).

A non-linear correlation is formed between f_{sw} (switching frequency) and I_{load} (load current) and defined in eq (11). This means that the fixed step-size of the load current & switching frequency remained unchanged, but it varies non-linearly. Such modified variables Δf and ΔI are non-linear. Because of a non-linear deviation, the optimized switching frequency may be achieved over a short convergence duration. If there are variations in line, then the load current will be affected by these variations, and the resultant average load current is the basis of the following iterative decision (increasing or decreasing) of the AFO controller.

IV. PERFORMANCE OF THE CONVERTER

Fig. 4 illustrates a digitally controlled buck converter's block diagram. The suggested auto-tuned controller has been employed to control the optimal switching frequency for peak efficiency as per the load current. In this suggested controller, the upper and lower limits of the switching frequency are set to protect the converter against disruption. For marginal changes in the load current, the least changes in the switching frequency are determined and the incremented/decremented function needed to update the switching frequency is thus evaluated. This is a non-linear incremented/decremented function that gives the optimized switching frequency. The correlation between load current and performance is drawn for separate switching frequency values. The maximum performance is found in the CCM-DCM limit condition after examination of the graphical plots with different switching frequency values.

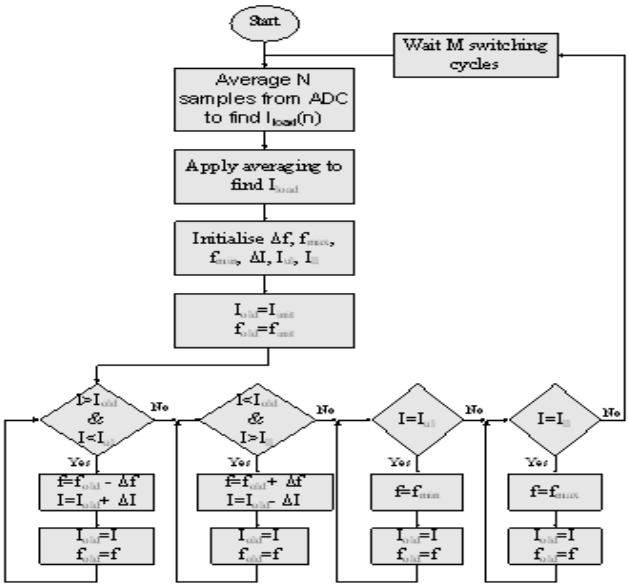


Fig. 3 : Proposed AFO controller flowchart

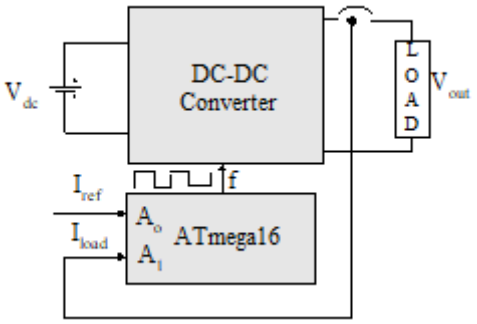


Fig. 4 : Digitally controlled Buck Converter Block Diagram

In both CCM-DCM modes, efficiency is reduced. Therefore, an association between switching frequency & load current is formed to work the DC-DC converter at the boundary. The efficiency point would also be changed if the load current shifts from its preceding value. If the system's switching frequency is maintained constant, efficiency would degrade for a new current value. This frequency needs to be adjusted accordingly to keep the efficiency stable. The maximum efficiency point with the latest current value now is shifted from curve to curve. Therefore, by simply varying the switching frequency, the maximum efficiency can be kept stable.

The previous value of load current will be compared with the value of the sensor in the suggested controller. If the sensed value exceeds the preceding value, the frequency of switching is reduced by Δf. The Δf function has been set to 1 unit. The value of the following iterative load current is determined based on the non-linear association between load current and switching frequency with a decreased frequency ($f_{old} = f_{old} - \Delta f$), then the

modified load current is subtracted from the preceding value of load current. Used to obtain a new current value, ΔI is derived following deduction. To obtain a new current value for the next contrast, the value of ΔI is added to the old load current value. Now, this new value of current is comparable to the sensed value again. If the value of the new current is higher, the condition will be violated and out of the loop. The loop persists if the condition is not violated. Once out of the loop, the previously updated loop value is evaluated again in a new decisive loop, where it is verified that the previously modified load current value is larger when compared with current sense. This loop performs the similar process until it violates the condition. When two loops have been compared, it examines if the switching frequency has gone beyond its lower/upper limits

A closed-loop synchronous buck converter simulates the effect of shifting in the switching frequency. The frequency varies between 1 kHz and 25 kHz in a digitally monitored buck converter. The value of inductance is set to 250μH for the simulation. The system has been configured so that it only works for a broad range of load variance on the limits of the CCM-DCM condition.

As depicted in Fig. 5(a) the inductor current simulated in steady-state with V_g (gate drive voltage). The inductive current is retained at the CCM-DCM boundary. At 0.5 The duty cycle is maintained. The duty cycle is kept constant, at varying loading conditions. The inductor current (I_L) and gate-source voltage (V_g) and the IL inductor current are seen in Fig. 5(a) with a 4 kHz switching frequency. Fig. 5(b) & Fig. 5(c) display the output voltage as well as inductor current variance under different conditions of load. The output voltage and inductive current can be seen for different load currents such as 2.3A, 3A, & 5.5A. The optimum switching frequency would be higher or lower based on the trade-off between the switching loss and the conduction loss. The complex voltage response, as well as inductor current, are often shown by a magnified vision. The dc-dc converter transient reaction is smooth since the inductor current flows in different loading conditions constantly. Without output variations in voltage, the DC-DC converter can work under different load currents.

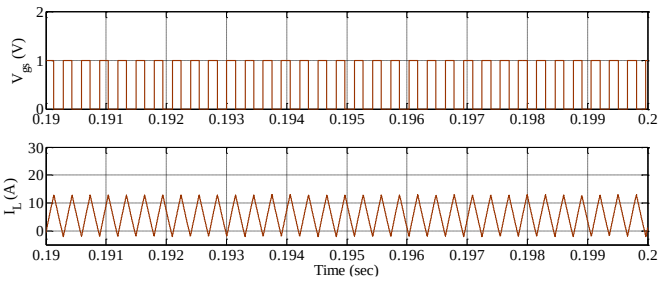


Fig. 5(a) : (i) V_g, (voltage of gate source) (ii) I_L, inductor current in steady-state

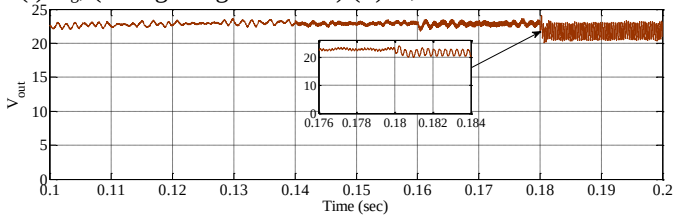


Fig. 5(b) : V_{out} of non-isolated DC-DC converter in dynamic state

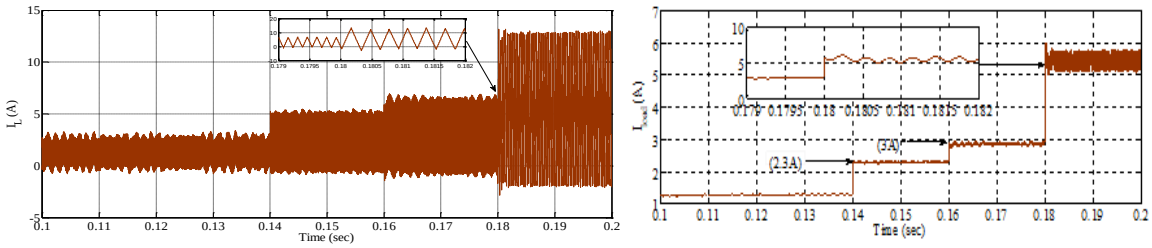


Fig. 5(c) : I_L inductor current variance in according to the load current

Fig. 5(d) : load current I_{load} variance under separate loading conditions (Extended vision for ripple content).

TABLE I. EFFICIENCY AND OPTIMUM SWITCHING FREQUENCY WITH DIFFERENT LOAD CURRENT AND

I_L/ Vin	1.0A		2.0A		3.0A	
	η (%)	$f_{optimum}$	η (%)	$f_{optimum}$	η (%)	$f_{optimum}$
40 V	95.06	19 kHz	95.89	11 kHz	94.98	7 kHz
50 V	94.83	18 kHz	94.89	9 kHz	94.91	6.8 kHz
60 V	94.75	16 kHz	94.50	8 kHz	95.03	6.2 kHz

TABLE II. DIFFERENT I/P VOLTAGE

TABLE III.

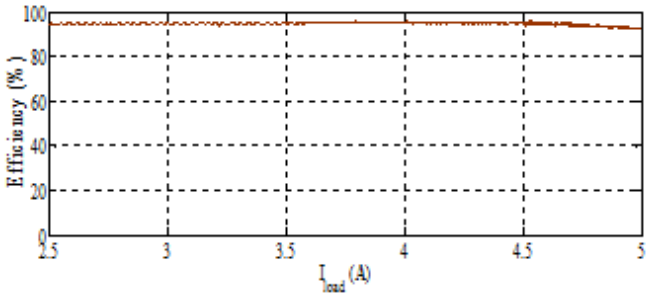


Fig. 6 : Efficiency vs load current curve with AFO

Table I shows how the suggested controller senses and adapts the new optimum switching frequency, and the I/P voltage for the load current 1, 2, and 3A varies between 40 and 60V. As the voltage of input differs depending on the trade-off between switching loss as well as conduction loss, the optimum switching frequency will be higher or lower.

By using the adaptive frequency optimization technique, the efficiency curve is shown in Figure 6 against load current. The efficiency of different load current values is determined using AFO. The efficiency is kept constant with respect to the current load value.

V. DESIGN AND HARDWARE IMPLEMENTATION

A. DC-DC Converter's design with a digital controller

In the configuration of the experimental power stage, there is a single step, buck dc-dc synchronous converter having 250µH of L_o (o/p inductance) having 102mΩ of DCR, 1000µF of input/output capacitor, Fast Recovery Diodes: MUR8100E, MOSFETs lower and upper switches: IRFP250. The inductor is constructed using the equations in (4)-(9) and determined the critical inductance value which enables it to work at the CCM-DCM boundary. The value of the inductor is optimized through the use of equations that satisfies the switches with satisfies the zero-voltage condition and the lowest volume.

B. Implementing the AFO algorithm using ATmega16

In a digital controller, AFO approaches are prototyped for proof of concept. The AFO algorithm is used by a low-cost microcontroller in hardware. Fig. 3 shows the entire algorithm's flowchart. An AFO algorithm is implemented with the digital ATmega16 microcontroller.

TABLE II. CIRCUIT PARAMETERS OF DC-DC CONVERTER

Parameter	**Value**
Capacitor's ESR	0.2Ω
Output Capacitance (C_{out})	1000 µF, 200V
Input Capacitance (C_{in})	1000 µF, 200V
Inductor Resistance	0.102 Ω
Inductor Inductance(L)	250 µH

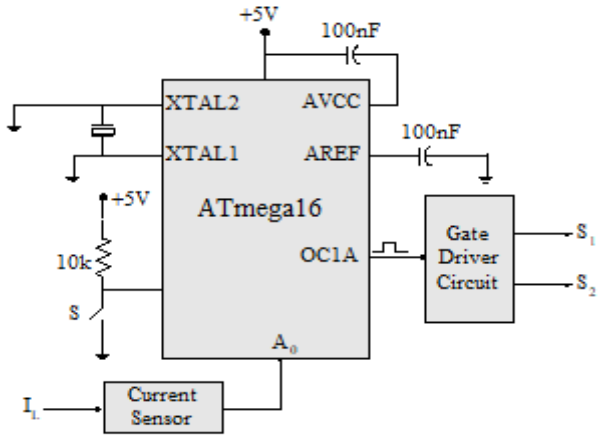


Fig. 7 : Implementing the AFO Algorithm using ATmega16 microcontroller

A 10-bit ADC is used to detect input current through the WCS2705 current sensor. By using a digital controller, converted data has been processed and is used by the AFO algorithm.

Fig. 7 shows AFO Algorithm Implementation by microcontroller ATmega16. There is a 10-bit ADC in ATmega16. The current sensor output voltage is encoded into binary data. Data obtained in two Special Registers, namely ADCL (results in A/D low) and ADCH (results in A/D high), following the binary conversion. ADC's V_{ref} is connected with the 5V and the analog ADC circuitry is supplied with AVCC pin in a 10-bit ADC. To achieve greater accuracy AVR ADC, the AVCC pin must be supplied with a stable voltage source. The V_{ref} has become more stable and the ADC precision is improved by adding a capacitor between the GND and AVREF pin. The conversion time will be determined by the crystal-related frequency between XTAL1 as well as XTAL2 (F_{osc}) pins and ADPS0:2 bits. If an ADC channel is chosen, the ADC gives the sample and hold capacitor (C hold) some time for charging to the input voltage level of the channel. On each conversion, the AVR requires 25 ADC clock cycles and 13 ADC clock cycles. The A/D has a resolution of 10-bit at 1024 steps maximum. The size of the step will be 5/1024=4.883mV if the internal reference voltage is set to 5V. The current sensor circuit provides the microcontroller with its measurement. In the feedback process, the new WCS2705 sensor is used. The maximum pass current of this sensor is 8A and the sensitivity is 255mV/A. The application of the current passing through the conduction path produces a magnetic field that is sensed and transformed into a proportional voltage in the integral hall IC. A dc $V_{dd}/2$ offset is given by WCS2705. So, if the current sensor detects 1A current, the sensor generates a 255mV+2.56V ($V_{dd}/2$) voltage of sensor = 2.815V. Likewise, 3.07V is produced from the sensor after sensing 2A current. The actual current load value is, therefore, compare to the set point in an algorithm. The output voltage of the sensor is therefore converted again into the value of the old load current.

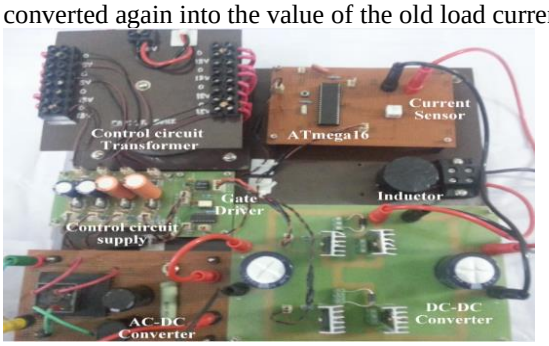


Fig. 8 : A prototype of 100-W effective DC-DC converter with optimized switching control

To achieve 1A load current, 2.815V will be multiplied by 3.855 and deducted by 9.80. To make a comparison in the suggested algorithm, a load current of 1A is given with these arithmetic calculations.

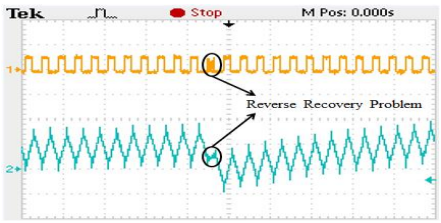
C. Current Sensor Circuit and Low Pass Filter

ADC0 pin of 8 channel ADC attaches the current sensor voltage output. A Zener diode and an LPF are developed to decrease the noise and overvoltage of the current sensor output voltage. To eliminate a high-frequency noise from the ADC input signal, a low pass filter has been developed.

$$f = \frac{1}{2\Pi RC} = \frac{1}{2\Pi \times 100 \times 10^{3} \times 1 \times 10^{-6}}$$

$$f = 1.5915\,\text{Hz} \qquad (12)$$

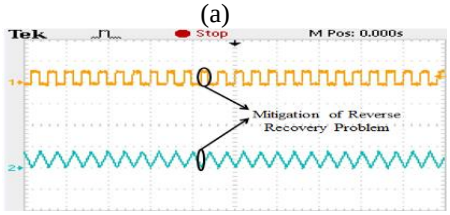
This cut-off frequency is used to design a low-pass filter. The frequencies lie above 1.5915 Hz will be eliminated by cut-off frequency. A Zener diode of 7.5 V is used to avoid overvoltage in input on the ADC channel parallel to the film capacitor (used for low-pass filter). The channel is preferred in the A/D converter by setting up the ADMUX register with the MUX0-MUX4 bits. The ADC can be enabled/disabled by setting/clearing the ADCSRA (bit ADEN in ADC & Status Register A). For higher accuracy, the ADC conversion is performed 8 times. The average of these 8 specimens is then accumulated. The variation of the switching frequency spectrum is from 1 to 25 kHz. The photograph with optimized switching control demonstrates in Fig.8 the 100W effective dc-dc converter. Fig. 9 (a) demonstrates the reversal recovery issue of the current inductor waveform. Fig. 9(b) shows by using fast Recovery and Schottky diode, issue of reverse recovery also mitigated. The problem is that the body diode of the semiconductor switch slowly recovers in reversal recovery time. The body diode of MOSFET IRFP250 is 650ns in reverse recovery time, and the dead time of the gate driver is 750ns. The circuit of the gate driver includes driver IC 2111, opt-isolator, and buffer. IR 2111 has a dead band of 750ns. If one MOSFET's body diode is triggered by switching on the opposite unit, a "short circuit" causes that is close to the shoot-through conditions.



.

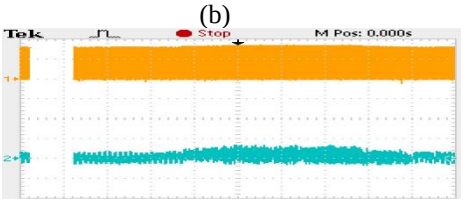
(Y-axis: 25V/div & 1A/div, X-axis: 100µs/div)

(a)



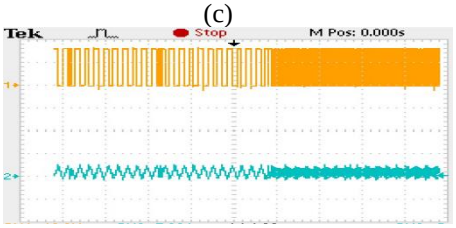
(Y-axis: 25V/div and 1A/div, X-axis: 100µs/div)

(b)



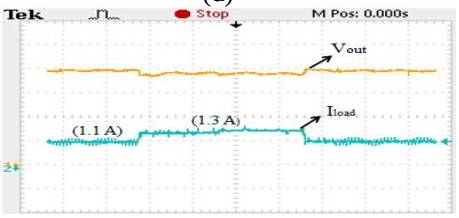
(Y-axis: 10V/div and 5A/div, X-axis: 1s/div)

(c)



(Y-axis: 10V/div & 5A/div, X-axis: 1s/div)

(d)



(Y-axis: 10V/div and 1A/div, X-axis: 1s/div)

(e)

Fig. 9 : Experimental waveforms: (a) I_L (inductor current) while reversal recovery problem, (b) I_L (inductor current) when reversal recovery problem is mitigated, (c) I_L (inductor current) under dynamic condition, (d) I_L (inductor current) under dynamic conditions (in magnified view), (e) output voltage and output current under dynamic conditions

TABLE III. EFFICIENCY AND OPTIMUM SWITCHING FREQUENCY WITH DIFFERENT LOAD CURRENT AND DIFFERENT INPUT VOLTAGES

Vin=40V			**Vin=50V**		
$f_{optimum}$	**I_{load}**	**η (%)**	**$f_{optimum}$**	**I_{load}**	**η (%)**
24.05 kHz	0.6 A	92.5	17.14 kHz	0.9A	92.71
19.25 kHz	0.8 A	92.40	14.30 kHz	1.1A	92.37
14.61 kHz	1.1 A	91.05	11.05 kHz	1.3A	91.02

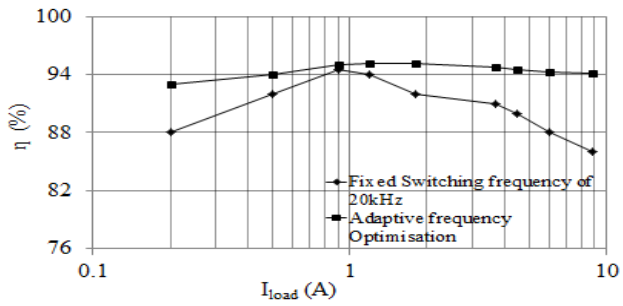


Fig. 10 :Experimental efficiency vs load current with AFO algorithm correlated with fixed switching frequency operation

For the proposed controller, fig. 9(c) and (d) indicate experimental outputs. The current waveform of the inductor is dynamically presented. Fig. 9(c) indicates the variation of inductor current if the switching frequency is varied by a proposed controller from 14.30 to 11.05 kHz for an input voltage of 50V. For load currents 1.3A, the optimum switching frequency is 11.05 kHz as shown in Fig. 9(c). For load currents 1.1A, the optimum switching frequency is 14.30 kHz. Fig. 9(d) displays the dynamic output voltage waveform (in the magnified form) when the load current has been modified stepwise.

Table III illustrates the optimal switching frequency at separate load currents and input voltage. For load currents 0.6A to 1.3A, the input voltage varies between 40 and 50V. The correlation between AFO and the experimental efficiency curve of the fixed 20 kHz switching is shown in Fig. 10. There is only one local (i.e., maximum effectiveness point) for the fixed switching frequency, while the adaptive frequency optimization works for different frequencies to reach the maximum with any load current value.

VI. CONCLUSION

The load adaptive with high-efficiency dc-dc converter is introduced in the present paper. The working of this non-isolated converter is retained at the CCM-DCM boundary. It is accomplished by an adaptive switching optimization algorithm. The suggested algorithm prevents oscillations of the limit cycle with its peculiar auto-tuned capability. The variation in load current is examined as well as the optimum switching frequency is performed to keep efficiency well over 95 percent under variation in load as well as the input voltage. The enhanced converter's output shows that the variations in parameters allow convergence without shifting during retaining appropriate stability. Implementing the framework with a single current sensor on a low-cost microcontroller platform has many benefits. With the new topology, 100W prototype output fits the perfect configuration of a non-isolated dc-dc converter having no reversal recovery problem. This proposed DC-DC converter attains 95% efficiency with the 100W prototype at the lowest cost of the microcontroller

REFERENCES

1. F.Z. Peng, Li Hui, G. J. Su, and J. S. Lawler, "A new ZVS bidirectional DC-DC converter for fuel cell and battery application, "*IEEE Trans. Power Electron.,* Vol. 19, No.1, pp. 64-65, Jan. 2004.
2. X. Huang, X. Wang, T. Nergaard, J.-S. Lai, X. Xu, and L. Zu, "Parasitic ringing and design issues of digitally controlled high power interleaved boost converters," *IEEE Trans. Power Electron*., vol. 19, no. 5, pp. 1341-1352, Sep. 2004.
3. J. Abu-Qahouq, H. Mao, H. Al-Atrash, and I. Batarseh, "Maximum efficiency point tracking (MEPT) method and dead-time control," *IEEE Trans. Power Electron*., vol. 21, no. 5, pp. 1273-1281, Sep. 2006.
4. W. Al-Hoor, J. Abu-Qahouq, L. Huang, and I. Batarseh, "Adaptive variable switching frequency digital controller algorithm to optimize efficiency," in *Proc. IEEE Int. Symp. Circuits Syst*., 2007, pp. 781-784.
5. J. Abu-Qahouq and L. Huang, "Load Adaptive control scheme to improve converter efficiency and performance," in *Proc. IEEE Int. Symp. Circuits Syst.,* 2006, pp. 5051-5054.
6. J. A. Abu-Qahouq, O. Abdel-Rahman, L. Huang, and I. Batarseh, "On load adaptive control of voltage regulators for power managed loads: Control schemes to improve converter efficiency and performance," *IEEE Trans. Power Electron.,* vol. 22, no. 5, pp. 1806-1819, Sep.2007
7. W. Al-Hoor, J. Abu-Qahouq, L. Huang, and I. Batarseh, "Design considerations and dynamic technique for digitally controlled variable frequency DC-DC converter," in *Proc. IEEE Power Electron. Spec. Conf. (PESC 2007)*, pp.846-850.
8. J. Klien, "Synchronous buck MOSFET loss calculations with Excel model," Fairchild Semiconductor Application Notes AN-6005, 2006
9. S. Chattopadhyay, "Analysis of limit cycle oscillations in digital current-mode control," *IEEE Applied Power Electronics Conference*, pp. 7, March 2006.
10. C. Yang, H.-F. Xiao and S.-J. Xie, "An improved two-switch buck-boost converter with reduced reverse-recovery losses," presented at the IEEE Energy Convers. Congr.Expo., Atlanta, GA, 2010, pp. 1959-1964.
11. J. Zhang, J. Lai, R. Kim, and W. Yu, "High-power density design of a soft switching high-power bidirectional dc-dc converter," *IEEE Trans. Power Electron.,* vol. 22, no. 4, pp. 1145-1153, Jul. 2007.
12. Jaber Abu-Qahouq, Lilly Huang, Osama Abdel-Rahman, and Issa Batarseh, "Analysis and Experimental Results of Load Adaptive Voltage Regulator for Battery Powered Applications Society 41st Annual Meeting, IAS'2006, October 2006.
13. M. Pahlevaninezhan, P. Das, J. Drobnik, P. K. Jain, A. Bakhshai, "A New Control Approach Based on The Differential Flatness Theory for an AC/DC Converter Used in Electric Vehicles," *IEEE Trans. Power Electron.,* Vol. 27, No.4, pp. 2085-2103, Apr.2012.

14. M. Rais and J. Zbib, "Synchronous buck converter with increased efficiency" in *Proc. Annu. IEEE Applied Power Electronic Conf. (APEC)*, Feb. 2007, pp.714-718.
15. Xi Chen, Issa Batarseh, "Variable Step-Size Switching Frequency Modulation for Synchronous Buck Converter, "*IECON 2018-44th Annual Conference of the IEEE Industrial Electronics Society*., vol. 18, No.2, pp. 88-92, Oct. 2018.
16. Xi Chen, Anirudh Pise, Issa Batarseh, John Elmes, "A New Maximum Efficiency Point Tracking Technique for Digital Power Converter with Dual Parameters Control," *IEEE Energy Conversion Congress and Exposition.,* vol. 23, no.6, pp. 167-175, Dec.2018.
17. Praful V. Nandankar, M.V. Aware, "High efficiency discontinouous mode interleaved multiphase bidirectional dc-dc converter," *IEEE International Conference on Power Electronics, Drives and Energy Systems.,* vol. 28, no.8, pp. 123-128, Dec.2012
18. Praful V. Nandankar, Prashant P. Bedekar, Prashantkumar V. Dhawas, "Variable Switching Frequency for Synchronous Buck Converter," *5th IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE).,* vol. 45, no.12, pp.341-346, Dec.2021.
19. Praful V. Nandankar, Prashant P. Bedekar, Prashantkumar V. Dhawas, "Efficient DC-DC Converter Using Variable Switching Frequency Digital Controller," *5th IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE).,* vol. 45, no.15, pp.375-380, Dec.2021.