Study of Memory Cell Architectures in QCA Technology

Sushmitha yadav[a], Neeraj Kumar Misra*[b], Anil Kumar Sahu[c], Sankit R Kassa[d]

[a,b,c]Department of Electronics and Communication Engineering, Bharat Institute of Engineering and Technology, Hyderabad, India (ORCID:0000-0002-7907-0276)
[d]Department of Electronics and Communication Engineering, SNDT Womens University, Mumbai, India
Corresponding author Email id: neeraj.mishra3@gmail.com

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Abstract: CMOS technology is experiencing power dissipation, short channel effects and quantum effects problems with its relation to chip size, which makes it too hard for integrating more transistors, reaching its scaling limits. Quantum Dot Cellular Automata (QCA) is one of emerging nanotechnologies in recent times to overcome this flaw. The QCA technology is used for designing and implementation of digital circuits efficiently due to its features like smaller feature size, high speed, low power dissipation and high switching frequency. These characteristics prompt memory cell architecture and implementation in QCA as an appealing choice for manufacturing storage devices. This paper discusses architectures of several line and loop based memory cells to compare in terms of density, low power, complexity and switching frequency and to deduce an architecture method which is significant for designing memory cells

Keywords: Quantum Dot Cellular Automata, memory cell, architecture, density, complexity, low power

1. Introduction

In CMOS computing components are becoming smaller in size based on the Moore's law. This has caused CMOS based computing devices to experience several limitations (Misra et al., 2014). Some of important CMOS limitations are high power consumption, interconnection effects, short channel effects, fabrication difficulties and its high cost as a result of CMOS devices, high performance capability and device density which is making difficulties for CMOS technology advancement (Bhoi et al., 2021).

A new alternative paradigm for conventional CMOS technology in nanotechnology called QCA technology has emerged which overcomes flaws which are experienced with CMOS technology (Misra et al., 2015). The QCA technology used quantum cells, which makes it reversible in nature and has a relatively small feature size, low power dissipation and low delay compared to conventional CMOS (Bhoi et al., 2017).

The QCA technology features are very suitable for implantation of memory cells, while designing QCA memory cell architecture, important issue to consider is switching frequency and feedback paths so that so that arrangement of clocking zones are accurate in order for correct operation by means of pipelining (Frost et al., 2002).

Memory architecture, designing in QCA technology cannot be done similar to that of CMOS technology due to QCA's unique characteristics like the placement of the cells, clocking need to be considered so that memory is always in movement.

In this paper, our objective is to discuss and study memory architectures, which are broadly based on the prior line based and loop based memory cell designs, then discuss both line and loop based memory designs for their characteristics like density, low power, design complexity and latency. Lastly, we conclude why loop based architecture design approach of memory cells is suitable.

The paper organization is as follows. Section II briefly discusses fundamentals of QCA technology such as QCA cells, clocking schemes of QCA, and basic QCA gates and memory in motion. Section III discusses existing line and loop based memory cell architectures.

2. Fundamental of QCA Technology

2.1. QCA Cell

A QCA cell consists of four quantum dots placed at each of four corners of a square shaped cell as shown in Figure 1. Two electrons can move diagonally in between any two quantum dots due to coulombs interaction. Based on the position of electrons, polarization of the QCA cell is determined. There are only two possible states of a QCA cell based on polarizations -1 and +1. The QCA cell is in state low or logic '0', if electrons are diagonally arranged on the left side of a QCA cell, then the polarization of the cell is considered to be -1. The QCA cell is in state high or logic '1', if electrons are diagonally arranged on the right side of a QCA cell then polarization is cell is considered to be +1.

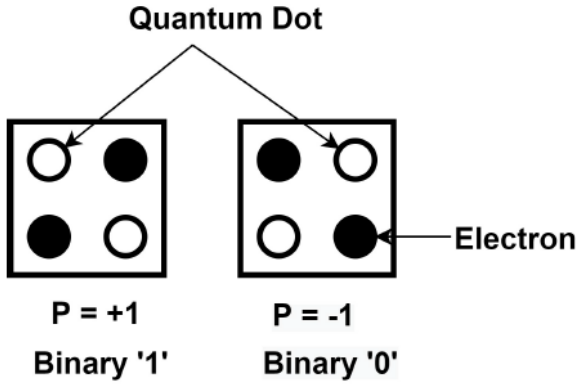


Figure 1. QCA Cell and its Polarization

2.2. Clocking Scheme in QCA

Clocking of cells in QCA technology is vital during the implementation of any circuit in order to synchronize and switching states or phases of cells for the data to flow correctly. There are four clocks shown in Figure 2, which can be applied during implementation where each clock is in phase difference of 90 degrees.

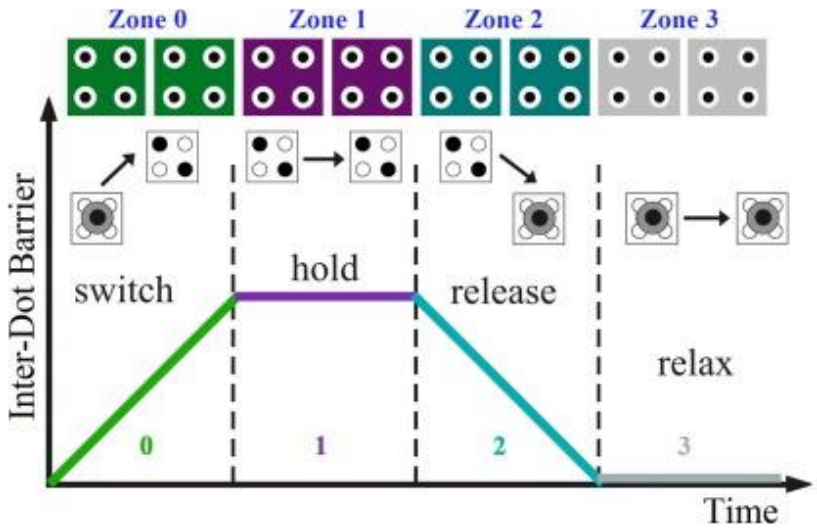
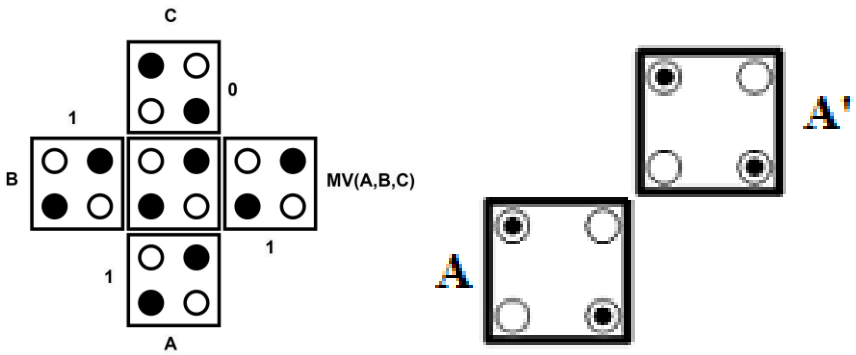


Figure 2. Clocking Schemes in QCA

2.3. Basic QCA Gates

The basic QCA gates are inverter and majority gates, which are vital components during designing. The majority gate consists of five QCA cells shown in Figure 3a, where middle cell is a driver cell. It has three input cells and one output cell. The output of majority gate is majority states of its input value. By changing any one of input majority gates to polarization -1, an AND gate is realized. Similarly, if any one of input of majority gate is fixed as polarization +1, an OR gate is realized.

A QCA inverter has QCA wire which is broken in such way they are parallel to each other as in Figure 3b. The last cell is of opposite polarization of that of first cell due to coulomb attraction force.



(a) (b)

Figure 3. Basic QCA gates (a) Majority gate, (b) Inverter

3. QCA Memory Cell Architecture Review

For QCA technology memory implementation, the memory should always be in motion. The memory cells are connected as a loop, the memory should move continuously through these cells. The loop is divided into all four clock zones to hold information shown in Figure 4b. Memory architecture can employ serial or parallel process (Frost et al., 2002)

In QCA technology, memory cell design to keep memory in motion has broadly two architectural approaches, namely line based and loop based shown in Figure 4 presented in (Heikalabad et al., 2016). Below we review how data movement is maintained, clocking employed and operation of several memory cells based on line (Figure 4a) and loop based architectural approach (Figure 4b).

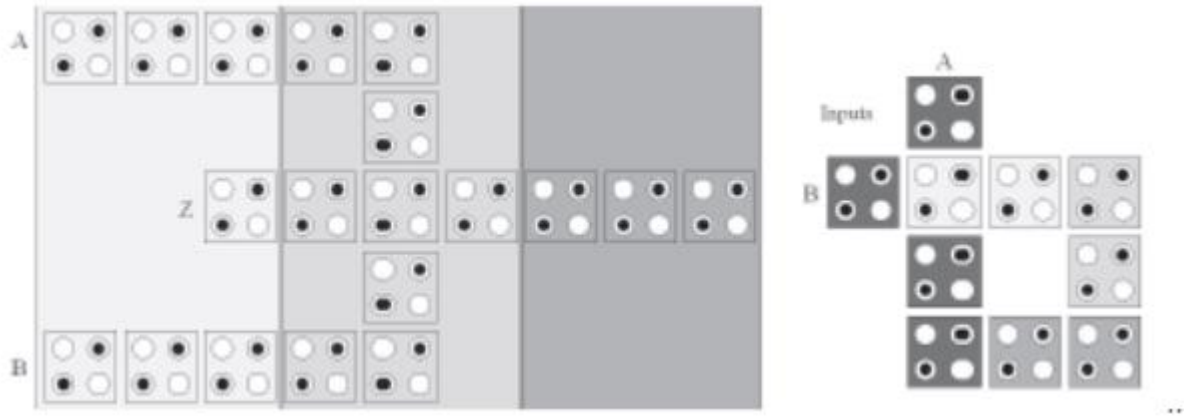


Figure.4. QCA Memory cells (a) Line based, (b) Loop based

3.1. Line Based Approach of Memory Cells

Types of approach for designing of memory cells are reviewed below. Line based approach needs to have a QCA wire with a clocking technique so that data needs to propagate back and forth.

In (Vankamamidi et al., 2005a), used parallel memory architecture and topology is based on two lines. So, it has advantages over (Vankamamidi et al., 2005b), as there is no delay for a bit to read or write since only one bit is stored in each memory cell. This helps in reduction of delay and clock cycles compared to serial memory architecture. A basic bidirectional line is used for storing of memory data, data is moved along this line back and forth. Read or write of data is done in four process steps, hence it employed three clock cycles for implementation of memory cells. To make a memory in motion on the line, two more clock cycles are used to relax and hold for adiabatic switching.

A two phase clock cycle is used by this memory cell in (Taskin et al., 2006), which is used for synchronization. A bi-directional line is used for rotation of stored data and uses a parallel memory architecture. Only one clock generator is used for generating two clock cycles. An advanced two phase parallel architecture is presented in (Taskin et al., 2008). This architecture has a majority gate at core of memory cells. Depending on memory operation, it can act as a majority gate or as a memory line.

In (Song et al., 2020) is a serial process, so many bits are stored in each memory cell. So, the delay depends on the number of bits present in memory cell when it needs to perform read or write operation. It requires dual level clocking across three memory tiles (which were presented) for input, loop and output. Thus, each memory tile has three clock cycles. Memory cells and memory line share same clocking zones irrespective of its word size.

3.2. Loop Based Approach of Memory Cells

In (Berzon et al., 1999) presented a memory cell implementation done using a SQUARES formalism for the address circuit logic realization components. A majority gate acts as SRAM is used as for realizing write logic to the loop. A shift closed loop is implemented based on SQUARES which employs four clocking zones. The loop output is pipelined to shift register. To load register, read signal is required and specified bit is written on output bit line. The shift, loop holds the data for all counter cycles. A series of the XNOR gates are used in array for implementing comparator circuitry. As all bits stored use the same read or write circuit, delay is same as that of bits stored. Additionally, density is more, using lots of clock cycles.

In (Vankamamidi et al., 2005b), a RAM memory cell using QCA technology is presented. The individual single layer RAM cell has read or write circuitry. By using a memory loop, data is stored. When read or write line are polarized to 1, input enters the loop and continuously circulates. If read or write line is polarized to 0, data in a loop are given to output. To achieve read or write circuitry AND, OR and inverter gates is used, making design simple. A total of 158 cells is utilized for memory cell layout. To design a more bit RAM. The memory can hold more than two bits if we employ parallel process architecture.

In (Dehkordi et al., 2011) presents two memory cells modified using the inherent capabilities of QCA. The programming of majority gate and clocking techniques are employed for circuitry design. Firstly discussed memory cell is based on S- R latch design which forms a memory loop for holding data. Memory cell utilizes 100 cells with seven clocking zones and over all delay of 4 clock cycles to implement RAM cell circuitry. In second memory cell is based on D latch. D latch is a memory loop which holds data which is used in RAM cell designing. The RAM cell uses a total of 63 cells, but utilizes 12 clock zones, making the overall delay of RAM cell to 4 clock cycles. In (Hashemi et al., 2012) presents a novel memory cell with set/ reset capability. The D flip flop is level and edge triggered is introduced which is used as a storage memory loop for RAM cell circuitry. Set/reset is used to activate the memory cell. A 2:1 multiplexer which is presented, is also used for realizing memory circuitry. Total 109 cells are used to realize D flip flop based memory cell with a delay of 1.75 clock cycles.

In (Angizi et al., 2015), D latch is realized using a majority gate, which is presented. This Majority gate acting as D latch is used in realizing RAM cell. This design is simple and has improved in the area, but is has low speed computation.

In (Fam et al., 2019), a D latch using the advanced clocking mechanism is presented which used as a memory loop in realizing RAM cell of a single layer. It has simple design for read or write circuitry with total utilization of 55 cells and delay of 2.5 clock cycles.

In (Heikalabad et al., 2016) presents a five input minority gate, which is used in the comparison circuitry in CAM cell. A S-R latch memory loop is also employed for storing memory in read or write circuitry of CAM cell. This design uses 100 cells for design of CAM cell and delay of 2 clock cycles making it more speed operation. The (Khosroshahy et al., 2017) introduced a majority gate of five inputs which is used as a component in the comparison circuitry of the single layer CAM cell. This cell uses read or write circuitry same as that of (Fam et al., 2019), but is more area efficient.

In (Taskin et al., 2008), a low power XOR gate is presented which is used in the comparison circuitry in the CAM cell of a single layer. Additionally, read or write circuitry is reduced and has advanced clocking mechanism compared to prior works which has significantly less area and power.

In (Heydari et al., 2019) a set or rest RAM cell is presented. A majority gate of low power is presented which is used to set or reset RAM cell output. It has a considerable low area and delay with efficient switching energy. In (Heydari et al., 2019) and (Mubarakali et al., 2019) are RAM cell crossover structures, where (Mubarakali et al., 2019) uses an S-R latch based memory loop and (Sadoghifar et al., 2018) used novel D latch based memory loop. Both these memory cells have reduced wastage area, reduced cell count.

In (Song et al., 2020) presents an asynchronous RAM cell with set and reset capability. The set and reset of RAM cell are done by 2 to 1 multiplexer which is also presented. The proposed RAM cell is of multilayer structure with improved area and delay with efficient scalability.

4. Discussions

The line and loop based memory cell's architecture are discussed and compared in terms of density, low power, complexity and latency.

4.1. Latency

The clock zones for line based memory cell structures require additional clocking in order to facilitate flow of data through a QCA wire, and storing of data needs additional clocking zones making implementation of such memory cell complex. Whereas loop based memory cell structures use a feedback path loop though, where data is circulated and stored easily though there is difficulty in employing efficient clocking mechanisms. The loop based memory cell implementation is more preferred as it doesn't require additional clock zones. The delay of parallel memory cell architecture is less compared to serial memory cell architecture as in parallel only one bit is stored in memory loop, so during read or write operation there is no additional delay wherein in serial access, more bits stored in each memory cell which use shared read or write circuitry, making delay equal to that of word size in memory loop.

4.2. Density

The implementation of memory cell through feedback path has significantly reduced the number of cells as read or write circuitry plus a memory loop is included within same where data is continuously circulated. Additionally, novel components and techniques are introduced for read or write circuitry implementation using a feedback path like latches, multiplexers, decoders etc. Which further reduces wastage areas and size comparable to a line based memory cells where it requires additional clock generators decoders and read or write circuits individually. So, the size of memory loop implementation in loop based architecture is significantly less compared to that of line based design.

4.3. Low Power

The decreased number of clock zones and density in loop based architecture significantly yields low power dissipations. Low power components in recent times are used to implement a memory cell in feedback fashion which further decrease high power considerations. The line, based memory cells, though easy to design have additional cells, wastage areas, additional clocking doesn't yield an overall power efficiency.

4.4. Design, Complexity

The line, based memory cells are very simple to design and implement even if it has disadvantages in speed, power and size. There is little scope for advancement of line based memory cell techniques (Sodoghifar et al., 2018).

The loop based memory cell circuitry designing and implementation needs considerations in clocking and layout mechanisms as memory loop is significantly smaller in size thus raising difficulty and need for using efficient clock zones within that memory loop. The architectural layout is further needed to be researched and apply novel advanced design techniques to reduce wastage areas, gates and clocking. Research is thus needed to find efficient novel architectural design techniques and advanced novel clocking in order to implement efficient memory cells.

The loop based memory cells have an overall efficiency compared to line based memory cells, even if there is complexity in design of loop based memory cells. No advancement in research for line based memory cell designing techniques further make loop based memory cells more preferable.

5. Conclusion

There is a steady advancement in research of loop based memory cells where researchers are finding new techniques for designing and clocking in order to achieve efficient and better performed memory cells in terms of smaller density, low power and fast speed. The line, based memory cells wherein has little to no scope for further advancement and improvement of memory cells in order to yield a better performed memory cell.

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