FinFET based Add and Shift Multiplier for Wireless Communication

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Abstract: In this paper FinFET based low power multiplier for IOT applications is proposed. At present society is need of low power IOT devices such as Bluetooth, Wi-Fi, RFID and Zig-Bee to connect the things to real world. FinFET BSIM CMG model files for the feature size 7 nm, 10 nm, 16 nm and 20 nm are used to analyze FinFET based conventional multiplier using licensed SymicaDE software tool. Static and dynamic power dissipation is investigated for FinFET based conventional multiplier. As the technology node decreases simulation results proved that power dissipation of multiplier circuit reduces and its value is less compared to MOSFET based multiplier circuits. FinFET based Array multiplier, Vedic multiplier circuits. The proposed FinFET multiplier can be used for low power IOT devices such as wireless sensor networks and RFIDs which operates with low power batteries with more battery life.

Keywords: Low Power (LP), Internet of things (IOT), FinFET, Metal oxide semiconductor Field effect transistor (MOSFET), Complementary metal oxide semiconductor (CMOS).

1. Introduction

At present development of every section of society takes place with the usage of IOT technology is used in wide area of applications such as Embedded Systems, mobile computing, smart energy a, smart grid, smart health, smart transportation and smart environment requires devices and circuits which operate at low power (LP) design. Future technologies such as cloud computing, Fog computing, big data, distributed computing utilizing IOT technology need circuits which work on high secure, high speed, low area, low power. The high-performance circuits can be designed by using advanced devices such as FinFET compared to MOSFET. Low leakage power and miniaturization FinFET is considered as emerging transistor compared to MOSFET due to control of channel by the gates. Portability is an important aspect for IOT devices along with low battery power and high security. Portability is achieved by scaling of device. At reduced technology below 20 nm FinFET has less energy compared to other technology nodes which presented by Dinesh Kumar in research article [1]. At the technology node below 20 nm FinFET emerged as leading technology as it overcomes short channel effect compared to MOSFET [2]. Senthil Kumar in research article shown that and gates, Vedic multiplier designed by FinFET has low power compared to MOSFET [3].

In digital circuits such as CPU, multipliers are important component in which speed and power requirement is main concern. To reduce the power dissipation in multiplier switching activity has to reduced [4]. Many Researchers have done work to reduce the power dissipation for different multipliers [5]-[7]. Rajshree Shanmugam shown in research article on comparative analysis of various multipliers in that array Multiplier has more power and Baugh Woolley multiplier has low power and high speed [8] which was implemented in Xilinx ISE 8.1 for synthesis making used of VHDL programming. Large areas occupied by tree multipliers when used in high speed applications. Radix base multiplier such as carry select adder-based radix multiplier requires more transistors which consumes more power. Less area and simple in design is obtained by using multipliers based on radix and shift architecture [9]. Already authors have done research on conventional multiplier and BZFAD multiplier using 130 nm MOSFET CMOS technology [4]. The result showed BZFAD has less power compared to conventional at technology node 7 nm. Analysis of FinFET node from 20 nm to 7 nm which can be used for the design of FIR Filter for fabricating DSP processors which is used in many IOT applications such as wireless sensor networks, RFID etc.
The main objective is towards low power multiplier circuits compared to the existing FinFET Array Multiplier [10], FinFET Vedic multiplier [3] and MOSFET conventional multiplier & BZFAD ((By pass zero feed A directly) [4]. Heat dissipation is proportional to power. More heat dissipation results due to more power which decreases speed and reliability. So, the requirement for IOT devices such as smart environment, smart health and smart transportation invokes to make the devices for low power. M. Mottaghi-Basterji [4] presented a paper based on low power structure based on add and shift architecture, using 130 nm CMOS technology. V.M. Senthil Kumar [3] presented a paper implementation of Vedic mathematics based on discrete wavelet transform for biomedical and signal processing. MAC unit, RAM or ROM, Adder, multiplier is included in the discrete wavelet transform the existing CMOS has more power than FinFET DWT which is implemented using 32 nm BSIM Files. Anubhuthi Mittal [11] presented the design of low power and high speed 16 order FIR filter. In the 16 order FIR filter [11] add & shift Wallace tree (WT) and Vedic multiplier are used for the multiplication. Reduced area and delay is obtained by using add & shift multiplier implemented on FPGA Spartan 3 using Xilinx ISE 8.1.

1.1 Organization of paper

Section 2 presents the background of FinFET device. Section 3 presents the Proposed FinFET based conventional design of multiplier which is implemented by using 7nm BSIM CMG FinFET files. Section 4 presents comparison of proposed FinFET multiplier with existing multiplier. The proposed FinFET multiplier shown low power as compared to the existing one. Section 5 presents comparison of FinFET multipliers from 20 nm to 7 nm shown the result that as the technology node decreases the static power dissipation and dynamic power dissipation decreases. Section 6 concludes the paper

2. Background of FinFET device

FinFET device is a 3D structure which has a silicon body perpendicular to the plain of wafer [1]. The gate of the FinFET is wrapped on channel. FinFET can have one, two, three and four gates wrapped on channel. Channel is controlled by gates which reduce short channel effects [12]. Compared to MOSFET, FinFET has better gate control which results faster switching speed, higher on current, lower leakage. FinFET can be operated in 2 modes a) Independent gate mode (LP) b) shorted gate mode (SG). In the Independent Gate Mode four terminals are present in FinFET. Independent gate mode also called LP mode which is used to reduce threshold voltage. In this mode back and front gate are connected to different inputs. In the Shorted Gate mode (SG) 3 terminals are present in FinFET. Front gate and back gate both are tied together. At technology node below 20 nm MOSFET suffer from short channel effects such as more leakage power, threshold variations [13]. To overcome short channel effects FinFET is proposed. FinFET is formed on thin silicon insulator termed as fin [3]. Gate work function of the FinFET can be used to reduce power and adjust the threshold voltage. FinFET is emerged as promising device in literature to provide solution to the problem taking place due to reduced technology node [14]. FinFET fabrication is compatible with MOSFET for rapid deployment [15]-[16].

Figure 1. FinFET fabrication. 3. FinFET based Add and Shift Multiplier

Conventional Shift-and-add multiplication is similar to the multiplication performed by paper and pencil. To multiply two N-bit numbers, the algorithm takes one bit of the multiplier at a time from right to left, multiplying the multiplicand by this single bit of the multiplier and placing the partial product to the left of the earlier results. At every clock cycle the multiplier bit is shifted to its LSR value. If the multiplier LSR [0] value is “0” the accumulator is added with MSR register and zeros then 1-bit right shifting operation is performed. If the multiplier LSR [0] value is “1” then added to the accumulator is added with MSR register and A input then 1-bit right shift operation is performed. After all the multiplier bits have been tested the product is in Partial Product Register (MSR, LSR). The conventional
multiplier consists of the following components.

1. Vectored 2X1 Mux of k bit each input.
2. Ripple carry adder k-bit with k+1 bit.
3. Two special purpose shift Registers with parallel in parallel out and right shift register used to store the Product.
4. Control logic circuits has outputs such as counter output signal and shift/load signal. The counter output tells which partial product is generated for the input given to the multiplier.

![Figure 2. Architecture of Conventional Shift and Add Multiplier](image)

**Table 1: Analysis of Conventional Add and Shift Multiplier by Mathematical method input A=0011,B=0011**

<table>
<thead>
<tr>
<th>Res f</th>
<th>Cloc k</th>
<th>Shift/Loa d (1/0)</th>
<th>Adder MSR+A Partial Product MSR LSR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0011</td>
<td>00011 0000 0000</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0011</td>
<td>00011 0000 0000</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>00110</td>
<td>00111 0011 0011</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>00100</td>
<td>00101 0011 0010</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>00111</td>
<td>01000 1001 1000</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>00010</td>
<td>00100 0001 0010</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>00010</td>
<td>00100 0001 0010</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>00010</td>
<td>00100 0001 0010</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>00010</td>
<td>00100 0001 0010</td>
</tr>
</tbody>
</table>
Fig 3. Flow chart of conventional Multiplier
Figure 4. Simulation Results of 4bit Conventional Add and shift Multiplier for A=0011, B=0011 and Output=00001001

Figure 5. Schematic of 4-bit FinFET Conventional Multiplier

Figure 6. Power simulation for conventional Add and shift Multiplier

4. Results and Discussion

Simulation results of FinFET based conventional multiplier using 7 nm BSIM Files [15] shown that the static power dissipation in conventional multiplier is less than existing multipliers with MOSFET at different technology nodes and its static and dynamic power dissipation decreases as technology node reduces. Table 5 data results show that comparison of static power dissipation of FinFET conventional multiplier has low power dissipation compared to the existing MOSFET conventional and FinFET array and Vedic multiplier.

Table 2 : Static Power (µW) Comparison
Table 3: Dynamic Power (µW) Comparison

<table>
<thead>
<tr>
<th>Technology</th>
<th>20 nm</th>
<th>16 nm</th>
<th>10 nm</th>
<th>7 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>0.9</td>
<td>0.85</td>
<td>0.75</td>
<td>0.7</td>
</tr>
<tr>
<td>Conventional</td>
<td>325</td>
<td>187.4</td>
<td>85.07</td>
<td>3.90</td>
</tr>
</tbody>
</table>

Table 4: Transistor count and clock cycles of Proposed multiplier

Figure 7. Comparison of static power dissipation of FinFET conventional multiplier at different technology nodes.
Figure 8. comparison of dynamic power dissipation of FinFET conventional multiplier at different technology nodes.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transistor count</th>
<th>Clock Cycles / Multiplication</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>2022</td>
<td>8</td>
</tr>
</tbody>
</table>
Table 5: Comparison of static power dissipation of Existing multipliers and Proposed 7nm FinFET Conventional multiplier

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>Width</th>
<th>Technology</th>
<th>Static Power (µW)</th>
<th>Ref. Paper No.</th>
<th>Published Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEDIC</td>
<td>4-bit</td>
<td>32 nm (FinFET)</td>
<td>175.68</td>
<td>[3]</td>
<td>2019</td>
</tr>
<tr>
<td>Designed</td>
<td>4-bit</td>
<td>7 nm (FinFET)</td>
<td>3.90</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 9. Comparison of static power of Existing multiplier and proposed 7nm FinFET conventional multiplier

Figure 10. Transistors count and clock cycles per multiplication of 7nm FinFET conventional multiplier
Conclusion

The Multipliers are extensively used in Digital Signal Processing (DSP). With the advancement in VLSI technology as the DSP has become increasingly popular over the year, the high speed realization of multiplier with less power consumption has become much more demanding. The operation of FIR filter is mainly depended only on the multiplier design. Implemented Conventional multiplier using FinFET 7 nm, 10 nm, 16 nm and 20 nm technologies accomplished by using BSIMCMG files and licensed Symica Tool. Simulated multiplier shown the results that the FinFET based conventional multiplier has low power compared to the mosfet based conventional and BZFAD multiplier. The power dissipation, of FinFET based conventional multiplier is found less than the FinFET based Vedic and array multiplier. By observing these comparisons, we can state that conventional multiplier reduces the power dissipation. To improve the multiplier performance the FinFET based conventional multiplier is best compared with mosfet based other multipliers for implementation.

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