Role Of Machine Learning In Vlsi Ic Design

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Abstract*:* AI has influenced the field of integrated circuits, this being its first application in AI. This technology replaces the traditional VLSI design methodology existing today. Automation of design devel- opments have been implemented by replacing the time consuming manual design's generated by humans. This advancement would lead to massive revolution in the area of hardware computation and AI research domain. With the advent of modern chip, which are highly complex, it is a very tedious and slow process to design with humanly aids. The process of confirming the critical design's manually also finds no hope. Hence automation of various task is done in past 40 years, and many other complex task are automated. When someone comes with a new idea (in view with computation, processing, optimization, interconnect fabrication) the process of designing is automated. Companies such as IBM and Intel are enabled with their own CAD Organization for handling these automated tasks. CAD tools have been sold by many companies such as Candence, Synopsis and Mentor Graphics serves as implementation of AI in Chip design. Machine learning has extended its arm in aiding feasible solution for many kinds of problems in many engineering fields. The role of machine learning in EDA tools business, have expanded its potential in reducing the time consumption in design implementation, cost reduction, productivity of design products. In this paper we have reviewed the role machine learning in VLSI chip design and implemented ML based BIST.

Keywords- ML, AI, VLSI, BIST, CAD

1. Introduction

A rapid growing of an integrated circuit technology is overtaking when compared with capability of IC design. This is mainly due to the significant growth of AI. The computation task which is assigned to VLSI is comparative and time taken process, once the AI is implemented to do the same computational task. AI research is derived from the advances of VLSI design support and computing hardware. As the technology growth is happening in day by day and time to time, that growth is necessarily to be observed and implemented by VLSI developers in order to enhance their design tool. An improved design methodology, features and capabilities brings to VLSI design that is promises by AI. Though AI brings lots of features and methods, bringing a solution for various problems is still having certain limitations. So, the introduction of machine learning (ML) gives many improved opportunities to either collaboration or individual field of VLSI and computer-based-design. Computer chips are designed and implemented from the knowledge of gained from AI. It is treated as foremost application from AI. In recent days, computer-based design tools are handled and frequently used by the knowledge obtained from the introduction courses from AI. Earlier, most of the chips are designed by hand due to which the size of those chips are too large and its performance also slow. It is difficult and complex task to verify those hand based designed chips. These kinds of complexities are lead to develop an automation tool. This automation tool is upgraded for additional tasks which are assigned to it. Chip designers brings new ways of design in time to time basis like combing the memory, new procedure in computational task, etc., need to be automated in the design process. Companies like Intel, IBM have internal CAD establishments for these purposes. Numerous companies like Cadence, Synopsys, Mentor Graphics sell CAD tools, which can be regarded as applications of Artificial Intelligence to chip design. Sometimes data obtained from the cluster or collecting the data is mandatory to rec- ognize the pattern. This pattern can be recognized effectively by concentrating on the fol- lowing things like classify the various objects, predict the object of interest, input-output relations based on their complexities, deep neural networks with various other layers are utilized for various kinds of pattern, objects and speech recognition applications. Machine learning has a great interest on those above mentioned areas. DNNs needs to responds for the new things with comparison to the already suggested things or existing methods. This must be extended for the most recent stage of development. If any kind of non-stationary systems, it is required to adjust the decision-making process in order to strengthen the process of action and this is one kind of machine learning outcome. Management of power dynamically and controlling the electric vehicle can be learned from the action of strengthening process such as temporal difference learning (TD-lambda). In this way, the problems are tackled by pedram's group. Power management in data centers is required to strengthen the process of learning and it is taken as the recent work.

2. Role of ml in manufacturing process

Implementation of Physical Verification using Machine Learning, lithography hotspot detection is one among step involved in validation, this process is known as Physical verification fig 2.1. Machine learning specially

facilitates to lower flip-round-time and production expenses. Lithography hotspots denote precise styles that have a tendency to fail in printing since behind the process of resolution enhancement techniques, which might be turning into increasingly common due to the difficulties in lithography system, procedure variant. To improvise the ability of manufacturing and decrease expense, the early hour's detection of lithography hotspot remains chosen an important mission. Usually, heavily priced lithography simulation is needed for correct hotspot detection, frequently resulting to extended turn-round time. With higher predicting efficiency, machine learning is a appropriate technique used in developing efficient hotspot detection fig 2.2 [2]. Hot spot detection is a kind of process which involves classifying a layout chips into two categories namely hotspot and non-hotspot. The aim is to develop a model which can exactly classify chips into two labeled categories. The evaluation process is carried out practically by means of two metrics, which is false alarm and detection accuracy. Detection accuracy refers to the proportion between the no. of real hotspots and the correctly detected hotspots. The term False alarm refers to the number of non-hotspots that are considered the same as hotspots.

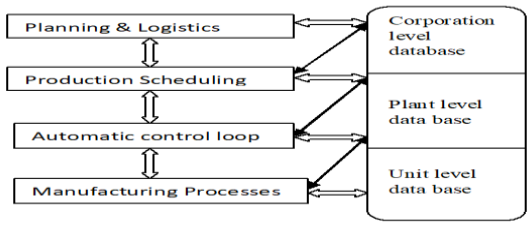


Fig 2.1 ***MANUFACTURING*** *process*

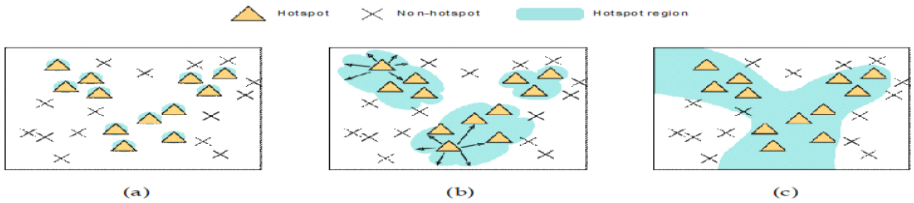


Fig 2.2 [2] A 2D-space example of hotspot region decision. (**a**) Pattern matching. (**b**) Fuzzy pattern matching. (**c**) Machine learning

Few novel applications of Artificial intelligence techniques in the design and production of chips. With an increasing number of data intensive tasks, the ability of Artificial intelligence in classification, inference and optimization is highly desired to be completely activated. The successful applications can minimize the workload of designers to extract the key information from massive data set, eventually speeding up the process of chip design.Sub-22 nm regime has become an extremely complex process requiring hundreds to thousands of steps due to the increasing process variability, increased design complexity and reduced design margin, chip design and manufacturing. Identification of pre-silicon hotspot by grouping, detection of post-silicon variance and position of defects by assumption, and timing after silicon tuning. The hotspot identification issue in physical design and testing stages is to identify hotspots with quick turn-around-time on a defined model. Conventional hotspot identification depends heavily on full chip lithography simulation, which can achieve very high accuracy but can be extremely expensive in computation. The subject includes presilicon hotspot discover by grouping, identification of postsilicon variance and localization of defects by inference, and scheduling post silicon adjustment by iterative testing and optimization.

3. Role of ML in mask Synthesis

As the size of channel length to the furthest of light frequency, a few quality improvement methods (Resolution Enhancement Techniques) such as optical proximity correction (OPC) Fig 3.1, source mask co-optimization, and sub resolution help highlights, transform into prerequisite. AI could be put on a few Resolution Enhancement Techniques to upgrade turnaround time of mask synthesis.

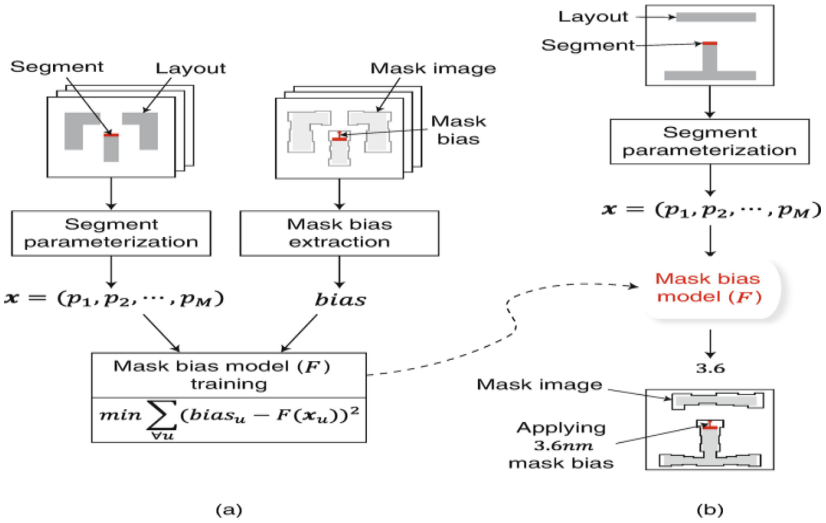


Fig 3.1 Optical Proximity Correction [5]

4. Role of ML in Miscorrelation:

When a particular task is analyzed with the help of two different tools for the similar data as an input, there is a possibility to produce different results even though applying "laws of physics" and this is happening because of miscorrelation. Miscorrelation leads to affect the design flow and there is possibility that worst things may also happen in the flow. For example, the following two different tools analyzed which are P&Rs (Static Timing Analysis) STA tool and signoff STA tool. These tools determine its endpoint as positive and negative worst slack respectively. So, the design flow analysis to be repeated in order to avoid the miscorrelation. If concentrating to reduce the worst things in the design flow on one particular (P&R) tool fig 4.1, may create a miscorrelation to the signoff tool. This causes unnecessary sizing, shielding or Voltage-Temperature swapping operations that cost area, power and design schedule. When the miscorrelation is respect to time then it is very detrimental because timing closure of design flow consumes 60% of total design time. The guard bands protect the design flow from worst things and also help to bring the balance between power and speed.

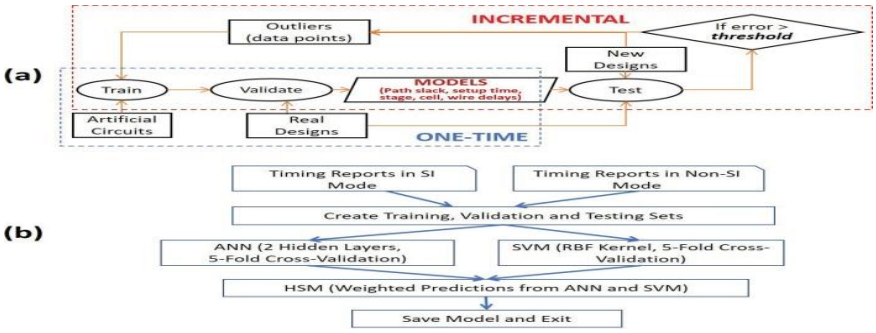


Figure 4.1: Flow Chart for machine learning of STA toolmiscorrelation.[3]

5. Role of ML in Data path Placement

S. Ward et al [12], proposed an automatic data path extraction in the following new way. Judges the different data paths and then assigns the ranks to them in order to optimize it. This optimization is followed in a general way of driving or placing the data along with new placement flow fig 5.1[12]. SVM and ANN methods are joined together at the initial training stage in order to discriminate and judge the data paths. This makes an efficient model during run time and treated as a compact model when both the methods are combined together. From the set of working data paths an error tolerant is fixed in SVM model. But ANN will produce the decisions from the trained samples and it is like network of neurons presents in humans. Whether it is data path or non-data path, accuracy of evaluation is the prime aim. This can be achieved by both SVM and ANN. Identifying the data path pattern from unknown pattern is improved which can met in the data learning models in the training stage. Certain threshold levels are set while using SVM and AVM evaluation in order to identify the particular pattern is data path pattern or non data path pattern.

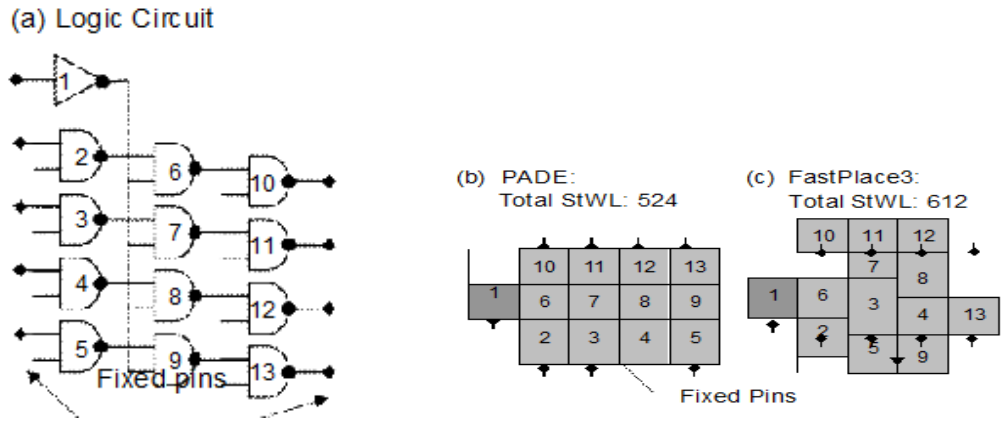
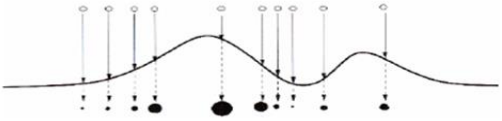


Fig 5.1 Data path placement [2]

6. Role of ML in Power Analysis:

Power calculation of VLSI circuits in traditional methods in more complicated circuits is more complicated. And the Power calculation technique is always a trade-off between time and precision. Simulation-based calculation of power provided the most reliable yet time-consuming performance. Here, VLSI power calculated in Monte-Carlo and other statistical approaches is less dependent on simulation and with less time obtained accurate performance. The Monte-Carlo methods or experiments in Monte-Carlo are a wide variety of computational algorithms focused on repeated random sampling for numerical results fig 6.1. Study was carried out on power analysis at RTL or an elevated abstraction level [7]. To get accurate power characterization, much low-level info on the circuit need to be modeled, which include standard cell parameters, gate sizing and gating of clock and placement of the registers. Gate-level power evaluation uses them to estimate the switching capacitance and activity element of each circuit node.



$$p_N(x) = \frac{1}{N}\sum_{i=1}^{N} w(x^{(i)})\delta_{x^{(i)}}(x) \xrightarrow{N\to\infty(a.s.)} p(x)$$

Fig 6.1 Sample based Monte-Carlo [7]

7. Role of ML on Routability Prediction:

The work [9] materials the first methodical study on rout ability prediction based on Convolutional Neural Network. Subliminally, that is obviously a promising route but isn't well studied previously. The technique, RouteNet can simply forecast general routability fig 7.1 in circumstances of Design Rule Violation count taking into consideration macros. RouteNet achieves comparable precision in comparison to that of global routing but is generally orders of magnitude quicker actually if training period is typically counted. To the most effective of our understanding, this is actually the 1st rout ability predictor which includes both such great accuracy and great velocity. In predicting DRC hotspot locations considering macros, it makes a large improvement of 50% accuracy improvement vs. global routing. Furthermore, RouteNet extraordinarily outperforms SVM and logistic regression-centered prediction.

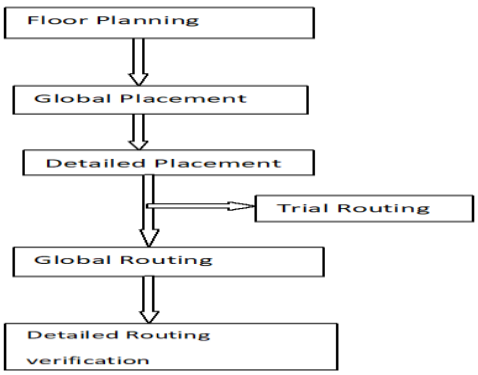
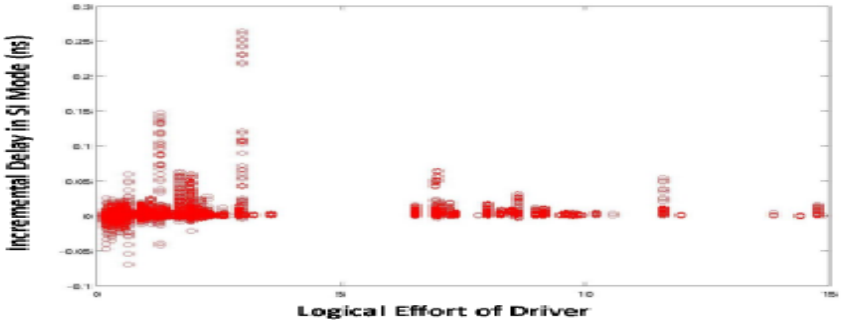


Fig 7.1 General Physical design flow

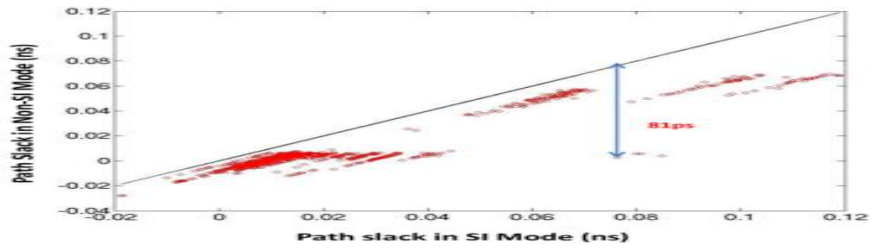
8. Role of ML on Interconnect Coupling Delay and Effects:

The paper [10] break down various sources that cause time deviation among SI and non-SI settings and offer latest instincts on electrical and sensible boundaries to influence steady progress time, deferral way to delay in SI mode. Dissimilar to, they approve various new boundaries impact SI Incr Delay ADsi. They created pristine ML based varieties for gradual changeover period and deferral because of sign respectability, and make these varieties to determine a fresh out of the box new model for way delay. The most pessimistic scenario absolute mistakes in displaying forecasts of gradual changeover period, incr delay because of SI and SI-mindful way delay (in ps) are 7.0, 5.2 and 8.2, separately.



(a)

Fig 8.1(a) Incr delay due to SI varies in the same way as $R \times C$*[10]*



(b)

Fig 8.1 (b) Path slack divergence in SI and non-SI analysis [10]

9. Role of ML on Testing

A pattern test design generator which ensures total issue inclusion while limiting test application time, region overhead, and check information stockpiling is fundamental for any effective built-in self test (BIST) plot. A wide range of age plans have been proposed to achieve different tradeoffs between these boundaries [11-14]. The arrangements range from pseudo-random strategies that don't utilize any capacity yet take a long application time and regularly don't recognize a few shortcomings to deterministic methods that may require huge test information stockpiling however accomplish total deficiency inclusion in a generally more limited time.

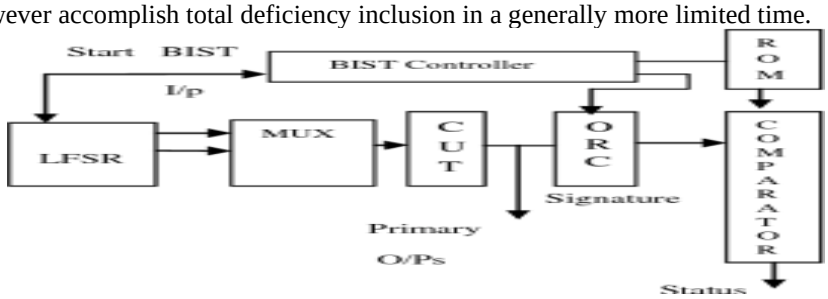


Fig 9.1 Pseudorandom BIST Architecture [11]

Conclusion

This paper we have demonstrated the use of Artificial intelligence in various aspects of VLSI Logical and Physical design like the use of AI in manufacturing, miscorrelation, power analysis, testing, mask synthesis, transition and interconnect delay, CAD tools. Yet there are plenty of scopes of AI in VLSI design phases.

Moreover, VLSI backend configuration is still at its beginning phase in applying AI procedures. For example, in the SRAF generation, pixel-by-pixel expectation is required and just direct models are utilized, restricting the utilization of more convoluted models because of high computational cost. Essentially, OPC is simply reasonable to embrace direct models also. Such sort of improvement issues basically need to create another cover picture with a given format image. It merits investigating whether generative learning strategies can be applied. For arrangement and directing issues, manual determination of significant highlights is as yet required, while it isn't evident whether general portrayal of format data exists and whether programmed include choice can be created. Furthermore, unlike fields with broad examination on AI like picture acknowledgment in which huge measure of information is accessible, it is for the most part troublesome and costly to acquire sufficient information in VLSI plan for preparing powerful and precise models. Along these lines, it is basic to create strategies to improve displaying exactness with loosened up necessity of enormous information so that AI can be generally embraced. All of these troubles stay to be explored in future.

References

1. Burges, Christopher JC.1998 "A tutorial on support vector machines for pattern recognition." Data mining and knowledge discovery 2, no. 2 121-167.
2. Lin, Yibo, and David Z. Pan. 2019"Machine learning in physical verification, mask synthesis, and physical design." In Machine Learning in VLSI Computer-Aided Design, pp. 95-115. Springer, Cham
3. Kahng, Andrew B.2018 "Machine learning applications in physical design: Recent results and directions." In Proceedings of the 2018 International Symposium on Physical Design, pp. 68-73.
4. Bansal, S., and R. Goering. 2012"Making 20nm Design Challenges Manageable." http://www.chipdesignmag.com/pdfs/chip design special DAC.pdf
5. Chan, Tuck-Boon, Andrew B. Kahng, Jiajia Li, and Siddhartha Nath. 2013"Optimization of overdrive signoff." In 18th Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 344-349. IEEE.
6. R. Goering, 2013“What’s Needed to “Fix” Timing Signoff?”, DAC Panel.
7. Kahng, Andrew B. 2018"New directions for learning-based IC design tools and methodologies." In 2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 405-410. IEEE.
8. Yang, Jianlei, Liwei Ma, Kang Zhao, Yici Cai, and Tin-Fook Ngai. 2015"Early stage real-time SoC power estimation using RTL instrumentation." In The 20th Asia and South Pacific Design Automation Conference, pp. 779-784. IEEE.
9. Xie, Zhiyao, Yu-Hung Huang, Guan-Qi Fang, Haoxing Ren, Shao-Yun Fang, Yiran Chen, and Jiang Hu.2018 "RouteNet: Routability prediction for mixed-size designs using convolutional neural network." In IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 1-8.
10. Kahng, Andrew B., Mulong Luo, and Siddhartha Nath. 2015"SI for free: machine learning of interconnect coupling delay and transition effects." In ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP), pp. 1-8.
11. Fagot, Christophe, Patrick Girard, and Christian Landrault. 1997"On using machine learning for logic BIST." In Proceedings International Test Conference , pp. 338-346.
12. Ward, Samuel, Duo Ding, and David Z. Pan.2012 "PADE: A high-performance placer with automatic datapath extraction and evaluation through high-dimensional data learning." In DAC Design Automation Conference , pp. 756-761. IEEE.
13. Yu, Bei, David Z. Pan, Tetsuaki Matsunawa, and Xuan Zeng.2015 "Machine learning and pattern matching in physical design." In The 20th Asia and South Pacific Design Automation Conference, pp. 286-293. IEEE.
14. Agrawal, V. D., C. R. Kime, and K. Saluja. "KA tutorial on built-in self-test, part 1: Principles." Design & Test of Computers, IEEE 10, no. 1 (1993): 73-82.
15. Bardell, Paul H., Jacob Savir, and William H. McAnney.1987Built-in test for VLSI: pseudorandom techniques. Wiley.
16. Savir, Jacob, and William H. McAnney. 1990"A multiple seed linear feedback shift register." In Proceedings. International Test Conference , pp. 657-659. IEEE.