Research Article

A Cascaded Multilevel Inverter With Reduced Switch Count Using Modified Sinusoidal Pulse Width Modulation Technique

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Abstract: In this article, the use of multilevel inverters is suggested by H-bridge. The recommended arrangement reduces the circuit size by the use of a reduced number of power switches and dc voltage sources. Simulation outcomes validate the efficiency and practical precision of the proposed topology using the new algorithm to produce all voltage levels for a 7-level inverter. For the two topologies obtained, it compares the percentage of THD.

I. INTRODUCTION

Multilevel inverters have now achieved greater popularity for their ability to work at high and medium voltages and due to other benefits such as high power consumption, lower order harmonics, lower switching failures, and increased electromagnetic interference. These inverters generate a stepped voltage waveform by using a variety of dc voltage sources as the input and an appropriate arrangement of the power-semiconductor-based modules. Three major architectures of multilevel inverters were presented: "diode clamped multilevel inverter," "multilevel inverter flying capacitor," and "multilevel cascaded inverter." The cascaded multilevel inverter consists of a set of single-phase H-bridge inverters and, based on the severity of dc voltage sources, is split into symmetric and asymmetric classes.

The magnitudes of the dc voltage sources of all H-bridges are the same for symmetrical types, while the values of the dc voltage sources of all H-bridges are different for asymmetrical types.

Multilevel inverters (MLI) have received further consideration for their high-power and medium-voltage capability and, for example, high power output these days, in view of various focal points. These inverters produce a staircase voltage waveform by using individual dc voltage sources by correctly arranging DC sources.

In recent years, multiple topologies have been introduced for cascaded multilevel inverters with distinct control techniques. The minimum number of dc voltage sources, which is one of the most critical features in evaluating the cost of an inverter, is the key value of all these devices. On the other hand, since a large number of bidirectional control switches are used by some of them, which is the main disadvantage of these topologies, a high number of bipolar gate insulated transistors (IGBTs) are required. The main drawback to this structure is its bidirectional control switches, causing the number of IGBTs and the inverter's total cost to increase.

Lately, a few geographies with distinct control methods have been introduced for lowered phased inverters. The main advantageous location in all of these devices is the low variety of dc voltage sources, and one of the most important highlights in deciding the expense of the inverter. Then again, as some of them use a high number of bidirectional force switches, which is the primary obstacle to these geographies, a high number of secure entryway bipolar semiconductors (IGBTs) are needed.

The main disadvantage of this device is the transfer of its bidirectional force, which makes it possible to increase the quantity of IGBTs and the maximum inverter cost. The considerable limitation of this geography and its dimensions is characterized by its ability to use a small number of dc voltage sources and force switches to generate a remarkable amount of yield voltage ranges. Another geography of fell-phased inverters is proposed in this article in order to produce the amount of yield voltage levels and reduce the amount of force switches, driver circuits, and the overall cost of the inverter.

Moreover, from various points of view and different geographies, the proposed geography is contrasted, such as the quantity of IGBTs, the number of dc voltage sources, the variety of statistics for dc voltage sources and the measurement of obstructing voltages per switch. Finally, replication using matlab programming confirms the display of the geography suggested by using a 7-level inverter to produce all voltage levels.

II. TEN SWITCH SEVEN LEVEL MULTILEVEL INVERTER TOPOLOGY

There are a number of H-bridge inverter units connected and maintained from different DC outlets in series to a multilevel cascaded inverter. The DC roots must be isolated from each other since the yield is taken in order. Therefore, it is further recommended to use cascaded multilevel inverters with energy components or photovoltaic clusters, taking into account the objective of achieving higher levels of voltage.

By associating the DC source to the AC output and by various mixes of four switches where Vdc is the input voltages of the H- bridge, each bridge has the property to create three levels such as + Vdc, 0, -Vdc.

The proposed ten switch sevel level multilevel inverter topology is as shown in the figure 1.

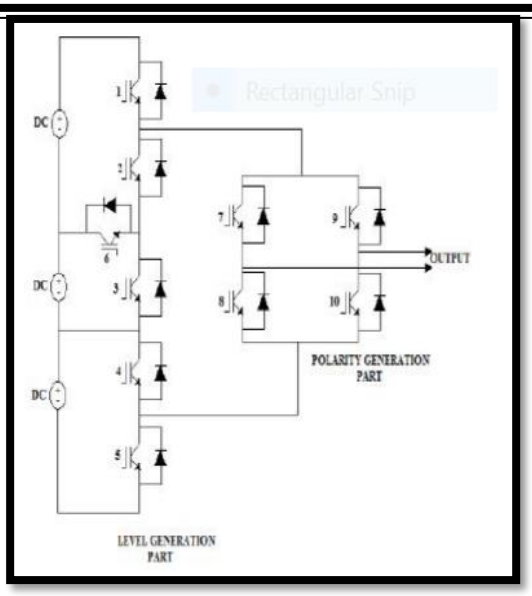

Figure 1. Proposed seven level inverter topology.

Output voltage in this hybrid multilevel inverter topology is divided into two sections. One vector is called the "level generator" and in positive polarity is responsible for level generation. In this segment, high frequency switches are required to achieve appropriate amounts. The other factor is referred to as the "polarity generator" that is responsible for producing the output voltage polarity. The polarity generator works at the frequency of the thread. To generate the multilevel voltage output, this topology combines the two parts (low frequency & high frequency).

In order to create a complete multilevel output, the positive levels are provided by the level generator (high frequency part) and then this part is fed to a polarity generator (full bridge inverter) which will generate the polarity required for the output. This would reduce the number of semiconductor switches responsible for generating output voltages of negative and positive polarities**.**

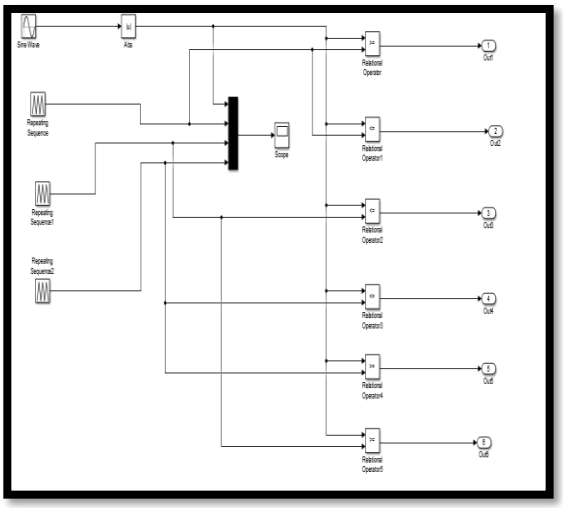

Figure2. Carrier/reference signal arrangement for SPWM-A technique.

TABLE 1:Table Showing The Switching States Of Proposed Seven Level Multilevel Inverter

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	O/P
0	1	0	1	0	1	1	1	0	0	**0**
0	1	0	1	1	0	1	1	0	0	**+V**
0	1	1	0	0	0	1	1	0	0	**+2V**
1	0	0	0	0	0	1	1	0	0	**+3V**

0	1	0	1	1	0	0	0	1	1	**-V**
0	1	1	0	0	0	0	0	1	1	**-2V**
1	0	0	0	0	0	0	0	1	1	**-3V**

IV. SINUSOIDAL PULSE WIDTH MODULATION FOR THE LEVEL GENERATOR CIRCUIT

SPWM-A Technique:

In order to achieve seven levels using the SPWM technique, one reference sinusoidal and three triangular carrier signals are necessary. SPWM, in this article, is introduced for its convenience. In this approach, carriers have a definite offset from each other and have no coincidence. They're also in contact with one another. In the figure below for SPWM, the reference signal and three carriers are shown.

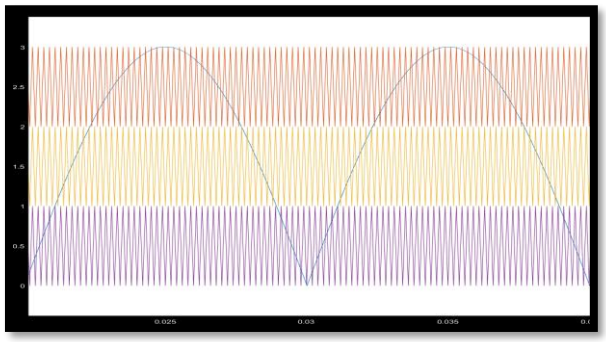

Figure 3. simulink model for SPWM-A technique

V. MODIFIED SINUSOIDAL PULSE WIDTH MODULATION TECHNIQUE

SPWM-B Technique:

Reference signals have the same amplitude and the same frequency, equal to the frequency of the line, in the SPWM-B control technique. They are in phase with one another with an offset value equal to the magnitude of the carrier signal. In order to produce pulses for inverter circuit switches, three reference signals are compared to the carrier signal.

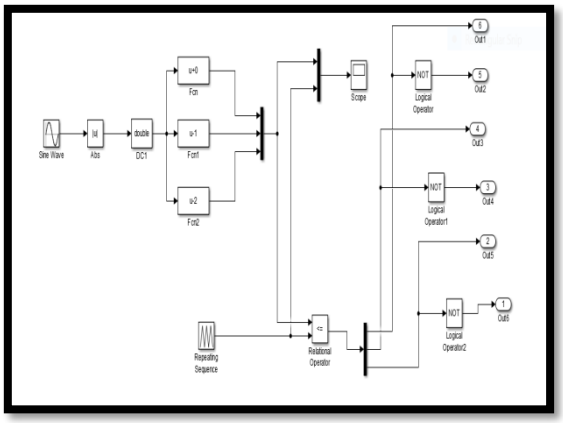

Figure 4. simulink model for SPWM-B technique

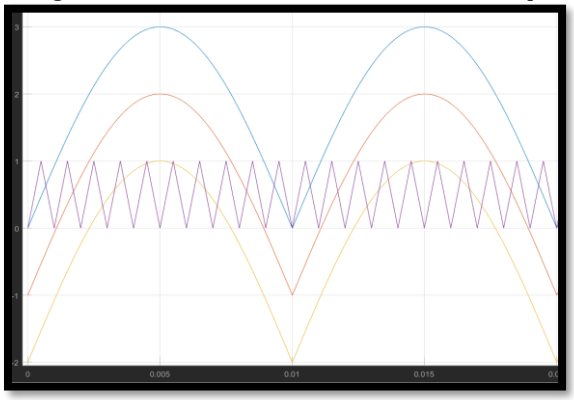

Figure 5. Carrier/reference signal arrangement for SPWM-A technique.

VI. SIMULATION DIAGRAM FOR THE PROPOSED MLI TOPOLOGY

The suggested multilevel inverter using the mosfets is simulated from the simulink library. Figure 6 illustrates the topology's circumstantial framework. The full harmonic distortion is indicated by using the THD block from the simulink library.

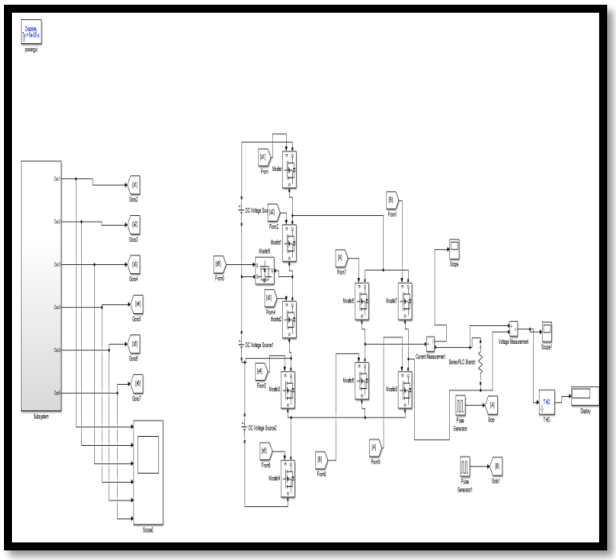

Figure 6. Simulink Model Of The Proposed Seven Level MLI Topology

VII. SIMULATION RESULTS

The above suggested simulation model is repeated in the simulink software, and the resulting results are shown. Output voltage and current waveforms are obtained for both the SPWM-A and SPWM-B strategies.

SPWM-A Results:

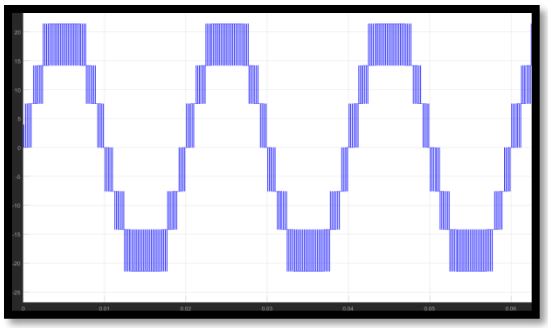

Figure 7. output current waveform of the proposed seven level MLI topology using SPWM –A technique

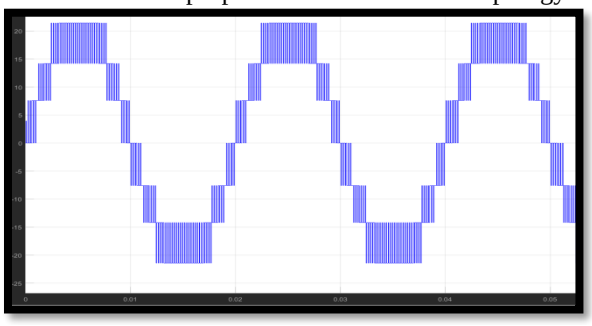

Figure 8. output voltage waveform of the proposed seven level MLI topology using SPWM –A technique

B) SPWM-B Results:

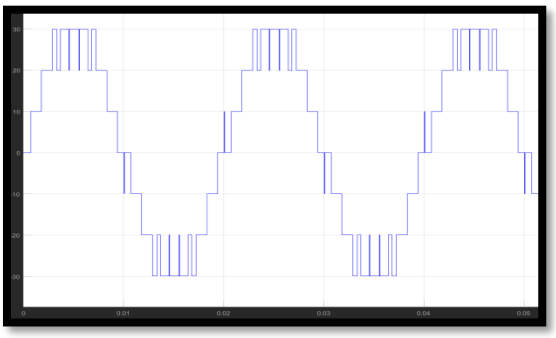

Figure 9. Output current waveform of the proposed seven level MLI topology using SPWM –B technique

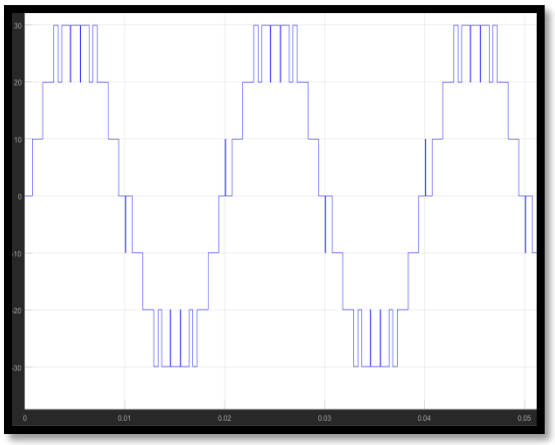

Figure 10. Output voltage waveform of the proposed seven level MLI topology using SPWM –B technique

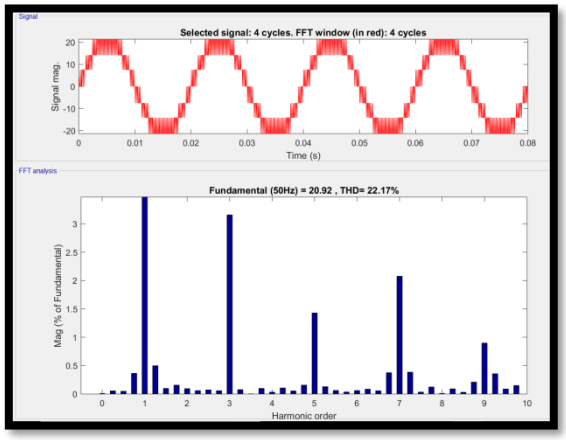

Figure 11. FFT analysis for SPWM-A technique

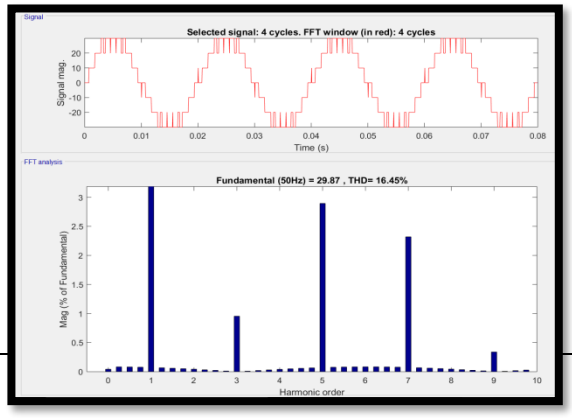

Figure 12. FFT analysis for SPWM-B technique

VIII. FFT ANALYSIS

IX. Comparison of THD for the proposed seven level inverter topologies

The following table gives the information of the total harmonic distortion.

Table 2. Detailed indication of the THD for different control strategies used

Number of levels of the output waveform	Control strategy used	THD
7	SPWM-A	22.17
7	SPWM-B	16.45

X. CONCLUSION

. The seven level ten switch inverter is simulated using both superior performance in MATLAB and Simulink software, providing enhanced output waveforms in terms of number of switches required, system power, and typical topology quality. In the mentioned topology, the switching frequency is split into high and low frequency parts. This will add to the converter's performance and lower the size and expense of the inverter.

XI. REFERENCES

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