Research Article

A Modified Design of Multilevel Inverter Using Sinusoidal Pulse Width Modulation

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Abstract— Multi-level Inverter technology is gaining popularity and been a momentous choice in the region of the high-power medium voltage-energy control. Producing high quality without the use of more count of switches and thus the development of such low switch Multi Level Inverter (MLI) topologies are concentrated more in this current research. These have the ability to meet the increasing demand of power rating using improved power quality through subsequent reduction in harmonic distortion. MLIs have their impression in the fields of large electric drives, traction, renewable energy conversion, electric vehicles, active power filters, HVDC and facts. The multi-level inverter generate a quasi sinusoidal voltage from various level of DC voltage. The proposed inverter is a 15-level cascaded MLI inverter and 23-level being its extension. These both are created by using the Level Shifted-Sinusoidal Pulse Width Modulation (LS-SPWM) technique. Reduction in the Total Harmonic Distortion (THD) has been the chief aim of the selected pattern. It gave a superior result in the THD. The proposed configuration overcomes the drawbacks of MLIs such as complexity, need of great number of power devices. It has less number of switches resulting in more levels of count from 15 to 23. Thus reduces the cost and gets better reliability for medium power applications. The proposed topology is simulated using MATLAB/SIMULINKR2013a and is verified.

I. INTRODUCTION

In recent, multilevel inverters have waved to a new path of interest in industry and academia. They have been changing into a viable technology for numerous applications and are playing a vital role in modern technologies [1]-[2]. The era of multilevel inverters (MLIs) has started with the diode clamped MLI in 1981, then capacitor clamped MLI or flying capacitor (FC) in 1992 and the cascade H-bridge MLI in 1995 [3]. Today MLIs are greatly used in many applications such as electric drives, renewable energy conversions, tractions, electric vehicle, active power filters, HVDC, and FACTs [4]-[5]. Decrease in the total harmonic distortion (THD) and increase in the output waveform quality are the facts which have made the MLIs more benificial. In addition, less switching losses, less voltage stress of dv/dt on switches, and an improved electromagnetic interference are the other very important advantages of MLIs [6]. The operations, efficiency, power ratings, and applications of MLI depend mainly on its topology and the kind of control algorithm used in its Pulse Width Modulation controller.
The most commonly known MLI topologies are [7]-[8]:

1. Neutral-point-clamped (Diode clamped) MLI
2. Flying capacitor (Capacitor clamped) MLI
3. Cascaded H-bridge MLI

By uniting these topologies with one another, hybrid topologies are developed. In the same way, by applying various DC voltage levels, an asymmetric hybrid topology has been equally achieved. The asymmetrical cascaded MLIs create more number of output levels with the same count of power electronic devices because of the different amplitude of its DC voltage sources [9]-[10]. Moreover, MLI control techniques which are based on the fundamental and the high switching frequency include [7]:

1. Space vector control (SVC)
2. Selective harmonic elimination (SHE)
3. Space vector PWM (SVPWM)
4. Sinusoidal PWM (SPWM)

These techniques have been extensively used because of their features such as SPWM which is easy to adopt, SVPWM has an extensive range of modulation flexibility and SHE can erase the specified lower order harmonics. However, these traditional techniques have their own limitations like

1. Designing and implementing is difficult (in SVPWM) when levels are more than 5
2. To calculate the switching angles, SHE plays a vital role in Newton-Raphson method
3. In SPWM technique a wide sideband harmonics exist.

Therefore the paper focuses on reducing the aforementioned limitations by using the proposed carrier based SPWM technique.

Assisting with the advanced present research in this field of MLIs, we proposed a new topology. It includes a decrease in whole part count when compared to that of classical topologies. The proposed algorithm implements a novel hybrid multilevel inverter to improve the magnitude and harmonic profile of load voltage. It has in it a few switches, gate drive circuits, and power supplies. Excluding the transformer has made the new topology more productive. Hence the anticipated configuration has less number of components to reduce the cost and enhance the reliability of the converter for medium high power applications for inbuilt isolations. It attains a 15-level output voltage. Hence it's a "15-level inverter using modified carrier SPWM switching strategy excluding transformer" with an extension to 23-Level MLI using the same strategy.

II. PROPOSED 15-LEVEL TOPOLOGY

The proposed multilevel inverter topology is for 15 levels (15L). The reference multilevel inverter is a cascaded transformer based multilevel inverter. This was presented for single phase systems. Its topology can produce a 19-level output waveform consisting of two bridges with individual low frequency transformers. The two bridges can individually generate quasi-square waveform and pulse width modulated (PWM) waveform and energized the two transformers whose secondary terminals are cascaded. The transformer provided the inbuilt isolation between the supply and load. The proposed switching algorithm of the reference is implemented for a novel hybrid multilevel inverter in order to improve the magnitude and harmonic profile of the load voltage.

The configuration was designed with power switches of count 12, gate driven circuits and power supplies. The switches used are IGBT which are bidirectional current and unipolar blocking voltage switches. Regarding the input dc supply, the sources are of count two V1 and V2. Here magnitude of V1 was selected as twice the magnitude of V2. The reference work is carried forward with PWM strategy.

The configuration of the proposed multilevel inverter topology for 15 level operation is shown in fig1. It was designed with three voltage sources and power switches of count 09. The voltage sources are taken as V1, V2 and V3. The power switches considered are unidirectional switches (IGBT) with anti parallel diodes. The extended version of this proposed multilevel inverter being 23-level consists of three voltage sources and a switch count of 14. The extension of this proposed MLI is given in further contexts.

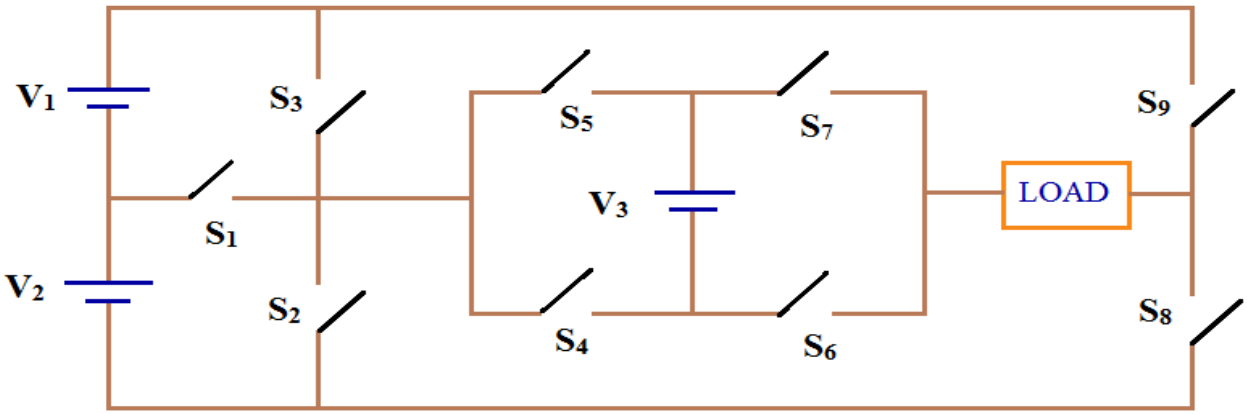


Fig 1. Circuit diagram of 15 Level MLI

Number of DC sources: 03
Number of switches: 09
Number of levels obtained: 15
Voltage sources: V_1=3V, V_2=3V and V_3=1V

III. SWITCHING OPERATION AND TABLE

Let us now evaluate each level considering the input voltages and the switches that are ON for that particular level:

1. First state (1L): This level is designed as 1L and switches S2, S4,S7,S8 are ON. Thus the load voltage $V_L=V_{dc.}$

2. Second state (2L): Switches S1, S5, S6 and S8 are ON. Therefore, voltage across the load becomes $V_L=2V_{dc}$.

3. Third state (3L): Switches S1, S5, S7 and S8 are ON. Therefore, voltage across the load becomes $V_L=3V_{dc}$.

4. Fourth state (4L): Switches S1, S4, S7,and S8 are ON, therefore, voltage across the load becomes $V_L=4V_{dc}$.

5. Fifth state (5L): Switches S3, S5, S6, and S8 are ON, therefore, voltage across the load becomes $V_L=5V_{dc.}$

6. Sixth state (6L): Switches S3, S5, S7, and S8 are ON, therefore, voltage across the load becomes $V_L=6V_{dc.}$

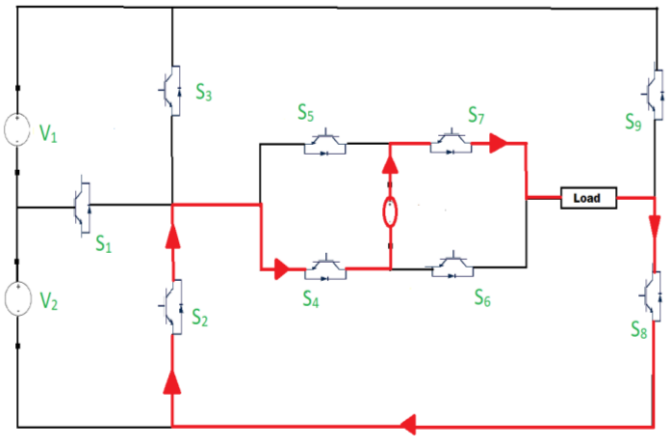
7. Seventh state (7L): Switches S3, S4, S7, and S8 are ON, therefore, voltage across the load becomes $V_L=7V_{dc.}$

8. Zeroth state (0L): This state can achieve in different combinations, herein, switches S2, S4, S6, and S8 are ON to generate zeroth load voltage state.

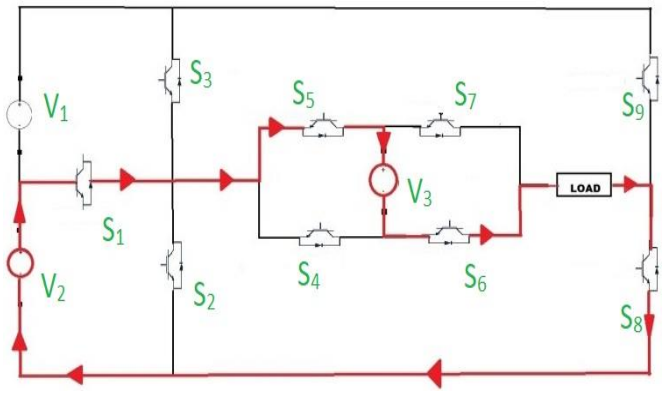
Similarly, the negative states of the load voltage waveform are created with appropriate changes. The basic idea behind this type of operation is to reduce overall conduction and switching losses of the proposed topology.

The paths for each level are given below:

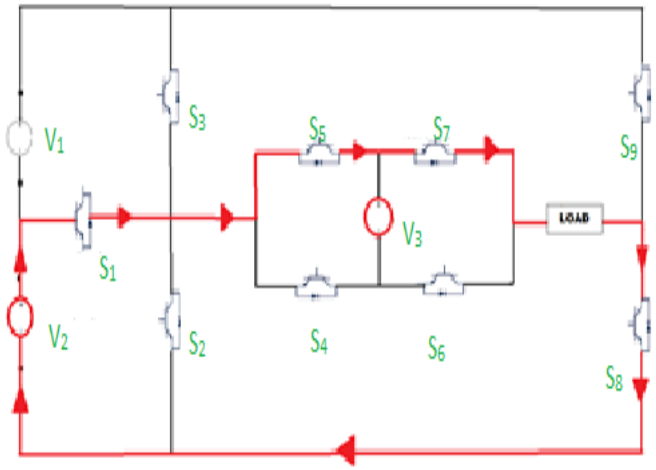
MODE 1: (V0= +1 volt)



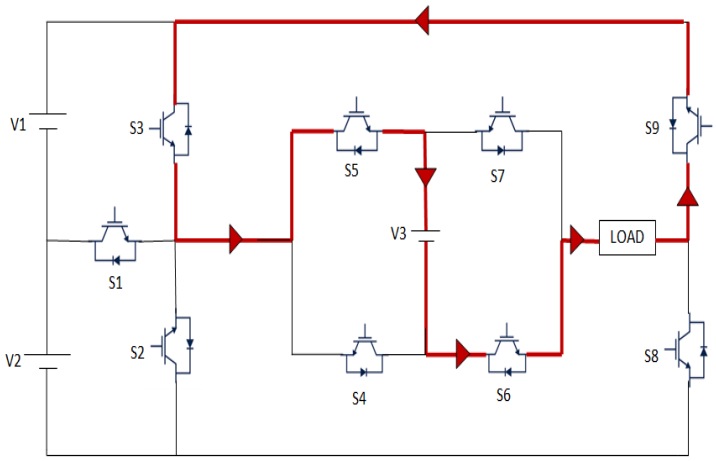
MODE 2: (V0= +2 volt)



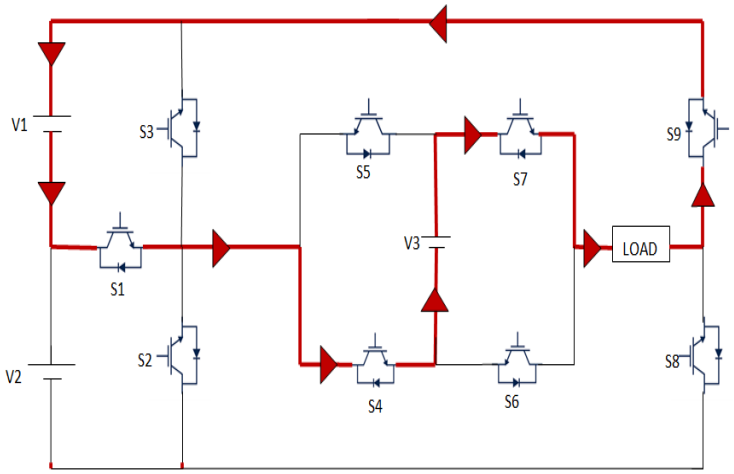
MODE 3: (V0= +3 volt)



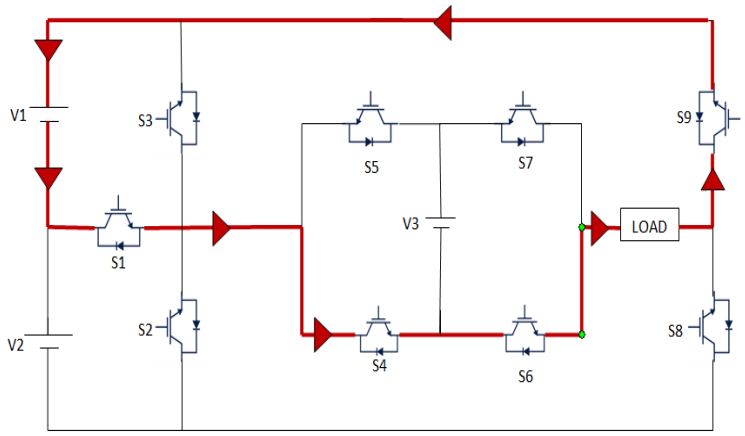
MODE -1: (V0= -1 volt)



MODE -2: (V0= -2 volt)



MODE -3: (V0= -3 volt)



The pattern of switching for the proposed topology is depicted as follows:
V1 = 3volts, V2 = 3volt, V3 = 1volts
For each set of levels i.e positive, negative and zero levels, the switching tables are given separately below.

TABLE 1: Switching table for zeroth level:

V0	S1	S2	S3	S4	S5	S6	S7	S8	S9
0v	0	1	0	1	0	1	0	1	0

TABLE 2: Switching table for positive levels:

V0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1v	0	1	0	1	0	0	1	1	0
2v	1	0	0	0	1	1	0	1	0
3v	1	0	0	0	1	0	1	1	0
4v	1	0	0	1	0	0	1	1	0
5v	0	0	1	0	1	1	0	1	0
6v	0	0	1	0	1	0	1	1	0
7v	0	0	1	1	0	0	1	1	0

TABLE 3: Switching table for negative levels:

V0	S1	S2	S3	S4	S5	S6	S7	S8	S9
-1v	0	0	1	0	1	1	0	0	1
-2v	1	0	0	1	0	0	1	0	1
-3v	1	0	0	1	0	1	0	0	1
-4v	1	0	0	0	1	1	0	0	1
-5v	0	1	0	1	0	0	1	0	1
-6v	0	1	0	1	0	1	0	0	1
-7v	0	1	0	0	1	1	0	0	1

By using suitable switching, cascading of different combinations of output voltages is possible so as to obtain fifteen levels in total.

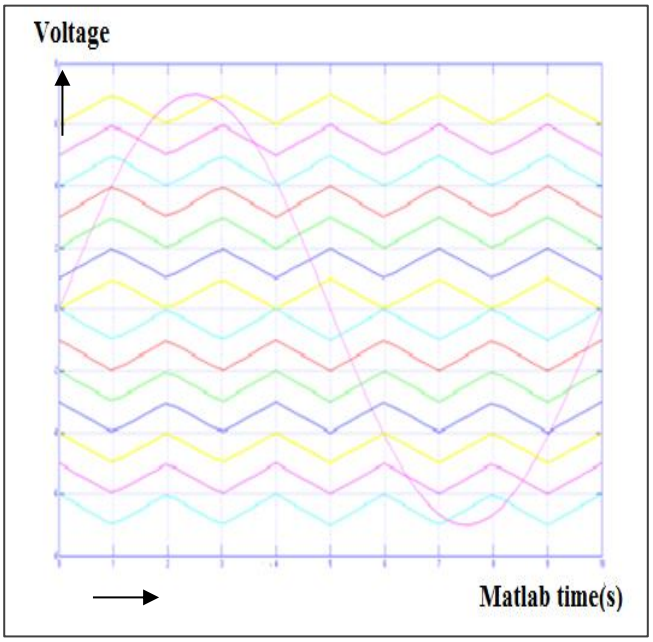


Fig. 2. shows how the triangular carrier wave is compared with reference sinusoidal wave.

The technique used for obtaining the proposed topology and its extension is Sinusoidal Pulse Width Modulation (SPWM).

It is a technique of pulse width modulation used in Inverters. An inverter generates an output of Ac voltage from an input of Dc with the help of switching circuits to reproduce a sine wave by generating one or more square pulses of voltage per half cycle. In sinusoidal pulse width modulation, the modulation signal is always less than the peak of the carrier signal. It is one of the methods to reduce the low frequency harmonics in the inverter waveform. In this method, a reference copy of the desired sinusoidal waveform and the modulating wave is compared to a much higher frequency triangular waveform called the carrier wave. It is used in Controlling DC motors, control valves, pumps, and other mechanical parts.

So, for the above applied SPWM vector concatenation we have the following advantages:

1. It is used to simplify the circuit and to reduce the size.
2. It can track with current and voltage values with less time.
3. It can be applied to any class cascade H-bridge multilevel inverter with current tracking.

The fig. 2 shows the vector concatenation at frequency 0.5Hz. Comparing this with the carrier wave at frequency 100Hz, a considerable difference in the harmonics can be observed in Fig. 3.

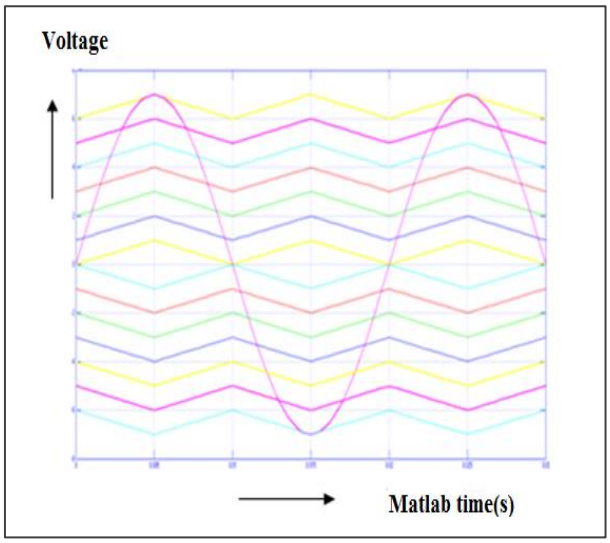


Fig. 3. Carrier waveform at frequency = 100Hz

IV. SIMULATION RESULTS

The unidirectional switches (IGBT) with anti-parallel diodes are used to design H-bridge to produce sinusoidal wave and the remaining are connected with 3 DC voltage sources.

The simulation result what we have obtained is a result of low THD by using a run time value 0.03. Therefore we obtained a voltage waveform of 15L of amplitude i.e. 7v in the positive peak and 7v in the negative peak which is symmetrical in nature.

Here the below figures show the simulation output, Fast Fourier Transform analysis and percentage details of harmonics present in the output.

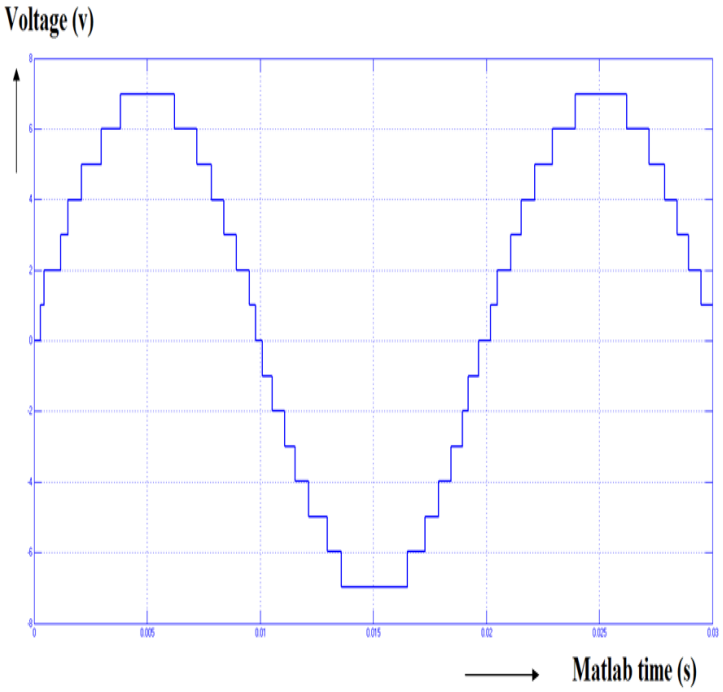


Fig. 4. Simulation output of fifteen level MLI

The Fig. 4 shows the simulation output of 15-level multilevel inverter. The peaks are at +7v and -7v as obtained.

The Total Harmonic Distortion also abbreviated as THD, is obtained with the percentage of 4.07 at the fundamental frequency of 50Hz for the proposed 15-Level multi level inverter. Fig. 5 shows the Fast Fourier Transform analysis and THD percentage obtained.

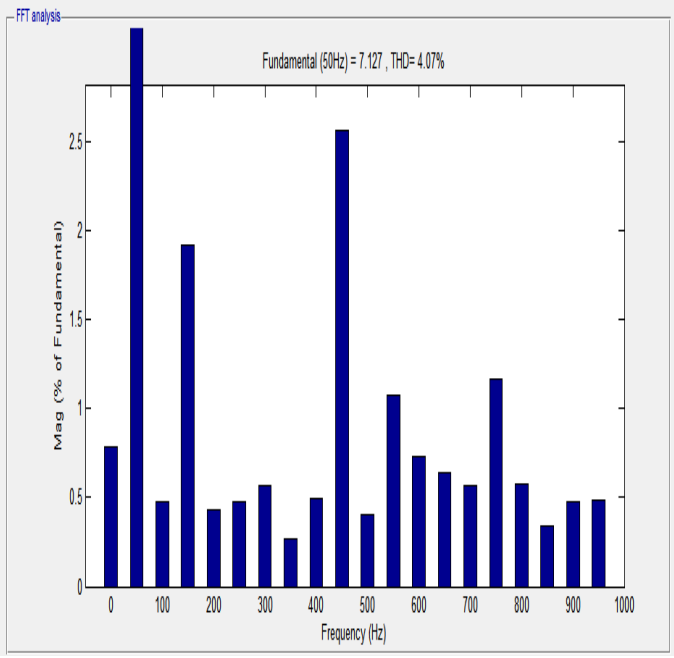


Fig. 5. FFT analysis of fifteen level MLI

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DC component      = 0.05585
Fundamental       = 7.127 peak (5.04 rms)
THD               = 4.07%

     0 Hz  (DC):          0.78%    270.0°
    50 Hz  (Fnd):       100.00%      0.5°
   100 Hz  (h2):          0.47%    249.1°
   150 Hz  (h3):          1.92%     93.9°
   200 Hz  (h4):          0.43%    136.5°
   250 Hz  (h5):          0.48%    104.1°
   300 Hz  (h6):          0.57%    199.1°
   350 Hz  (h7):          0.26%    -36.4°
   400 Hz  (h8):          0.49%    181.1°
   450 Hz  (h9):          2.57%    150.0°
   500 Hz (h10):          0.40%    219.0°
   550 Hz (h11):          1.08%     61.4°
   600 Hz (h12):          0.73%    235.6°
   650 Hz (h13):          0.64%    232.3°
   700 Hz (h14):          0.57%    211.8°
   750 Hz (h15):          1.16%    217.3°
   800 Hz (h16):          0.57%    238.6°
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Fig. 6. Percentage values of harmonics in the output.

The harmonic content percentage varies with the change in the frequency. The frequencies considered here are 0.5Hz, 100Hz, and 200Hz. The below bar graph shows how the second, third, fifth, and seventh harmonics change at the taken frequencies:

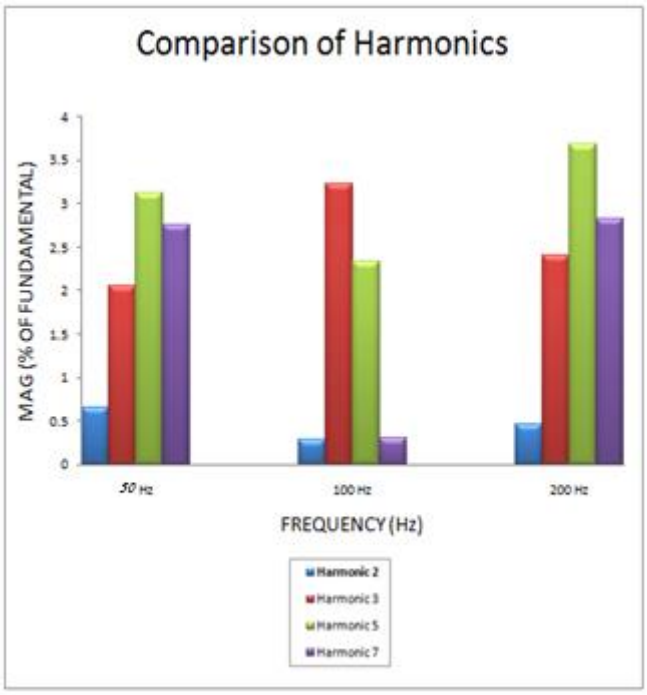

Fig. 7. Harmonic comparison of 15-level MLI at different frequencies

The total harmonic distortion varies with the frequency. For the same frequencies mentioned above, a bar graph for THD is depicted and shown below:

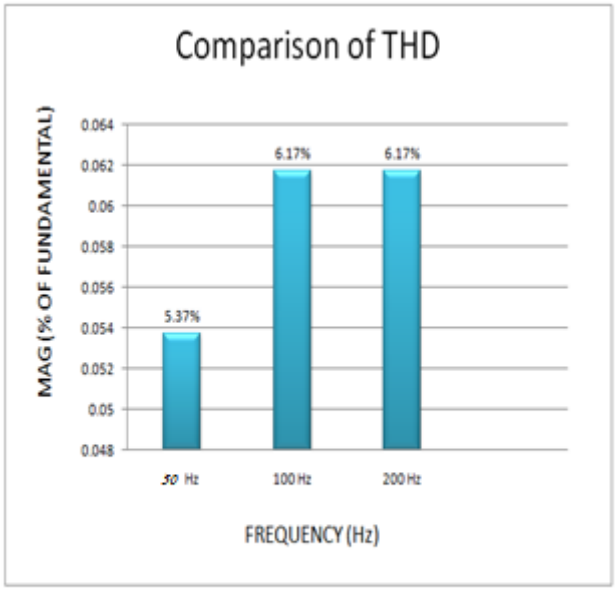

Fig. 8. THD comparison of 15-level MLI for different frequencies

V. CONCLUSION

The paper depicts an efficient output and a better harmonic performance with reduced switching losses. This has been obtained with less number of switches of count 09 for more output levels of 15. The proposed MLI have been deliberated on with the mathematical relations. On comparing with the existing topologies, one can approve the

merit of the above proposed topology in terms of ability to achieve more number of levels with a less distortion using a less number of switches and other total components. The proposed multilevel inverter has got an output voltage with harmonic profile of 4.07% Total Harmonic Distortion. Simulation results are presented and necessary comparisons through bar graphs are made. It gives an ideal solution for medium and low power applications with least harmonic distortion.

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