Implementation of A New Single-Stage Bridgeless Boost Half-Bridge AC/DC Converter with Bidirectional Switch

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Abstract: This paper discussed on the practical implementation of a newly proposed isolated bridgeless single stage AC-DC converter. The step for the practical implementation are discussed in details. These included the design of the printed circuit board, the values of the electronic and magnetic components. In addition, the experiment setup and procedures is also presented. This new circuit topology is implemented and tested at 115 Vac, 50 Hz of input supply and 20 Vdc output voltage with maximum output power of 100 W. It is also tested at input voltage with higher frequency of 500Hz to confirm the elimination of zero crossing of the input current.

Keywords: AC/DC converter, bridgeless, boost-half bridge, power factor correction (PFC) component

1. Introduction

The full bridge rectifier cascaded with DC-DC converter is mainly used in a conventional switch mode power supplies SMPS [1-5]. The input full bridge rectifier converts the AC source to unregulated DC voltage. The SMPS can be classified into two stage and single stage structure. In order to achieve high input power factor, the front end PFC is used to shapes the waveform of input current for a typical two stage SMPS. Then, followed by a DC-DC converter which controlled and regulated DC output. Single stage structure of SMPS's integrates the power factor correction (PFC) and DC-DC converter which obviously reduce the component count [6 -13]. However, both conventional SMPS structures cause significant power losses at input full bridge rectifier. This is due to reverse recovery issue of a slow diodes. Thus, a bridgeless converter has been introduced. Single stage bridgeless converter eliminates the full bridge rectifier which integrate the rectifier stage and the high frequency DC-DC converter. The semi-bridgeless [14~18] and totem-pole [19~23] circuit topology eliminates two diodes. Although semi-bridgeless and totem-pole circuit have its own advantages, obviously there are reverse recovery losses occurred. The new proposed circuit topology is then further eliminated this reverse recovery losses. However, the power switches in most full bridgeless circuit suffers from inrush current and consequently distorted the input current. In a Boost PFC topology [24], the inrush current is diverted through the additional switches and diodes. Thus, it is not a choice if the objective is to achieve less number of components. Therefore, the additional input or boost inductor [14, 15] slow down the inrush current and also contributed in shaping the input current.

In this paper, the practical implementation of a new full bridgeless circuit topology is discussed. The back to back Mosfet's which derived from [16;25~27] allows the circuit operation at positive and negative half cycle of voltage supply. The procedure to produce the boost inductor will be discussed which is expected to slow down the inrush input current. In addition, the application of the driver for the back to back Mosfet's will be explained. The design step calculation [28] of the transformer is further discussed. The experiment setup which involved the usage of the measuring equipment is briefly explained. The practical application of the new circuit topology is tested at 100 W (20 V / 5 A) with input voltage of 115 Vrms 50 Hz. In addition, the input current distortion at zero crossing is also suppressed at higher frequency of input supply. Figure 1 shows the main circuit diagram of the proposed circuit.

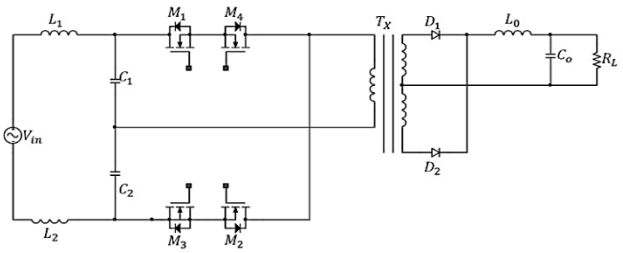


Figure 1: A new AC-DC Full Bridgeless Half-Bridge with bidirectional switch.

2. Main Circuit Components

Table 1 shows the design specification which implemented in this experiment. The expected duty cycle can be calculated by substituting the related design specification data the duty cycle equation of

$$d_1 = \frac{V_{in}}{2\left(2V_{in} - \frac{V_O}{n}\right)} \quad (1)$$

where n is the transformer transformation ratio. V_p is the voltage at primary side and V_s is the secondary voltage. The peak primary voltage V_p is equal to peak supply voltage V_inapproximately. Thus, the calculated duty cycle is 41%.

$$n = \frac{V_s}{V_p} \quad (2)$$

At initial the input power factor is expected to be 0.99, Thus, the boost inductor L_1 and L_2 is determine from

$$L_1 = L_2 \geq \frac{\left(V_{in} - \frac{V_O}{n}\right) d_1 V_{in} R \cos\theta}{2V_O^2 f_s} \quad (3)$$

where f_s is the switching frequency.

Next, the half-bridge capacitor is determine from the equation of

$$C_1 = C_2 = \frac{V_O^2}{\Delta V_C V_{in} R \cos\theta}(1 - d_1)T_S \quad (4)$$

where ΔV_C is the expected output voltage ripple. At secondary side circuit, the output inductor and capacitor is calculated based on the equation of

$$L_{O_{min}} \geq R_L d_2 T_S \quad (5)$$

$$r = \frac{\Delta V_O}{V_O} = \frac{d_2}{8 C_O L_O f_s^2} \quad (6)$$

Table 1: Proposed circuit parameters

Parameters	Value
Input voltage , V_{in}	115 $Vrms$
Input line frequency , f	50 Hz
Switching frequency, f_s	50 kHz
Output voltage, V_O	20 Vdc
Nominal output power, P_o	100 W
Output voltage ripple, ΔV_{Co}	≤ 10 %

3. Semiconductor Devices Selection

Themosfet's rating is identified by calculating the expected current flow to the devices which equal to the current flow to the primary winding of the transformer. The semiconductor switches has to block the maximum charging voltage of half bridge capacitor which approximately equal to the input voltage 115 Vrms. However, the mosfet's with slightly higher drain to source voltage, V_ds is used. In addition, in order to minimize the on-state losses, mosfet's with smaller on-state resistance R_(ds(on)) can be considered. In this work, the chosen mosfet is IPP60R080P7XKSA1. The Schottky rectifier diode can be considered to be used as secondary side rectification diode [29]. Schottky diode has an ability to switch fast with almost zero reverse recovery charge [30]. This due to silicon carbide (SICSiC) diode is a majority carrier device which does not have any minority carriers [30]. which Thus, mostly eliminated the power losses due to reverse recovery. The smaller lower forward voltage drop also much important in reducing the on-state losses. The amount of current flow through the diode gives significant on-state losses. In this work, diode with smaller on-state voltage is much important because of the high DC rail current of 5 A. Thus, SiC diode STPS20H100CT is used as a secondary side rectifier.

4. Transformer Design

The main goal of the transformer design is to convert the primary voltage to the desired output voltage with high conversion efficiency and reliability. The induced voltage in a transformer is dependent on the changing of the magnetic flux. Therefore, the size of the transformer becomes smaller if more flux changes occur. Hence, improved the conversion efficiency. Thus, it can be seen frequency has become a strategic variable. In a high voltage input SMPS, the choices of operating frequencies is limited by the used of the semiconductor and the switching frequencies up to 300 kHz can be found nowadays [31]. The operating frequency is only a few tens of kHz in many of application due to the EMC regulations [31]. These requirements can easily be met in the frequency area below 150 kHz [31]. However, difference level of consideration comes to play with higher frequency such as the core saturation, core loss and eddy current. In most SMPS application using ferrite core, hysteresis losses dominated at operating frequency of 200 – 300 kHz and then will take over by eddy current losses at more higher frequency [32]. The core material selection is driven by the core saturation considerations for power circuit operate at lower frequencies and vice versa.

In this work, the proposed circuit operated at switching frequency of 50 kHz. The design of the transformer is derive based on the geometric constant k_gfe method [28]. The saturation flux density B_sat and the peak ac flux density ΔB will be used to choose the appropriate core. The preferred core material for power transformer are F.L.P,R and T [33] and the ferrites of the 3CXX series is mainly used under saturation limit condition [31]. Thus, the P material core is chosen because it is available in almost all core sizes and shapes. The ferrites 3C90 grade is used as most preferably material applied for power transformer [34].Next, the pre-determine core shape is 43434 ETD based on the provided typical power handling chart [31, 33].The ETD shape is considered because ETD's offered round center post for minimum winding resistance, optimized for power transformer efficiency and economical. However, the most important is due to the excellent winding flexibility which much suitable for manual winding[35]. The suggested core size for ETD's shape are ETD29, ETD34, ETD39 and ETD44. Besides that, the core size also can be determine by the core geometry constant k_gfe. There are four ETD's cores suggested. Thus, the core geometry constant k_gfe is used to determine the much suitable size of core. The calculated k_gfe is then compared to magnetic design table [28]. However, sample of design calculation shown is only for ETD44 core. The core loss coefficient k_feis

$$k_{fe} = \frac{P_{fe}}{B_{max}^{\beta} A_C l_m} \quad (7)$$

The maximum flux density B_max can be found from the graph on page 30 [34]. Then, the expected core loss P_fe is determine from the figure 6, page 85 [34]. The typical value of core loss exponent β for ferrite is 2.6 or 2.7 [28]. The cross sectional area A_C and magnetic path length l_m is determine from the ETD core data table [28]. The core geometry constant k_gfe value is derived to determine the suitable core by using the equation of

$$k_{gfe} = \frac{\rho \lambda_1^2 I_{tot}^2 k_{fe}^{(2/\beta)}}{4 k_u (P_{tot})^{((\beta+2)/\beta)}} 10^8 \quad (8)$$

The typical value of wire effective resistivity ρ is 1.724×⟦10⟧^(-6) Ω-cm and typical winding fill factor k_u is between0.25 ~ 0.3. Assume that the primary voltage is square wave. Thus the primary volt-second is

$$\lambda_1 = V_p d_1 T_S \quad (9)$$

The expected peak primary winding current I_tot can be calculated by using transformer transformation ratio. Next, the allowed total power dissipation P_tot is assumed. In this work, the assumption of P_tot is 0.5 Watt. Therefore, the calculated k_gfe is 0.0033. Then, it is necessary to check the peak ac flux density ΔBnot to exceed the maximum flux density B_max.

$$\Delta B = \left[10^8 \frac{\rho \lambda_1^2 I_{tot}^2}{2 k_u} \frac{MLT}{W_A A_c^3 l_m} \frac{1}{\beta k_{fe}} \right]^{\frac{1}{\beta+2}} \quad (10)$$

The core window area W_A and mean length per turn MLT of ETD44 core is from ETD data table [28]. In this work the calculated ΔB is 137.6 mT which is less than B_max of 300 mT. Then, the number of primary turn is

$$N_1 = \frac{\lambda_1}{2 \Delta B A_C} 10^4 \quad (11)$$

The number of secondary turn is determined using transformation ratio equation. Note that the expected secondary side voltage is slightly higher than load voltage which include the voltage drop at secondary rectifier diode and voltage drop at output inductor L_o. Thus, the calculated number of primary winding is 27 turns while 5 turns for secondary winding. However, secondary side is center tapped. Thus, total number of turn is 10 turns. Then, assume that transformer at ideal condition and high full load power factor of 0.99, the calculated input

current is 0.878 A. Then, the fraction of primary α_1 and secondary α_2 winding window area for each winding is calculated.

$$\alpha_1 = \frac{N_p I_p}{N_p I_{tot}} \quad (12)$$

$$\alpha_2 = \frac{N_s I_s}{N_p I_{tot}} \quad (13)$$

Hence, the wire size are

Primary winding: $A_{W1} \leq \frac{\alpha_1 k_u W_A}{N_p}$ (14)

Secondary winding: $A_{W2} \leq \frac{\alpha_2 k_u W_A}{N_s}$(15)

Thus, A_W1 is 7.89×⟦10⟧^(-3) ⟦cm⟧^2 (1.109) and A_W2 is 0.182 ⟦cm⟧^2 (18.2). Therefore, from the AWG table, the primary winding will be AWG17 and AWG5 for secondary winding. However, the maximum amps for chassis wiring is higher than required. Hence, smaller diameter of wire can be used. In addition, stranded wire has to be considered to reduce skin effect and ease of winding especially winding manually. Thus,

A_W1 → 10 ×0.28 mm enamelled copper wire

A_W2 →29 ×0.5 mm enamelled copper wire

Figure 2 shows the cross section of core and winding diagram while the winding direction is depicted as in Figure 3.

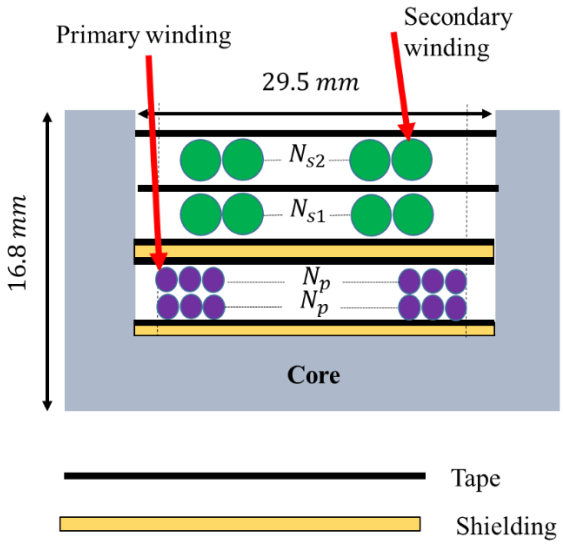


Figure 2: Transformer winding diagram

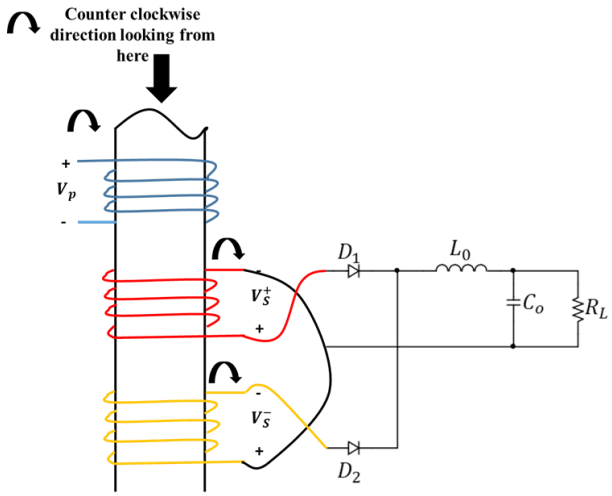


Figure 3: Transformer winding direction

5. Boost Inductor Design

The boost inductor is design based on the k_g method [28]. However, the available toroid is EPCOS-B64290L0632X035 with N30 ferrite core material. Thus, step to determine the core and size can be excluded. is used because of its availability. The boost inductor L_1and L_2 shared the same core. The number of winding will be the same because of same values for both inductor.

$$n_1 = n_2 = \frac{LI}{B_{max}A_c}10^4 \qquad (16)$$

The wire size formula is the same as equation (14). By referring to the datasheet, the calculated values of winding is 22 turns with wire size of AWG12. However, in this work, 10 pieces of 0.28 mm stranded wire is used because of the availability and to reduce skin effect.

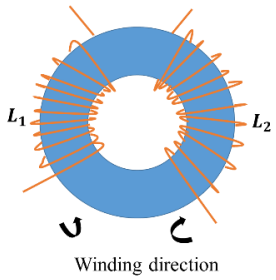


Figure 4 : Boost inductor winding direction

6. Overall Circuit Configuration

The main objective of this work is to verify the proposed circuit topology experimentally. Thus, simple voltage feedback controller is used to regulate the output voltage. The isolation between the output voltage rail and the controller is through the optocoupler 4N25. In this work, typical value of optocoupler diode current is 10 mA with maximum forward voltage of 1.35 V is used as provided in datasheet. The resistance R_1can be calculated by applying Kirchoff voltage law. The SG3525 PWM is used to provide the signal in order to drive all four Mosfet's. The SG3525 PWM IC has a build in proportional integral (PI) compensator, signal generator and generated two output to drive power switches. The SG3525 IC's is choose because of the simplicity to apply the designed control system. The PI compensator components values is as calculated in equation 17. The variable resistor is used to tune the value of resistor R_PI approximately. The switching frequency can be set by using appropriate values of R_T and C_T which depicted in equation (18)[36]. The resistor R_D is to determine the dead time.

$$\frac{K_i}{K_p} = \frac{1}{R_{PI}C_{PI}} \qquad (17)$$

$$f_s = \frac{1}{C_T(0.7R_T+3R_D)} \qquad (18)$$

In this work, the TLP250 is used to isolate between the SG3525 controller outputs and high side driver IR2117. Resistor R_3 and R_4 is to limit the forward current of the signal diodes D_3 and D_4. Thus, by referring to typical forward current in diode datasheet, the resistor R_3and R_4is choose to be 100 Ω. In addition, the 10 Ω of resistor is used for R_6 and R_7 . This to limit the current flow to the input of high side driver IR2117.

The resistor and diode between pin 1 and pin 4 of IR2117 is to form the boothstrap supply. This boothstrap method is simple and low cost. However, the duty cycle and on time are limited by the requirement to refresh the charge in the boothstrap capacitor. Therefore, proper capacitor choice can reduce this limitation. The estimated C_Boot capacitor is

$$C_{Boot} = \frac{Q_{Tot}}{\Delta V_{BS}} \qquad (19)$$

ΔV_BS is voltage drop at boothstrap capacitor which can be estimated with Krichoff voltage law. The total charge of the boothstrap circuit Q_Tot is determine from the datasheet. In this work, 5 Ω is choose as boothstrap resistance, 0.5 nF of bothstrap capacitor and boothstrap diode of 1N4007.

7. Measuring Equipment And Setup

The purpose of the practical implementation is for verification of the simulation result for the new propose circuit topology. It can be done with the observation of the main current or voltage waveform such as supply current and voltage, switching waveform and output current and voltage. Thus, the Rigol DS1102E digital oscilloscope is used together with Textronix A622 current probe, Textronix P5200 high voltage differential probe and normal voltage probe. The main power supply of GW Instek APS-9501 is used to provide input voltage V_s at 115 V_rms with line frequency of 50 Hz and 500 Hz. In addition, it measured the input power and power factor. The purpose of input voltage V_s with line frequency at 500 Hz is to verify that the input current distortion at the zero crossing is minimized when operate at higher line frequency. The Voltech PM1000 Power Analyzer is used to measure the input harmonic current, input power and power factor. The harmonic

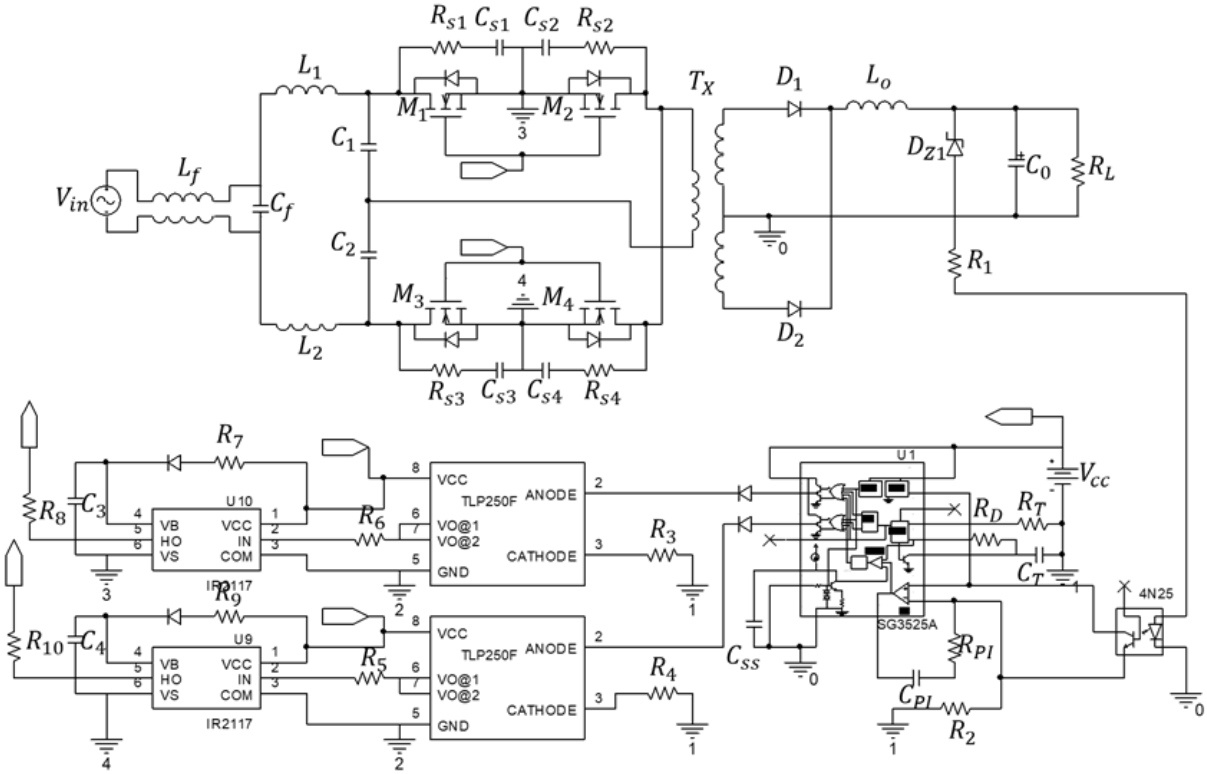


Figure 5 : Overall circuit configurations converter block diagram in PLECS

current is measured up to thirty ninth harmonic level as required by IEC 6100 -3-2 harmonic standard. The experiment workplace is shown as in Figure 6 and Figure 7 shows the implemented new circuit topology on the PCB.

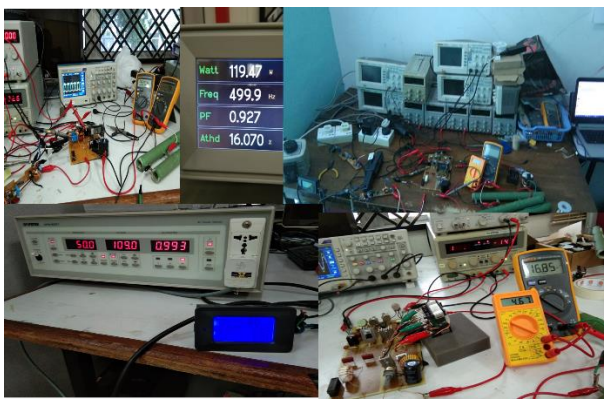


Figure 6 : Workstation and equipment

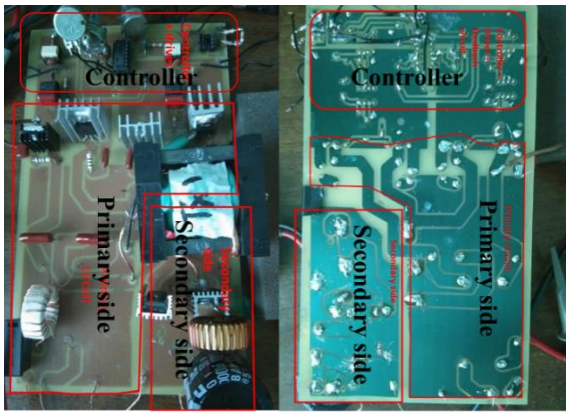


Figure 7 : PCB circuit design

8. EXPERIMENT OBSERVATION

The proposed circuit topology working principles is confirmed. The switching waveform shows good agreement as compared to the simulation result in Figure 8. Figure 9 shows some of the switching waveform experimentally.

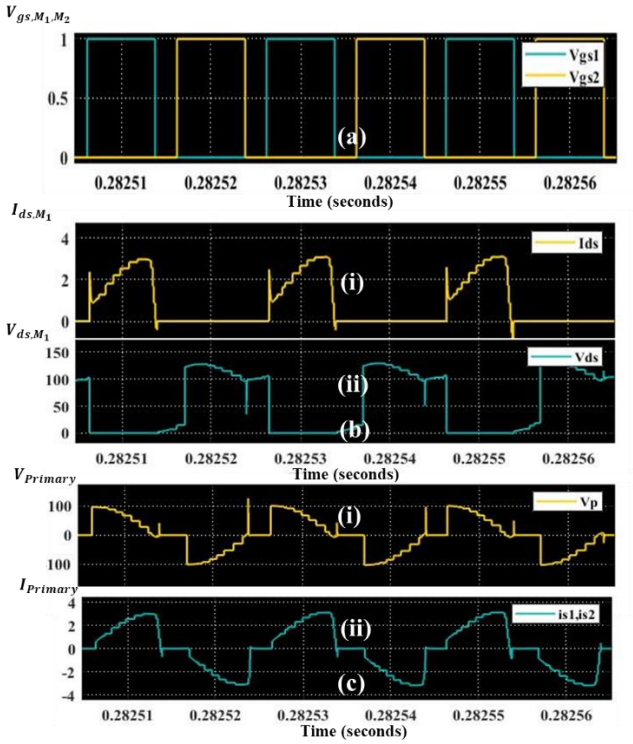


Figure 8 : (a)Gate drive voltage (b)Drain to source (i)voltage V_ds; (ii) current I_ds (c)Transformer primary (i)voltage V_primary (ii)current I_primary

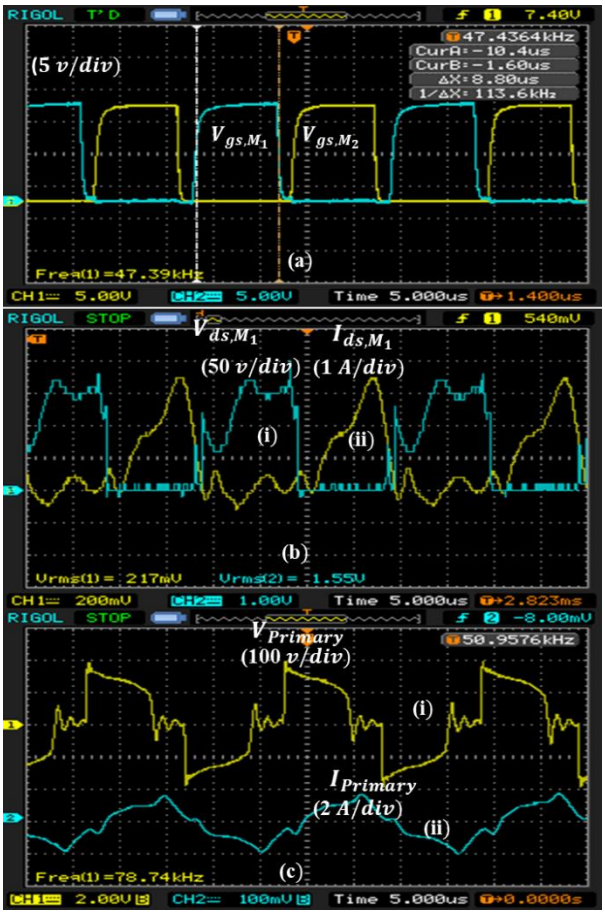
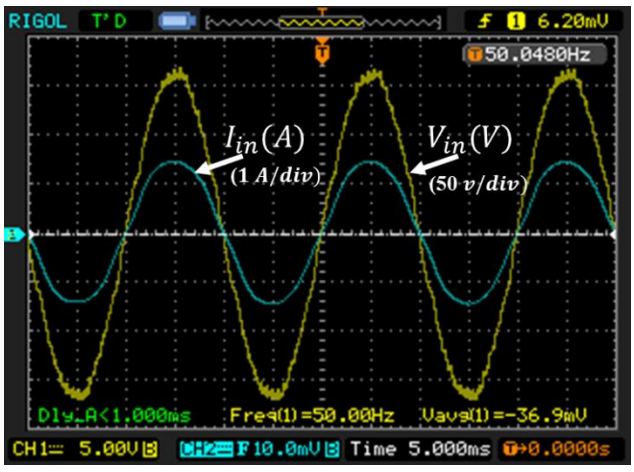
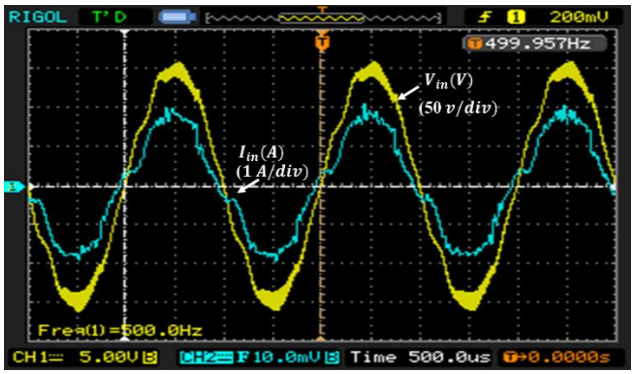


Figure9 : (a)Gate drive voltage (b)Drain to source (i)voltage V_ds; (ii) current I_ds (c)Transformer primary (i)voltage V_primary (ii)current I_primary



(a)



(b)

Figure 10 : Input voltage and input current at (a) 50 Hz (b) 500 Hz

It is also confirm that the proposed circuit has achieved maximum power factor of 0.99 at full load. In addition, no zero current crossing when operated at higher frequency of input supply 115 V_rms,50 Hz as shown in Figure 10(a). In Figure 9(b), the effect of current distortion at zero crossing is also minimized

The output voltage ripple as expected from the design calculation is observed. The measured output voltage ripple is ΔV_o; 1.60 V as depicted in output voltage waveform in Figure 11. Thus, it shows good agreement between voltage ripple from the experimental 8% and calculated 10%.

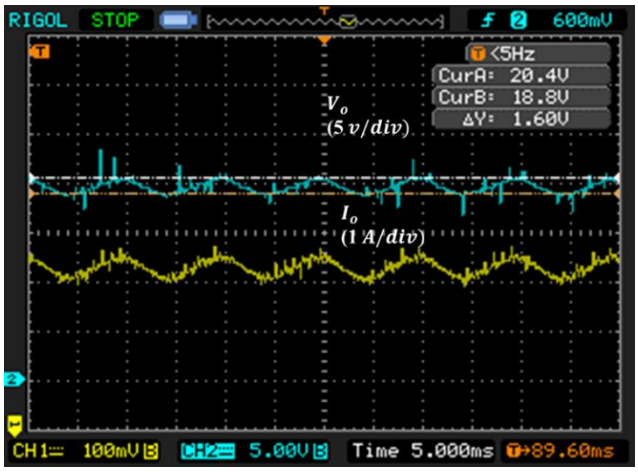


Figure 11 : Full load output voltage and output current

The input current harmonic is measured by Voltech PM1000 Power Analyzer up 20 39th harmonic level. Figure 11 shows the measured input current harmonic as compared to the IEC 6100 -3-2 harmonic standard. It shows that the measured input current harmonic level complied to the standard as depicted in Figure 11.

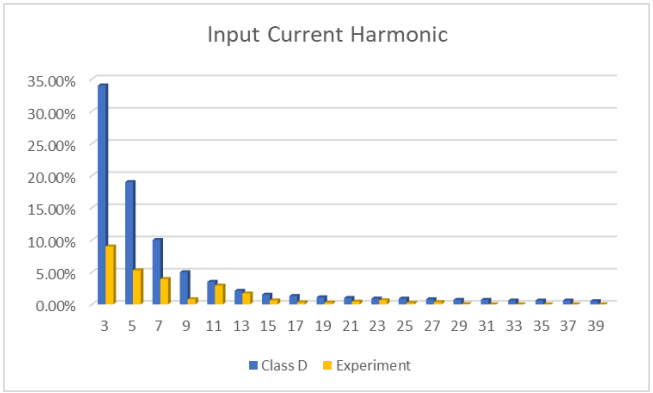


Figure 11 : Input current harmonic compared to the IEC 6100 -3-2 harmonic standard.

9. Conclusions

The proposed Bridgeless AC-DC half bridge circuit topology has been tested experimentally. The design calculation of the main power circuit components is then discussed. The magnetic components design calculation is discussed with supported by the winding diagram. The overall implemented circuit configuration is then explained. Then, the measuring equipment's used is list out followed by the actual workstation environment and the PCB board design. The observed experiment results is then presented to validate the design calculation. The results shows that good agreement between the expected design calculation and experiment. The measured full load power factor is 0.98 and no zero crossing of the input current at line and higher frequency of input supply. The full load output voltage ripple is below the expected in design calculation. Thus, the new proposed circuit topology has been practically implemented at input supply of 115 V_rms ;50 Hz and 500 Hz with full load output of 20 V_dc,5 A..

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