# Design and Analysis of 7 Level Multilevel Inverter for Industrial Applications

**Dr. R. Arulmozhiyal[a], Dr. M.Murali[b], and K.R. Manjeri[c]**
**a,b,c**
Department of EEE, Sona college of Technology, Salem, India.

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**Abstract:** Multilevel inverters are extensively implemented in high power and voltage applications because of its lower THD, lower switching stress over its switches etc. However, to obtain to lower THD the number of stages has to be increased. As a result, the size becomes bulky. Hence, to reduce this problem, this work formulated a new 7 level CMLI with reduced switches. This topology designs 7 level MLI with 6 switches and produce same output as that of conventional one. SVPWM technique is instigated to generate gate pulse to the switches. Finally the performance of this designed work is validated in MATLAB simulation. From the analyzed results, it is found that this proposed topology. Will results in better harmonic reduction, with lower number of switches.

**Keywords:** inverter, multilevel, MATLAB

## 1. Introduction

The application of conventional VSI in medium and high power/ voltage application results in poor efficiency. This is mainly due to power loss across the switches of the inverter as they have some limitations over high voltage applications. Hence, to get rid of this problem, MLI's was introduced. These inverters are more effective for both high and medium voltage applications. So the implementations of MLI's in industries have been increased. However, when the levels of the MLI increases, THD will be reduced. But the usage of power modules in the MLI gets increased. This in turn leads to complexity in isolation between switches and power supply. Hence, to overall all these problems, this work proposed a new 7 level cascaded MLI with reduced switches. Thus, numerous topologies have been so far introduced with reduced number of switches [9-17]. Khounjahan et al. 2015 introduced cascaded transformer MLI. It includes a DC source with single phase low-frequency transformer, 2 power switches and some additional bidirectional switches. In this, one bidirectional switch is employed for each transformer. Ebrahim Babaei et al. 2015 formulated a new cascaded MLI. In this, 5 different algorithms were adopted to generate voltage at the output. A 17 Level flying capacitor inverter and cascaded H-Bridge modules with floating capacitors has been introduced by Roshan Kumar et al. 2015. Thus, this proposed topology utilizes 6 switches to generate 7 level output. In this, CMLI is chosen because of its high efficiency over other two MLI topology. SVPWM technique is incorporated to produce gating signal of the switches. This formulated MLI comprises only 6 switches to produced 7 level output voltage.

## 2. Conventional 7 level CMLI

The conventional level CMLI is depicted in figure 1 consists of power electronics switches arranged in bridge form with input of single phase-power supply.

$n = (M - 1)/2$ (1)

Where, M – Level of CMLI, n- Number of H bridge/ phase

The conventional CMLI includes 3 H Bridge connections and hence, total 12 switches are utilized to produce the output.

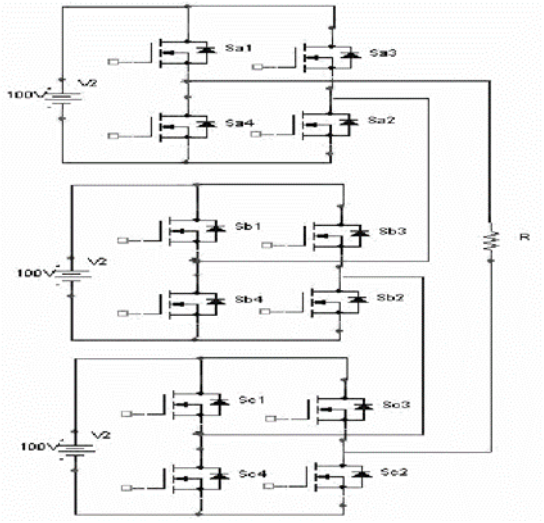


Fig.1 Conventional7 level MLI (Single phase)

**3. Design of proposed CMLI topology**

The design of MLI proposed in this work is depicted in figure 2.

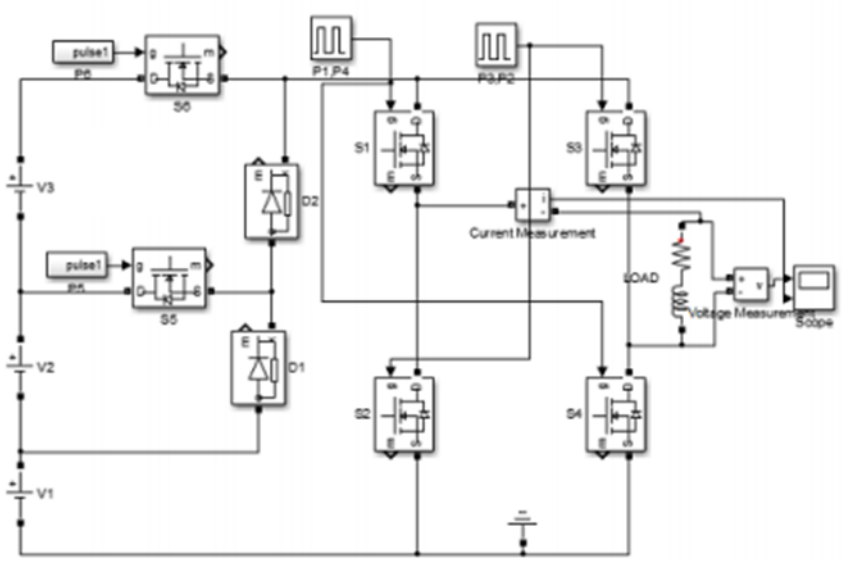


Fig. 2. Single phase 7level MLI with CHB

In this topology, 6 MOSFETS are used for single phase. 4 MOSFETS are used in H-bridge for changing the polarity and 2 MOSFETS are used for level generation. It provides 7 output voltage levels (3V, 2V, V, 0, -V, -2V, -3V). For 3V output voltage, MOSFETS (S1, S4 and S5) are in ON condition and others remains switched off. For 2V output voltage, switches (S1, S4 & S6) are in ON condition and others remain OFF. Similarly for output voltage (V), MOSFETS (S1and S4) remains ON and others are in OFF state. Thus the switching scheme of the proposed MLI is given in Table-1.

Table .1: Switching scheme for 7-level 6-switch topology

| **S.NO** | **$S_1$** | **$S_2$** | **$S_3$** | **$S_4$** | **$S_5$** | **$S_6$** | **Output voltage** |
|---|---|---|---|---|---|---|---|
| 1 | OFF | OFF | ON | OFF | ON | OFF | +Vdc |
| 2 | OFF | ON | OFF | OFF | ON | OFF | +2Vdc |
| 3 | ON | OFF | OFF | OFF | ON | OFF | +3Vdc |
| 4 | OFF | OFF | OFF | OFF | OFF | ON | 0 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 5 | ON | OFF | OFF | ON | OFF | OFF | −Vdc |
| 6 | OFF | ON | OFF | ON | OFF | OFF | −2Vdc |
| 7 | OFF | OFF | ON | ON | OFF | OFF | −3Vdc |

From the table, it is observed that only two switches remains ON during conduction. So switching loss is greatly reduced.

**4. Modulation Technique**

SVPWM technique has widespread PWM technique utilised in many applications such as control of IM, PMSM etc.,.It is a sine wave technique with lower THD. In this, the 3 quantities are transformed into 2 quantity using a stationary frame topology. From this obtined values, magnitude of the the reference vector is calculated and is utilised for generation of gating signals.

Thus the realization of SVPWM is carried out using the steps depicted below

1.Determine, an angle (α) ,Vd, Vref and Vq

2. Determine time required for each sector

3. Finally, Compute switching time of each swithches in the VSI.

Thus, Whenever either upper/lower switch of a specific phase is ON , then it can be denoted as '1' or '-1'. Correspondingly, when the switch is in OFF state, then it can be considered as '0'. According to these combinations, 8 switching vectors, line to neutral voltage and output line-to-line voltages are produced in SVPWM topology.

**5. Results And Discussion**

Based on simulation examine the performance of this projected topology, it is simulated in MATLAB environment. The simulation result and THD of the proposed topology is shown below. Figure 3 shows the output voltage of the proposed topology. The magnitude of the voltage is about 230 volts. The THD for the output voltage is about 17.98% and is shown in figure 4.

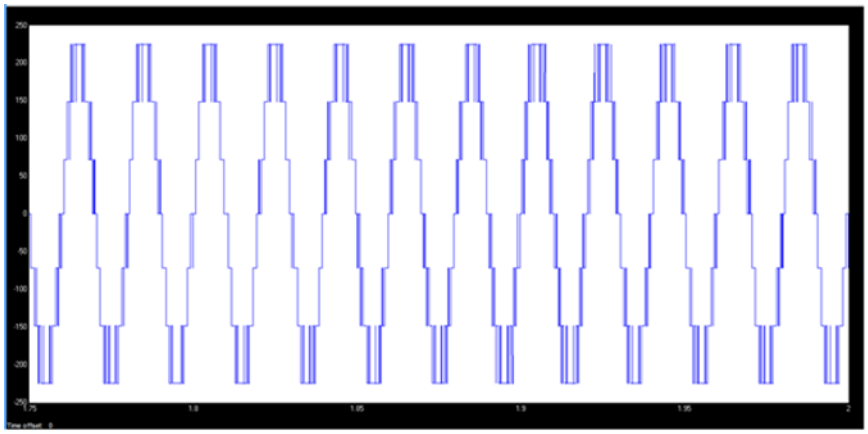

Figure 3: Output voltage

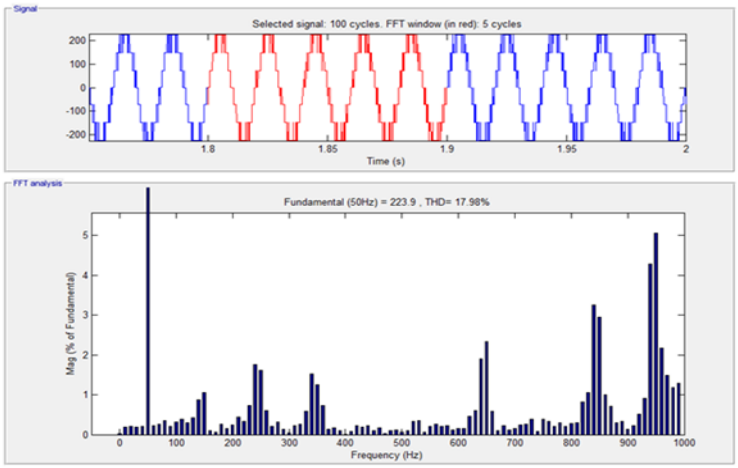


Figure 4: Output voltage waveform THD

Table 2 represents the THD results obtained for conventional and proposed MLI configurations.

Table 2. THD of conventional and proposed MLI configuration

| **Conventional CMLI** | **Proposed** |
|---|---|
| 24.26 | 17.98 |

Simulation results presented in table 2 reveals that THD is reduced to 17.98 %. Table 3 discuss about the voltage stress over the switches and Table 4 shows the comparison of proposed topology with other topology based on its structure.

Table 3. Voltage stress across the switches

| **Conventional CMLI** | **Proposed topology** |
|---|---|
| 5V (over all switches) | 3.32V (S3)<br>13.2V (S2)<br>23.2V (S1) |

Table 4. Comparison of proposed topology with other MLI topology

| **Inbuilt structure** | **Flying capacitor** | **Diode clamped** | **Cascaded 7-level** | **7-level, 6 switches** |
|---|---|---|---|---|
| No. of capacitors | 14 | 6 | — | — |
| No. of diodes | — | ≥8 | — | — |
| No. of switches | 10 | 10 | 12 | **6** |
| No. of dc sources | — | — | 3 | **4** |

From the above tables, it is clearly observed that the proposed topology exhibits more advantages over the conventional topology.

## 6. Conclusion

This topology designs 7 level MLI with 6 switches and produce same output as that of conventional one. SVPWM technique is instigated to generate gate pulse to the switches. From the results, it is evident that this proposed system reduces switching losses with less THD. Thus, the overall cost reduction and effective reduction of total harmonics distortion is achieved.

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