A Reduced Switch Count and THD Analysis in Cascaded H Bridge Multi-level inverter Topology

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Abstract: Designing of a multilevel inverter is required for power conversion with good efficiency, less switching loss, less THD values related to voltage and current . In a multi-level inverter, the desired output value depends on the harmonic values so as to increase the levels in output. This paper presents a 9-level cascaded H bridge inverter and a reduced number of switching devices.The developed H bridge inverter is analyzed in terms of THD values at different loads. The developed H bridge inverter is compared with PD,POD,APOD techniques in terms of THD values. Based on simulation results it has been observed that the developed H bridge inverter system performs well in terms of voltage and current THD values and achieve good efficiency due to less loss.

Keywords: Multilevel inverter, PWM Switching loss ,THD

1. Introduction

NOW a days, there is a huge demand for industrial automation, automotive and robotic systems that can be controlledbymobilityduetoenergyconversionandmaintain the high efficiency of the batteries used in these devices. Thus, in this issue, the inverters implemented on the multi-level inverter show that many advantages compared to the 2-level inverter, lower order harmonics can be reduced because the output voltage levels areincreased[1],[3].

Many multi-level inverter topologies have been proposed for industrial applications, providing efficiency in power quality andtheremainingonesarestillunderprocessing.Multi-level inverters are mainly divided into three types[11]: diode clampedinvertersystem,flyingcapacitorinvertersystemand cascadedHbridgeinvertersystemsbasedontherequirements and optimal conditions of the multi-level inverter topology systems[4]. While cascaded H bridge inverter is well known for having a novelty circuit to provide high efficiency , lower switching losses and lower order harmonics are compared to the diode clamping and flying condenser topologies[2],[5]. Despite the above mentioned advantages, in the case of cascaded H bridges, consideration has been given to the fact that higher switching and conduction losses are mainly due to the use of anti parallel diodes.[4] In many researchers there is little effort to reduce power switching devices and power converter applications, which have been found to be challenging due to the improvement of longer battery usage[9],[10].

In the multi-level inverter topology application, decreasing thenoofpowerswitchesandharmonicvalues.Thelessnoof main power switching devices to improve efficiency and the cost of implementing inverter systems are issues that many researchers consider focused on developing battery life and reducing cost functions due to the use of programmable ICs[6],[7].

Contribution of the paper including details

- In this paper, different THD values were analyzed using different loads and reducing power switchingdevices.
- In this cascaded H bridge inverter system, the results were developed and compared with the different PD.APOD, POD and current THD values.
- Remarks the reduced switch count method has higherTHDvaluesbyvaryingthedifferentload values of the THD voltage values as well asthe current THDvalues.

The remaining part of the paper is as follows: Section II describes the system that has been developed. Section III& IV presents the results of the simulations and the comparison analysis and conclusion of this study is provided in Section V.

2.System Discription

A. Cascaded Nine level invertertopology

One of the converter topologies is implemented here, which is based on a single-phase nine-level inverter series with dc sources[8]. Each one of the single phase full bridge produces 3 different values are +VDC,0VDC,-VDC and power circuit for one phase leg of this inverter with four cellsineachphase.

Resulting voltage is synthesized by adding theabove

voltages: +4vdc,0,-4vdc.Fig.1 shows the nine level inverter topology without filtering circuit.

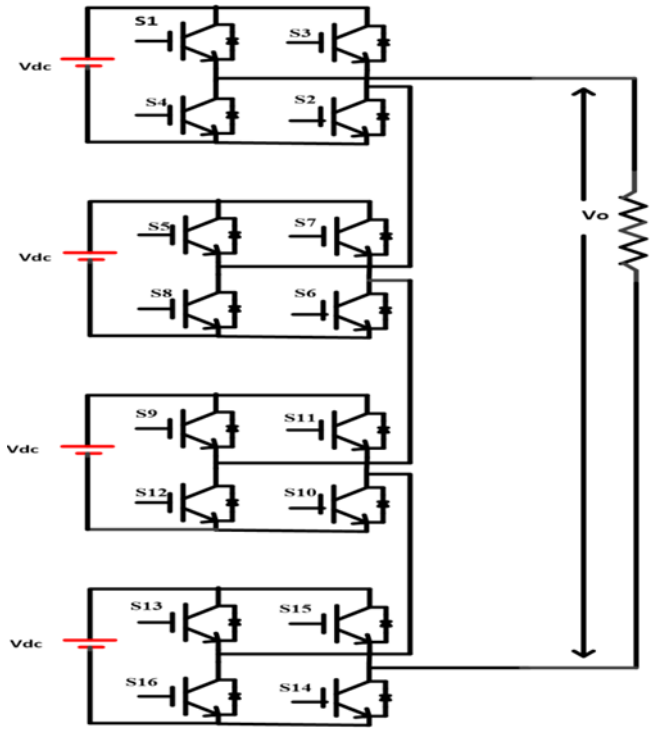


Fig. 1. Circuit diagram for cascaded H bridge multi level topology

Operating strategy in this circuit can be A PWM based on POD, PD, APOD modulations. PWM technique comparing one sine signal to four carrier signals if the reference signal is positive when the H bridge switches …..are in position and the reference signal is negative when the H bridge switches ….are in off position. Turns off the H bridge switches operated during the reference signalperiod.

1. PHASE OPPISITION DISPOSITION (POD) In POD modulation method, all carrier signals are in phase with a reference signal above zero and are 180 degrees out of phase with reference signal above zero. If number of level is m then (m-1) the carrier waveforms are arranged in phases above zero reference signal and out of phase at 180 degrees below zero reference signal. If the inverter switched to + Vdc/4 then the reference is high value compared to carrier signals, the inverter switched to Vdc=0 than reference is greater value than lower carrier waveform but less value than upper carrier waveform, inverter switched to – Vdc/4 when reference is less value than two carrier waveform signals.

2. PHASE DISPOSITION(PD)

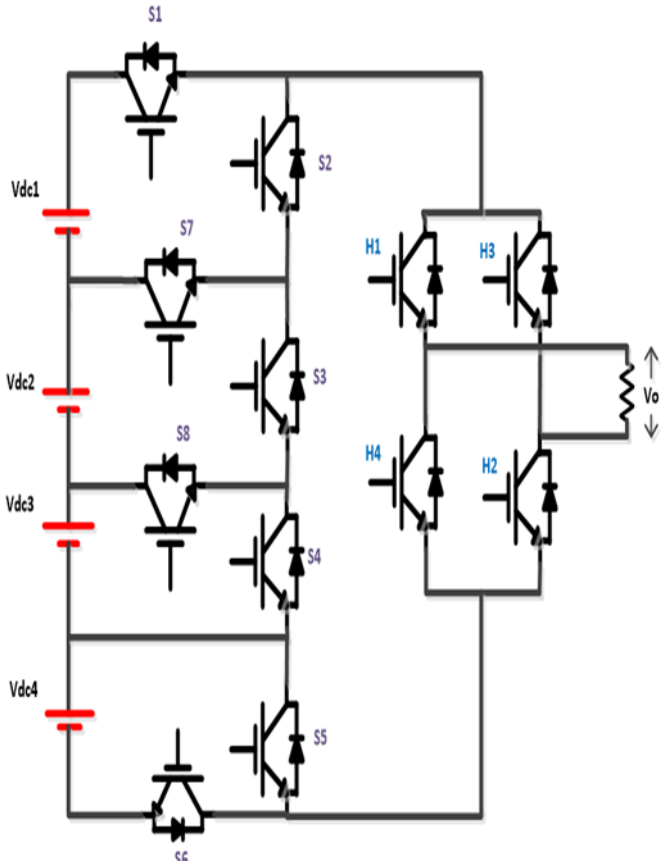
All carrier signals are in phase with the above zero reference signal in the PD modulation technique. If number of level is m then (m-1) the carrier waveforms are arranged in the reference signal phase. If the inverter is switched to +Vdc/4, then the reference is high value compared to carrier signal, the inverter is switched to Vdc=0,then the reference is high value or less value than the reference signal, and the inverter is switched to – Vdc/4, then reference signal is less thanthe reference signal in this way.

3. ALTERNATIVE PHASE OPPOSITION DISPOSITION (APOD)

In APOD modulation, each carrier waveform is out of phasewith180degreesbelowthecarrier.Inthismethod, when considering positive half-cycle + Vdc/4 the reference is high value compared to all carrier signals and Vdc=0 reference is greater than the upper reference signals and lower than the lower reference signals and + Vdc/4 the reference is less than the uppermost carrier waveform and greater than all other carrier waveforms. In this way, the same controlled applied in the negative half-cycle.

B. Nine Level Inverter With Reduced SwitchCount

Figure 2 shows the system developed MLI less no with reduced power switching devices. This system having 4Vdcs, and 4 H bridge connections (H1,H2,H3,H4) and 8 active power devices S1 to S8. H bridge switches , dc link switches can be selected at the basis of rated multi-level inverter power to reduce cost functions and improve system efficiency.



levelinverter

Operating switching modes:

When switching the configuration used to operate this system with different modes. If Vref>=4vc, the active switches(S1&S6) will be switched on. If Vref>=3vc then switches(S2,S6&S7)switcheson,ifVref>=2vcthenswitches (S2,S3,S6&S8)switcheson,ifVref>=vcthenswitches(S2,S3,S 4&S6)switcheson, If Vref<vc then switches(S2,S3,S4&S5) switches on. Table 1 shows switching on and off at different intervals.

Table- I: Switching conditions of the system T*ON, F*OFF

Voltage	S1	S2	S3	S4	S5	S6	S7	S8	H1 H2	H3 H4
4Vdc	T	F	F	F	F	T	F	F	T	F
3Vdc	F	T	F	F	F	T	T	F	T	F
2Vdc	F	T	T	F	F	T	F	T	T	F
1Vdc	F	T	T	T	F	T	F	F	T	F
0Vdc	F	F	F	F	F	F	F	F	F	F
-1Vdc	F	T	T	T	F	T	F	F	F	T
-2Vdc	F	T	T	F	F	T	F	T	F	T
-3Vdc	F	T	F	F	F	T	T	F	F	T
-4Vdc	T	F	F	F	F	T	F	F	F	T

3. Simulation Circuit

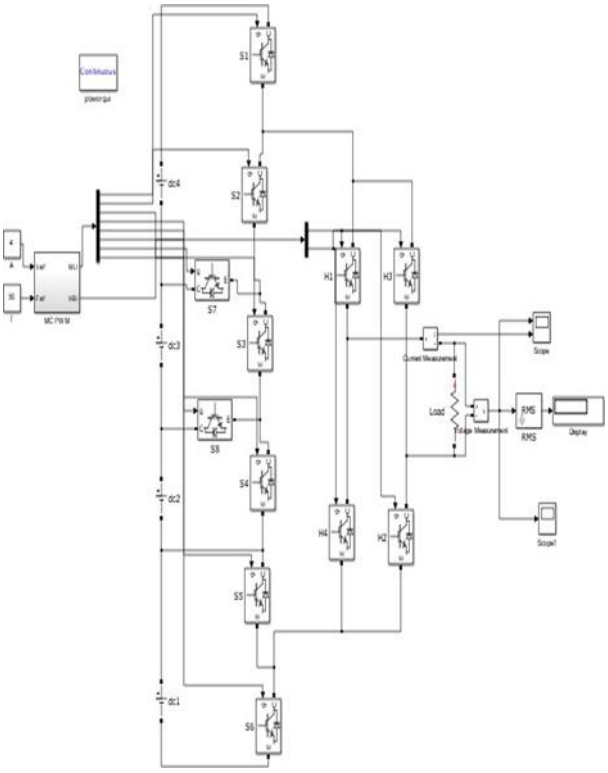


Fig.3.SimulationmodelforReducedswitchcountmultilevel inverter

4. Simulation Results

C. Cascaded 9 Level inverter

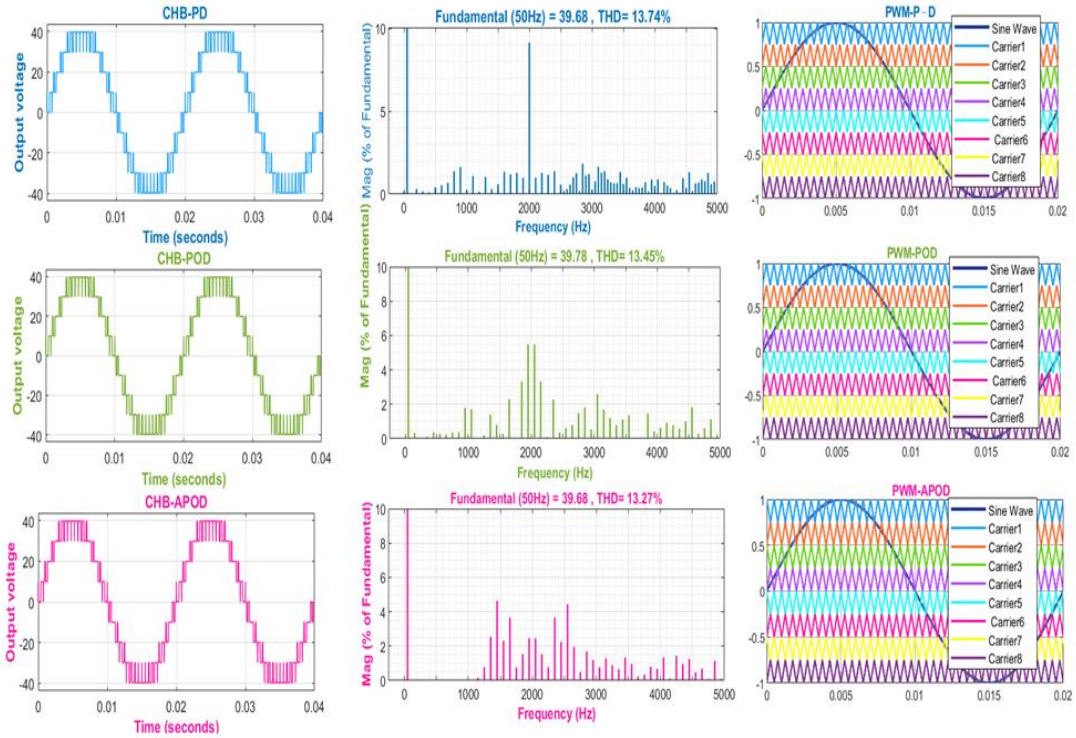


Fig. 4. Output results of Cascaded 9 level H bridge

Performance expressed in this system as THD with different loads.TheFigure4above.Displaystheoutputvoltagesignals with THD values and the respective waveform PD, POD, APOD models. Total Harmonic Distortion (THD) is a very important aspect used in audio, communication

devices , power systems. THD is one of the measurements that shows how much voltage and current distortion is due to the harmonics present in that signal. In general, the pure sine wave is not having harmonic value when the stepped wave forms signals with more harmonic distortion. If voltage and current signals are produced periodic but not exactly sine wave, higher frequency components will contribute to harmonicdistortion.Nowadays,manyresearchpracticesand development methods have been developed to reduce this THD value as low as optimally improve system efficiency. THD values with different loads have been developed in this system and compared to which load is more suitable for the reduction of these THDvalues.

D. Reduced switch countresults

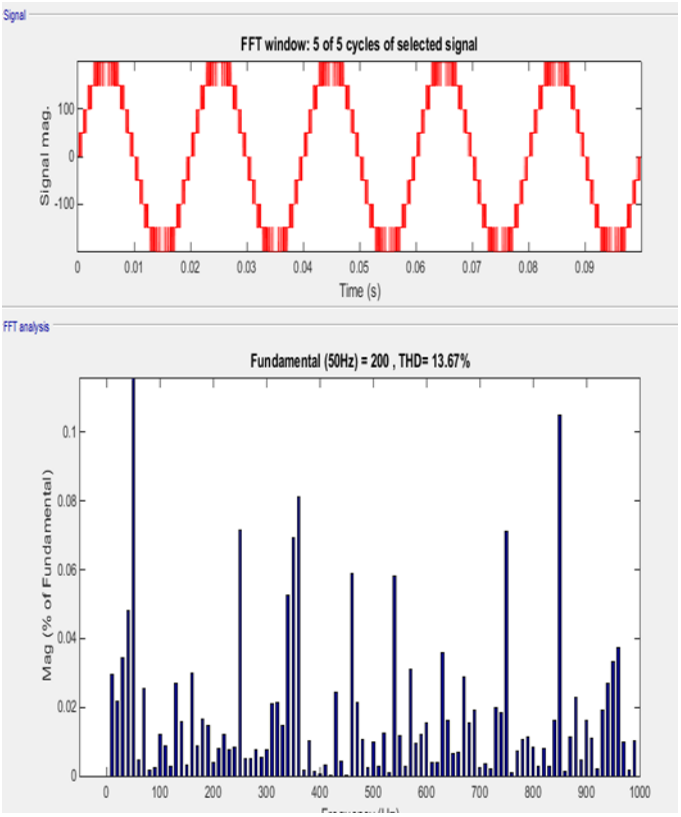


Fig. 5. Output results of Reduced switch count multi level inverter THD 13.67%

RESISTANCE Ohms	INDUCTANCE Henry	VOLTAGE THD	CURRENT THD
10	0	13.69	13.69
10	0.001	13.83	3.47
10	0.01	24.79	5.83
10	0.1	31.39	8.33
10	1	31.6	10.09
50	0	15.72	15.72
50	0.001	15.74	10.26
50	0.01	15.88	3.53
50	0.1	34.53	9.73
50	10	31.93	10.33
100	0	15.72	15.72
100	0.001	15.73	12.53
100	0.1	26.35	6.28
100	1	32.94	8.81
100	10	31.8	10.32

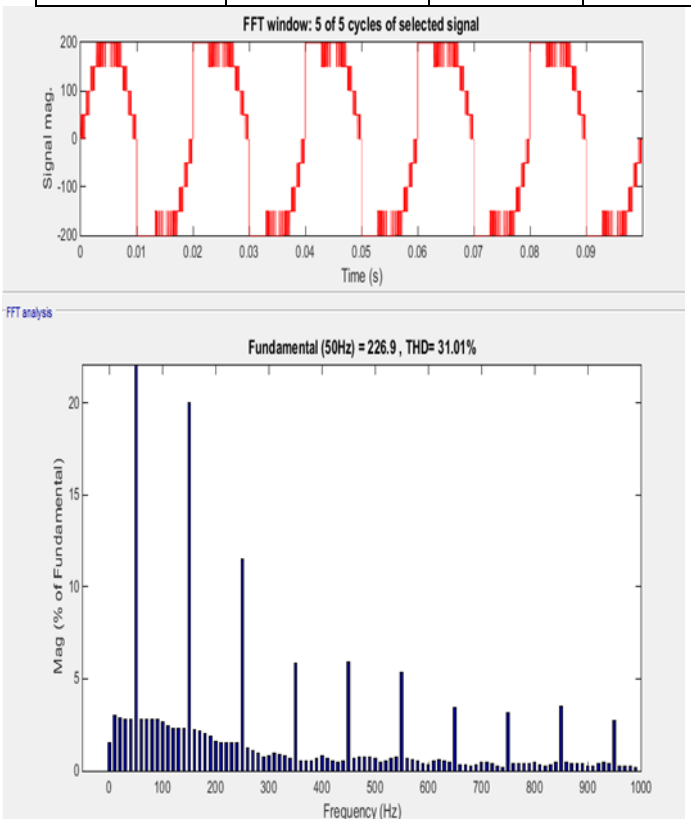


Fig. 6. Output results of Reduced switch count multi level inverter THD 31.01%%

Figure 5&6 shows the different THD values of the Reduced Switch Count method. In this system, the values of load resistance and inductance change output harmonic values accordingly.

Table- II: Harmonic values in Reduced switch count

Table- III: THD Analysis in 9 level inverter

9 LEVEL CASCADED H BRIDGE							
LOAD		PD CONFIGURATION		APOD CONFIGURATION		POD CONFIGURATION	
RESISTANCE (ohms)	INDUCTANCE (henry)	VOLTAGE-HARMONIC	CURRE NT-HARMONIC	VOLTAGE - HARMON IC	CURRE NT-HARMONIC	VOLTAGE - HARMON IC	CURRENT - HARMONIC
10	0	13.73	13.73	17.27	17.27	17.96	17.96
10	0.001	13.74	7.16	17.28	11.33	17.96	11.89
10	0.01	13.74	1.05	17.27	6.67	17.96	6.8
10	0.1	13.73	0.45	17.27	3.34	17.96	3.76
10	1	13.72	4.19	17.27	9.961	17.96	11.7
10	2	13.73	2.69	17.27	11.17	17.96	13.7
10	3	13.73	1.87	17.27	10.82	17.96	15.12
50	0	13.73	13.73	17.28	17.28	17.96	17.96
50	0.001	13.72	12.07	17.27	15.59	17.96	16.39
50	0.01	13.73	4.37	17.28	9.39	17.96	9.71
50	0.1	13.72	0.6	17.27	5.22	17.96	5.3
50	1	13.74	2.27	17.27	7.55	17.96	7.58
50	10	13.72	2.68	17.27	9.56	17.96	12.57
100	0	13.73	13.73	17.28	17.28	17.96	17.96
100	0.001	13.74	12.88	17.27	16.4	17.96	17.15
100	0.01	13.74	7.16	17.28	11.33	17.96	11.89
100	0.1	13.74	1.05	17.28	6.67	17.96	6.80
100	1	13.74	0.45	17.28	3.71	17.96	3.76
100	10	13.73	4.19	17.28	11.76	17.96	11.77

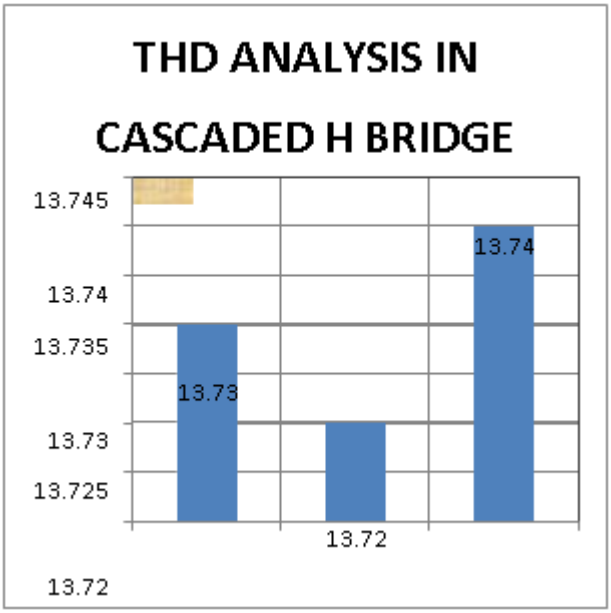


Fig. 7. THD analysis in Cascaded 9 levelHbridge

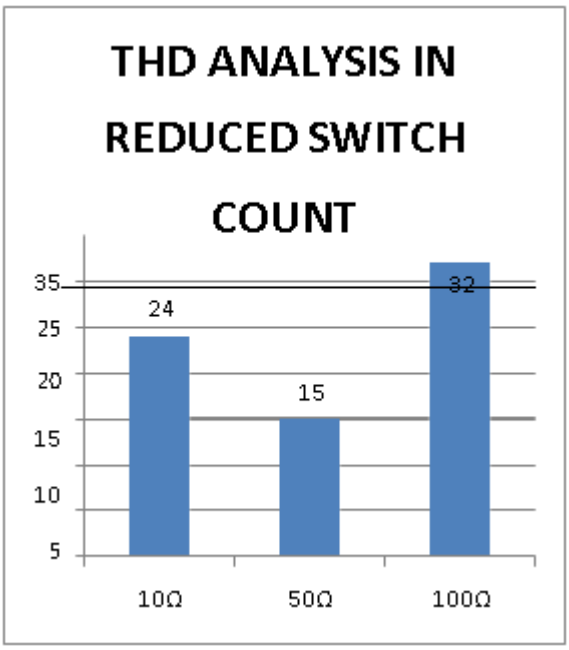


Fig. 8. THD analysis in Reduced switchcount

Figure 7&8 shows the THD analysis in the H bridge cascade and the reduced switch count in the multi-level inverter. Cascaded H bridge topology has been implemented with the production of THD in different PD, POD, APOD models. The THD value changes with the variation of the different load values. In this cascaded method, less harmonics related to voltage and current values are achieved by changing the load inductance and resistance values than no effect of THD voltage harmonics and current THD values are changed, but in this method, switching devices are longer than the reduced switch count method. In a reduced switch count method, considering fewer switches and operating with switching on and off, the THD values are high compared to the previous method. One of the disadvantages of this method is that it varies the load effect of the THD voltage values and the current THD values.

5. Conclusion

In this paper presents cascaded nine level Hbridge multilevel inverter topology was presented by considering the reduced switching device. This system discussed in detail the cascaded H bridge with 16 Switches configuration, producing a 9-level output model in PD, POD, APOD methods, and the extension of this systemwithreduced4Switchescount.Inthissystem,output9 levels with respective THD values are produced in different methods, followed by THD voltage values. Finally, several simulation results shows that suitable of

THD value of the developed H bridge inverter system with different types of loads by considering modulation indexes.

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