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Research Article

Asymmetrical Cascaded H-Bridge Multilevel Inverter For Uninterruptible Power Supply

K. Chitra[a], Viji K[b], M. Lakshmanan[c], P. Ramesh[d]

[a]Professor & HoD, Department of EEE, CMR Institute of Technology, Bengaluru, 560037, India
[b]Assistant Professor, Department of EEE, CMR Institute of Technology, Bengaluru, 560037, India
[c]Associate Professor, Department of EEE, CMR Institute of Technology, Bengaluru, 560037, India
[d]Associate Professor, Department of EEE, CMR Institute of Technology, Bengaluru, 560037, India

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Abstract : Cascaded H-bridge multilevel inverters (CMLI) have become very popular, because they are able to generate voltage waveforms with negligible waveform distortion. The number of isolated input dc sources and switching devices are very high in conventional CMLI to get high levels. This paper presents an Asymmetrical Cascaded H-bridge Multilevel Inverter (ACMLI) which varies from the conventional cascaded multilevel inverter (CMLI) based on the number of sources and power devices used. The 27 level ACMLI is proposed for Uninterruptible Power Supply (UPS) which has only 3 input dc sources and 12 switching devices when compared to conventional twenty seven level CMLI. The 27 level ACMLI multilevel inverter for UPS application is simulated using MATLAB/simulink software and the results are obtained. The hardware prototype for the single phase 27 level ACMLI multilevel inverter is designed and implemented. The simulation results are validated with hardware results.

Keywords: Multi level inverter, cascaded H bridge multi level invreter, UPS, THD

1. Introduction

The main objective of this paper is to obtain twenty seven level output with reduced number of sources and switching devices and to apply it for Uninterruptible Power Supply (UPS) system. The multilevel inverters (MLI) can produce the output voltage with low dv/dt and low distortion; high efficiency because of less number of switches; used for high power applications; less voltage stress; and lesser electromagnet interference (EMI) problem. There are three types of MLI which is shown in Fig. 1 [1].

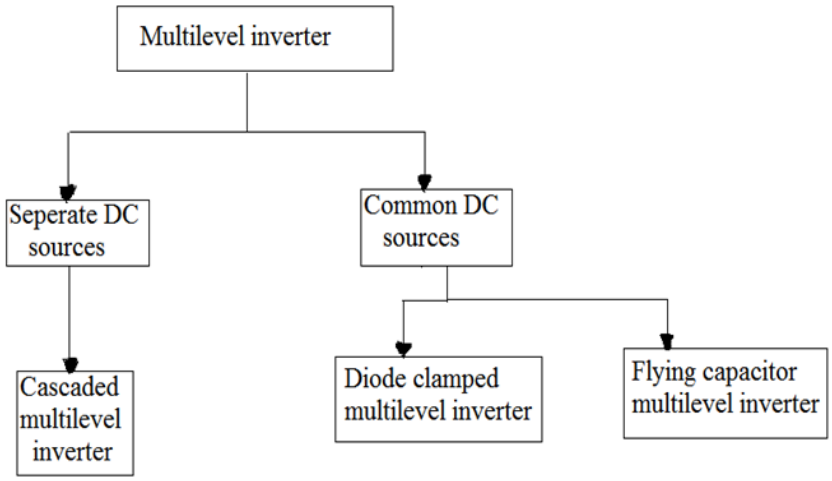

Fig. 1. Types of multilevel inverter (MLI)

The cascaded MLI (CMLI) topology is mostly used which consists of H-bridges, isolated independent dc sources. The output phase voltage is obtained by adding the voltages of H- bridges [2]. The output voltage can be increased with the help of different voltage level dc sources without clamping diodes and capacitors. This CMLI requires a separate dc source, hence reduces the applications [3]. Hence this paper proposes Asymmetrical Cascaded H-bridge Multilevel Inverter (ACMLI), with less number of switching devices and sources. The block diagram of 27 level ACMLI used for UPS is depicted in Fig. 2 [4-5].

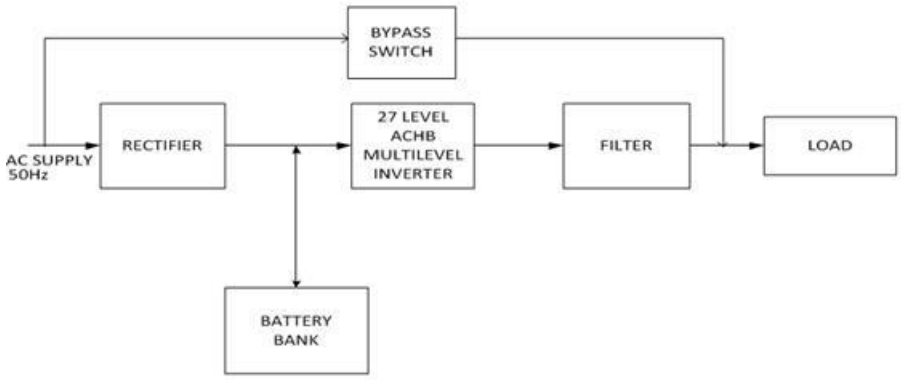

Fig. 2. Block diagram of ACMLI for UPS

The input AC supply is converted into dc with the help of diode bridge rectifier and it is given to ACMLI as input and stored in battery bank also [6]. In ACMLI, the main H bridges and auxiliary H bridges are fed directly by variable DC sources, which are in the ratio of 1:3:9. The output of ACMLI is filtered and given to the load.

2. Asymmetrical Cascaded Multilevel Inverter (ACMLI) for UPS Application

The ACMLI consists of one main H-bridge (MAIN), two auxiliary H-bridges (aux-1, aux-2), and dc input source with different voltage magnitude [7,8]. These dc voltages are in the order of 3x (3VDC, 9VDC and 27VDC). More than 80% of the power is carried by the inverter main bridge with fundamental frequency of 50 Hz. This improves the efficiency by suppressing the switching losses. The auxiliary bridges are responsible for the generation of different levels of voltage with less Total Harmonic Distortion (THD). This asymmetrical configuration can generate 27 level output voltage. The Fig. 3 shows the single phase circuit of 27 level ACMLI.

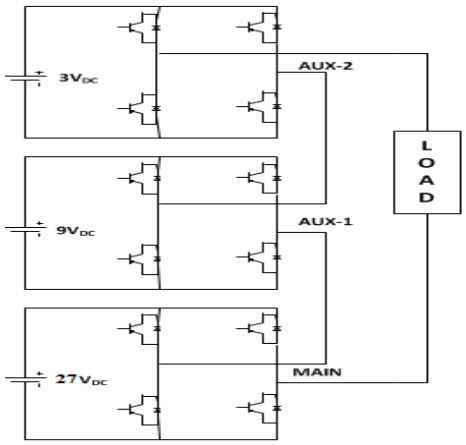

Fig. 3. Single phase circuit diagram of 27 level ACMLI

3. Design specifications of CMLI

CMLI generates the output voltage with less THD, hence it is very popular compared to the conventional two level inverters. In order to generate the more number of levels, CMLI needs more number of dc sources, switches and filters [9].

3.1. The design calculations for single-phase m-level CMLI is explained below.

Number of main switching devices = 2(m-1)
Number of main diodes = 2(m-1)
Number of bridges = (m-1)/2
Number of sources = Number of bridges = Number of DC bus capacitors
Where m = number of levels

3.2. The design calculations for single phase 27 levels CMLI is shown below.

No of main switching devices = 2 (27-1) = 52
No of main diodes = 52
No of bridges = (27-1)/2 =13
No of dc sources = 13
No of DC bus capacitors = 13

To design 27 level CMLI, 52 switches and 13 dc sources are required, which will increase the switching loss and waveform distortion. To provide dv/dt protection, separate snubber circuit is needed for each switch which

will increase the complexity of the circuit and cost. The firing pulses generation for the 52 switches is also complex. Hence the efficiency of the conventional cascaded MLI is reduced [10].

4. Design specifications of ACMLI

The ACMLI consists of one main and two auxiliary H-bridges, three dc sources with different voltages (3VDC, 9VDC and 27VDC). The main bridge is capable to carry more than 80% of power with fundamental frequency. This will reduce the losses and hence efficiency of ACMLI is improved.

4.1. The design calculations for single-phase m-level ACMLI is explained below.

No of levels = 3^{N+1}

Where N= No of Aux bridges.

4.2. The design calculations for single phase 27 levels CMLI is shown below.

No of bridges = 3

No of levels = 3^3 =27

No of switching devices =12

No of dc sources =3

DC voltage sources in the range of 3:9:27

The Table 1 shows the design specification comparison of conventional CMLI and ACMLI

Table 1. Comparison of conventional CMLI and ACMLI

Design Parameters	*Conventional CMLI*	*ACMLI*
No of levels	27	27
No of bridges	13	3
No of switching devices	52	12
No of dc sources	13	3

To produce the 27 level output the ACMLI needs only 12 switches with three DC sources. But by using CMLI, to produce 27 level voltage needs 52 switching devices with 13 DC sources. So the complexity of the circuit and switching losses are reduced by implementing ACMLI when compared to CMLI. The gating signals of the switches are given by using the pulse generator. The switching states are given in Table 2. By using this switching states, the switching pattern for all switches have been obtained. It has many pulses. For each pulse separate pulse generator is used. From this the gating signals for each switch is obtained and given to the switches. Consider in each cell the upper switches are positive and the lower switches are negative. Switching states are negative (-), positive (+) and zero (0) state voltage. The zero voltage occurs in a cell when either both the upper switches or both the lower switches are in ON condition [11].

Table 2. Switching states of Multilevel Inverter for 27 level

Voltage Level	*V1 (3VDC)*	*V2 (9VDC)*	*V3 (27VDC)*
-13VDC	-	-	-
-12VDC	0	-	-
-11VDC	+	-	-
-10VDC	-	0	-
-9VDC	0	0	-
-8VDC	+	0	-
-7VDC	-	+	-
-6VDC	0	+	-
-5VDC	+	+	-
-4VDC	-	-	0
-3VDC	0	-	0
-2VDC	+	-	0
-1VDC	-	0	0
0VDC	0	0	0
+13VDC	+	0	0
+12VDC	-	+	0
+11VDC	0	+	0
+10VDC	+	+	0
+9VDC	-	-	+

+8VDC	0	-	+
+7VDC	+	-	+
+6VDC	-	0	+
+5VDC	0	0	+
+4VDC	+	0	+
+3VDC	-	+	+
+2VDC	0	+	+
+1VDC	+	+	+

5. Simulation Results

The output voltage of the ACMLI depends on dc sources input to the inverter bridges. The output voltage levels can be varied by changing the input dc source voltage. The Fig. 4 shows the main and auxiliary bridge simulation diagram of 27 level ACMLI. This inverter is simulated by using Matlab simulation tool and the Fig. 5 represents the output voltage of 27 level ACMLI using pulse generator without filter.

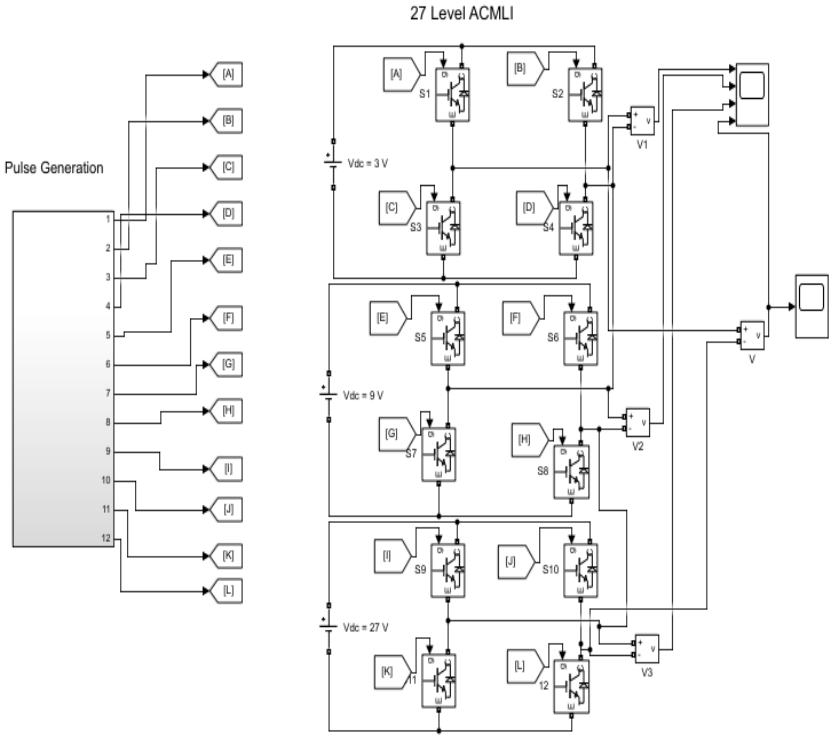

Fig. 4. Simulation model of 27 level ACMLI without filter

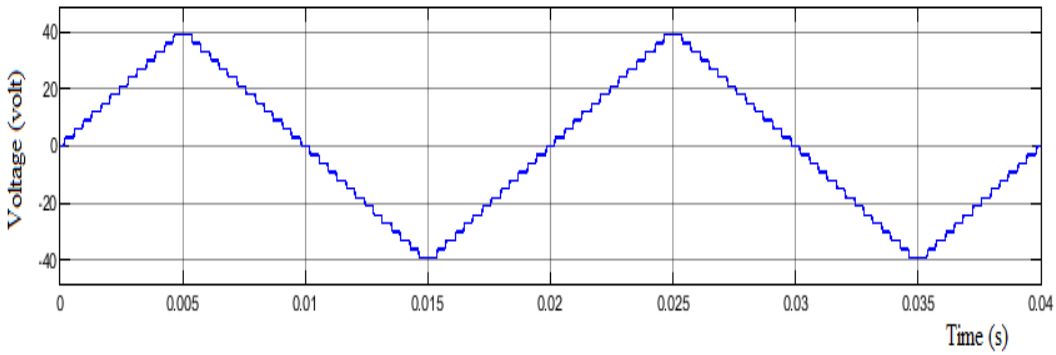

Fig. 5. Simulation output of 27 level ACMLI without filter'

6. Hardware Results and Discussions

The prototype model of 27 level ACMLI is developed to validate the simulation results. DC supply is given as input to the H-bridges of multilevel inverter. The DC supply for 27 level ACMLI should be in the proportion of 1:3:9. MOSFET switch is used in the multilevel inverter H-bridges. PIC controller is used in control circuit to

generate the gate pulses for inverter switches. DC supply is given from power supply circuit to the controller circuit. Opto coupler is used to isolate the controller circuit and power circuit. The prototype model of 27 level ACMLI is shown in Fig. 6.

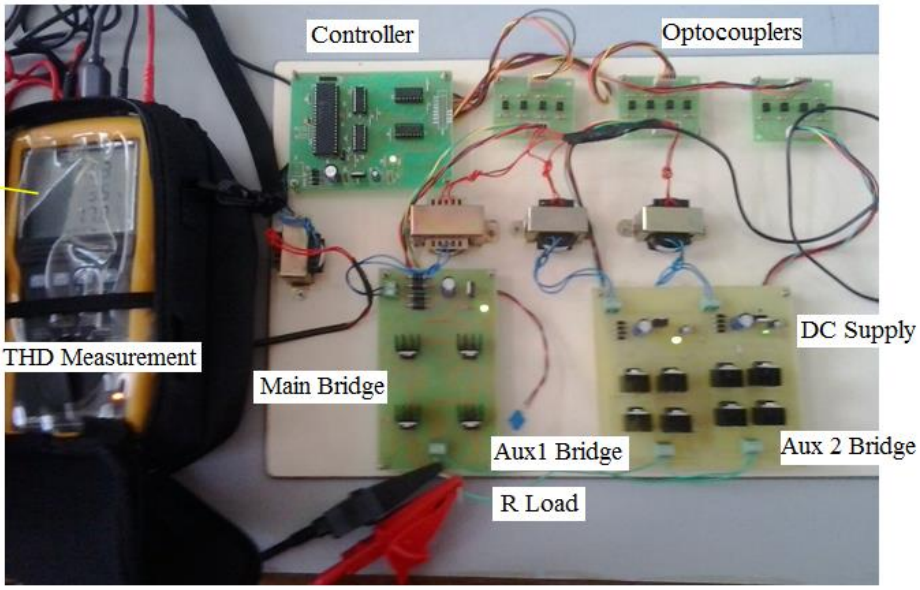

Fig. 6. Prototype model of 27 level ACMLI

The input to the ACMLI is DC, it is in the ratio of 1:3:9. The MAIN bridge is supplied by 27V, Aux-1 bridge is given 9V and Aux-2 bridge is given 3V are shown in Fig. 7.

The pulses are generated by PIC16F887 microcontroller. The controller produces output voltage of 5V. The controller output pulses are produced by using timer of the microcontroller. The output pulses generated for the MAIN bridge switches, Aux-1 bridge switches and Aux-2 bridge switches are shown in Fig. 8, 9 and 10.

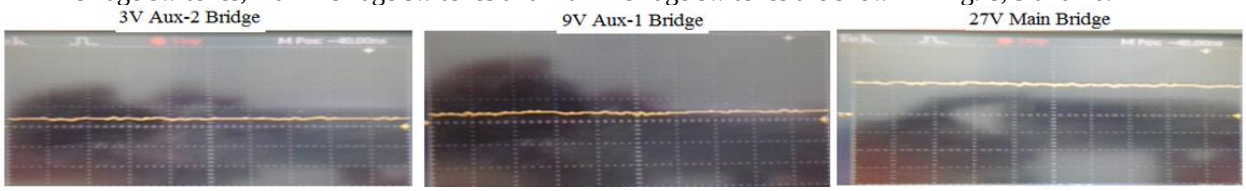

Fig. 7. Input DC sources to Aux-2 bridge, Aux-1 bridge, MAIN bridge.

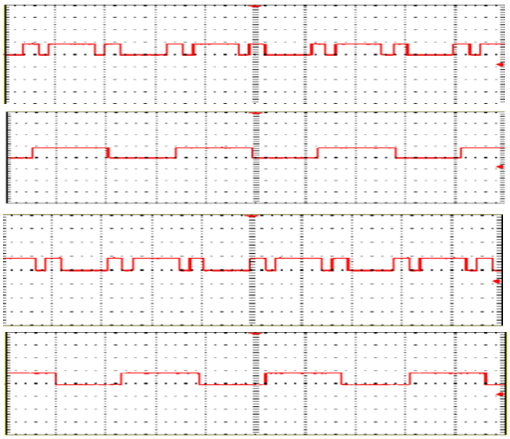

Fig. 8. Output pulses for the MAIN bridge switches

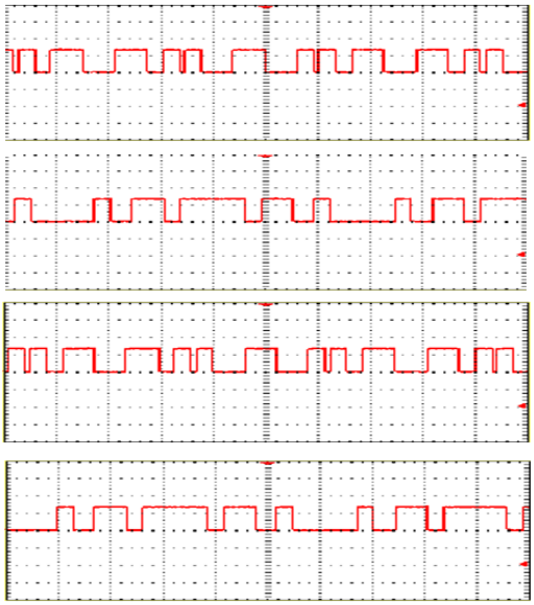

Fig. 9. Output pulses for the Aux-1 bridge switches

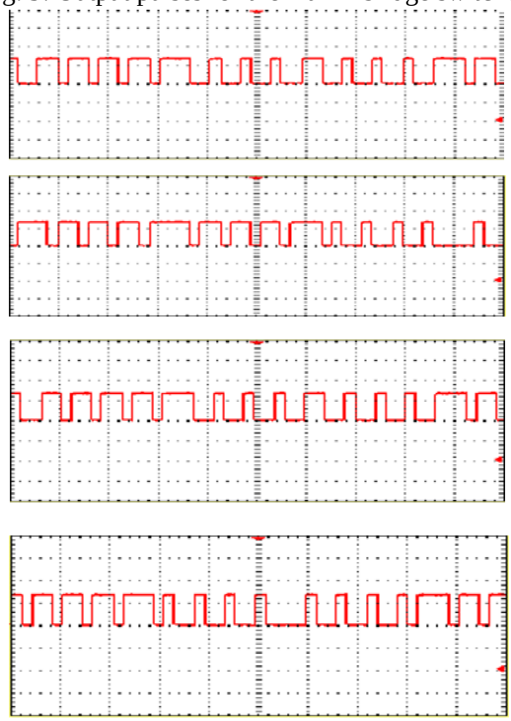

Fig. 10. Output pulses for the Aux-2 bridge switches

The output voltage of ACMLI depends on the input voltage applied to the main, aux-1 and aux-2 inverter bridges. 10KΩ resistor is connected as load across the H-bridges. The hardware output voltage of Aux-1 bridge, Aux-2 bridge and MAIN bridge are shown in Fig. 11, 12 and 13. The Fig. 14 shows the output voltage of hardware model of 27 level ACMLI. From the Figure 14, it is evident that the hardware results are similar to the simulation results and validates the simulation results. Fig. 15, depicts the output voltage (Total Harmonic Distortion) THD of the 27 level ACMLI. The THD value is 4.23%, by using filter it can be reduced and pure sinusoidal waveform can be obtained.

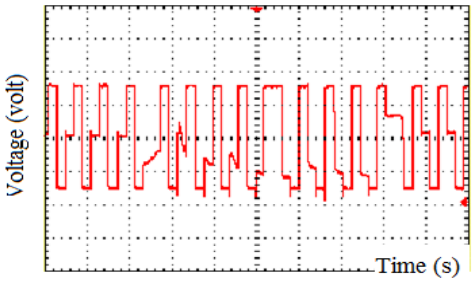

Fig. 11. Hardware output voltage of Aux-2 bridge

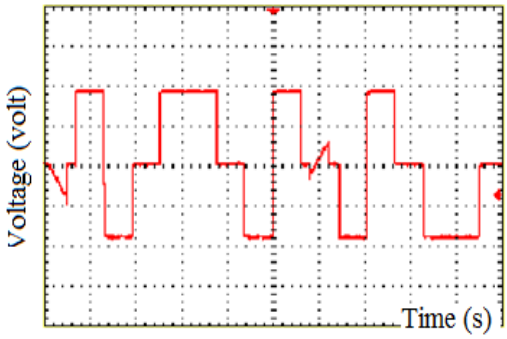

Fig. 12. Hardware output voltage of Aux-1 bridge

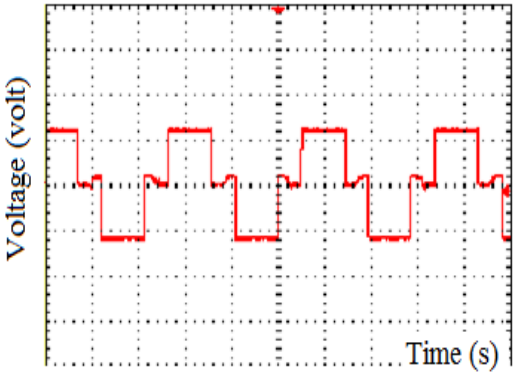

Fig. 13. Hardware output voltage of MAIN bridge

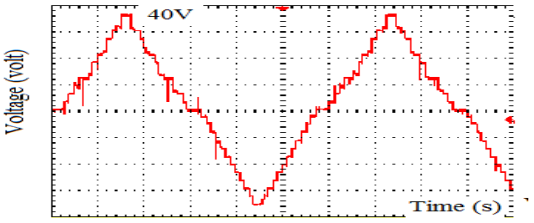

Fig. 14. Hardware output voltage of 27 level ACMLI

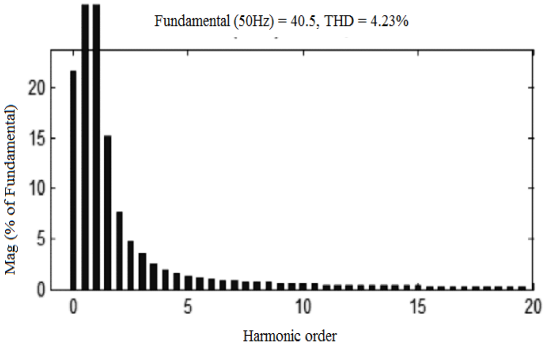

Fig. 15. Output voltage THD of 27 level ACMLI

7. Conclusion

The simulation and hardware results of 27 level ACMLI is presented. This ACMLI requires less number of power switches when compared to conventional CMLI. To obtain 27 level output voltage, the ACMLI requires only 3 H-bridges, 12 switches, and 3 dc sources; whereas CMLI requires 13 H-bridges, 52 switches, and 13 dc sources. Hence the switching losses in the ACMLI are less, cost of the ACMLI is less and efficiency of the system is increased. The THD percentage is 4.23%, which improves the power quality of the system. The simulation results are validated with the hardware results. This ACMLI can be used for UPS application in order to get pure and proper sinusoidal AC output voltage.

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