A New Speed Power Area and Accuracy (SPAA) Aware Cordic Processing Unit By VedicMathematics For The Application of Computer Vision

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Abstract—we are living in the era of fast processing applications like 3D, 5G, 9D. These types of application need a processing unit which have separate arithmetic unit & separate trigonometric unit which is well known as CORDIC processing unit. As we know Graphics processing unit is the brain of any graphics systems now a days there is Gaming specific systems are available which require ultra-high-speed GPU on those GPU there is separate trigonometric calculation processing unit is there which is called CORDIC. So, in this paper basically we proposed a novel architecture of CORDIC unit which is able to give the output in very less time. In this paper we also try to do the justice with the speed power area and accuracy Metrix.

Keywords— GPU, 3D, 5G, 9D, HD, ALU, SPAA

1. Introduction

Vedic Mathematic create a great support system for the fast calculation, by using of Vedic Mathematics we are able to get result in very few sec. As we know this is the era of high-speed internet, 4D graphics video, and 5G network. Now if you are talking about fast speed so there is need of fast calculation regarding that calculation, we can use Vedic mathematics.2020 is the period of high class clinical, aviation, robotization, and media innovation. According to these sort innovation there is necessity of acceptable nature of calculation which can do quick handling in exceptionally less time. As we probably am aware for sight and sound application now a days PC vision is assumed each significant part according to the PC vision, essentially it's a virtual vision framework which is show the fanciful substance in to this present reality. For these sort of high illustrations based PC vision there must be a need of extraordinary quality level based quick handling calculation which can make a quick preparing programming for those sort PC vision application. As we probably am aware every one of these calculations are dealing with preparing unit and according to the handling unit there is must be an Arithmetic unit is there which can do all sort of numerical figuring, presently the inquiry is just ALU unit is adequate to do quick handling for these sort of utilization and the appropriate response is no. According to the count of those sort of use need a Graphics handling unit where GPU have all unique kind of figuring measure. Presently CORDIC processor is one of the main calculations which are used in GPU for the count of mathematical capacities. In this paper we proposed a novel CORDIC processor which depends on estimate rationale, aside from that in this paper we did the correct similar examination on existing CORDIC calculation and Proposed CORDIC processor. According to the our relative examination on calculation level we utilize Discrete Cosine Transform based picture pressure calculation and play out the quality level investigation as far as picture quality boundaries .

The rest of the paper is sub arranged as follows. Important foundation and fundamental guideline of CORDIC Algorithm is given in Section II while Section III presents the Proposed CORDIC processor. Section IV presents the result analysis & comparative analysis Section V is end which wraps up the whole paper.

2. Literature Review

VLSI technology is a chip processing technology through VLSI now a days most of the applications are based on hardware. Where processing units are the most important part any application. In present era through VLSI there is possibility to create an application specific processing unit which is known as ASPU. Now if we are talking about any of the processing unit so the most important and common factor is its calculation unit which is known as ALU. Now a day's most of the applications have application specific arithmetic unit which is only design for that application only. Similar approximation logic is the one of the most important logic through this approach we are able to get application specific arithmetic unit. Now as we know Vedic mathematics is the one of the greatest and fast calculation mathematical approach. Using Vedic mathematics, we are able to get the value of any calculation logic in fraction of time. So now a days in VLSI Vedic mathematics play a great and

most important role. If we are talking about the CORDIC so CORDIC is kind of application specific processing unit which is mostly design for high end graphics processing units as there are two type of arithmetic calculation, where first is simple arithmetic logic which require addition subtraction , multiplication & division. Apart from that another type of mathematical logic is trigonometric so now a day there is specifically another processing unit is using which is known as cordic processing unit. Now the history of CORDIC is started in 1959 [10]. As per this approach there is loads of extra calculation is require for the calculation of cosine & sine. In [18], [19], [20] they makes use of the Taylor method and the usage of that logic they calculate the COSINE & SINE value however the problem with this strategy is too lots time consumption due to the variety of new release process. Now after that scaling free cording is proposed by way of [23] the place they are the usage of a method which is now not the usage of scale however once more it's an generation process. Supriya [24] in accordance to this paper creator recommend an strategy which is terrific in time & area. Supriya 2012[26]: This paper suggests a mechanical get mutually amazing game-plan for making backward of cosecant and secant waves task to the CORDIC (Coordinate Rotation Digital Computer) tally. In this outstanding shape the cordic experiences quintessential downsides like scale-factor figuring, slowness and satisfactory affirmation of little diploma turns. The requested figuring beats these weights. We make use of the use of one piece disclosure system to see the little increase turns. The scale free technique of the requested estimation relies upon upon on Taylor manner enhancement of the sine and cosine waves. Supriya 2013[27] this paper indicates a novel definitely sans scaling CORDIC figuring in upward shove up mode for hyperbolic heading. They use most-immense 1 piece ID strategy for limit as soon as extra scale flip enchancment age to scale once more the share of cycles. These are previous investigates which are recognized with the CORDIC figuring. As per the preceding present technological know-how there is loads of enchancment is require right here we additionally see there is plenty of complexity in CORDIC processing unit. Many authors strengthen imprecise however simplified arithmetic units, which grant an more layer of strength financial savings over conventional low-power plan techniques. This is attributed to the decreased good judgment complexity of the proposed approximate arithmetic units. Note that the approximate arithmetic units no longer solely have decreased wide variety of transistors, however care is taken to make certain that the interior node capacitances are a good deal reduced. Due to the barriers in this techniques and the accuracy degree necessities nevertheless the complexity can be decreased and the SPAA (Speed Power, Area, Accuracy,) metrics can be nonetheless performed efficiently. So to enhance SPAA metrics we want a novel arithmetic unit with low power, excessive speed, with extended density and PVC conscious circuits.

3. Methodology & Implementation

CORDIC algorithm is most powerful algorithm which used in GPU, due to that algorithm now a days we are able to get the great experiences on video & image processing system. As per the classic CORDIC algorithm they use the vector,Va[Xa, Yb] be derived via rotating the vector Vb[Xa, Yb] through an angle, then:

$$\begin{bmatrix} Xb \\ Yb \end{bmatrix} = Rp.\begin{bmatrix} Xa \\ Ya \end{bmatrix}, Rp = \begin{bmatrix} Cos\Theta & -Sin\Theta \\ Sin\Theta & Cos\Theta \end{bmatrix} \quad (1)$$

Here equation (1) shapes the fundamental rule for iterative arrange calculation in CORDIC algorithm [1].

$$\Theta = \sum_{I=0}^{B} \text{ui} * \text{ai} \qquad (2)$$

$$\text{Here ui} = -1,1; \text{ai} = \tan^{-1} 2^{-i}$$

As we can see in equation (3), the scale issue Ki is free and no longer dependent of the direction of micro-rotation

$$Rp = Ki.\begin{bmatrix} 1 & -ui.2^{-i}\Theta \\ ui.2^{-i} & Cos\Theta 1 \end{bmatrix} \quad (3)$$

Proposed Processing Unit:

As per our proposed algorithm we basically follow the mathematical formula for the calculation of Sine & Cosine value, we perform the followings steps:

1. Angel Difference
2. Use of Vedic Multiplier
3. Modified Radian K1 (For Sin 0-45)

4. Modified Radian K2 (For Sin 46-90)

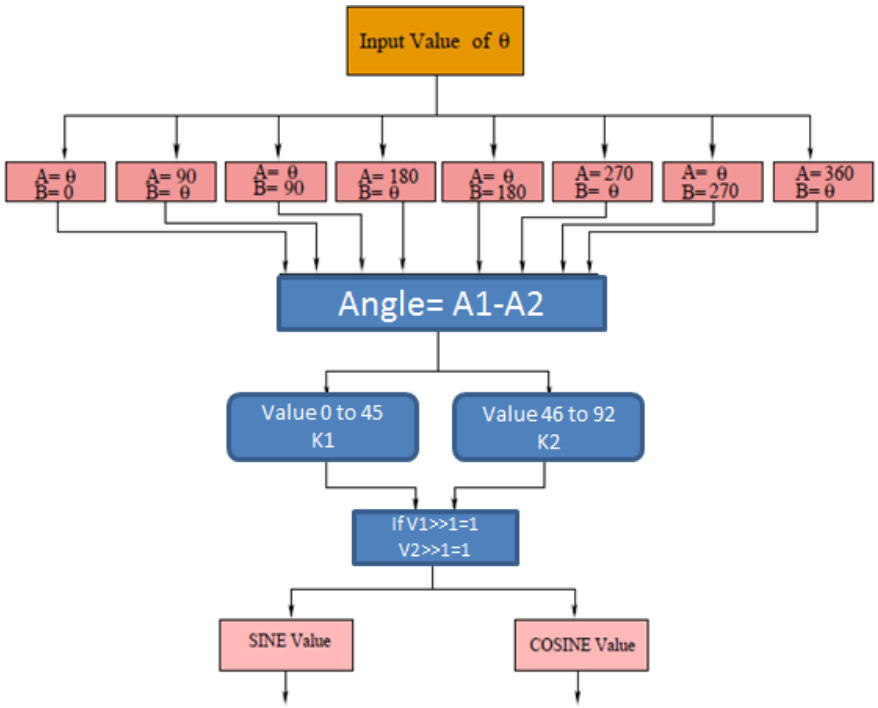

Fig.3.1 Proposed Design Flow

Using this way we calculate the value of sine & Cosine, as per this proposed algorithm we are able to get output, now for multiplication point of view use the approximate Vedic multiplier.

Approximate Vedic Multiplier: As per this multiplier use the concept of Urdhvatiryakbhyam, as per this design 4 BIT Accurate Urdhava multiplier, 4 Bit Semi Approximate Urdhava Multiplier and at last we design 4 Bit pure approximate Urdhava multiplier. According to Pure approximate multiplier our initial 4 bit is generated by the combination of 1,0. For Semi approximate our initial two is generated by 1,0 combination.

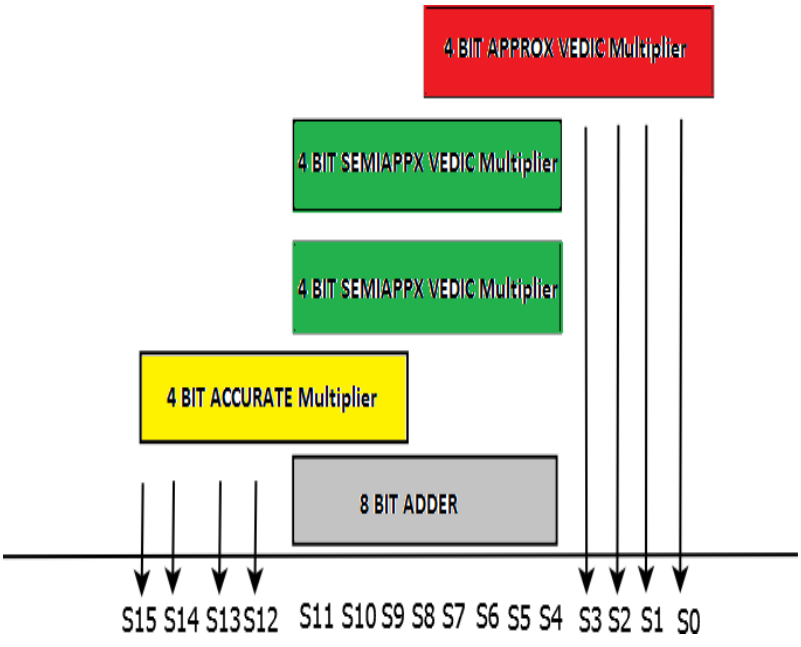

Fig. 3.2 8 Bit Approximate Multiplier

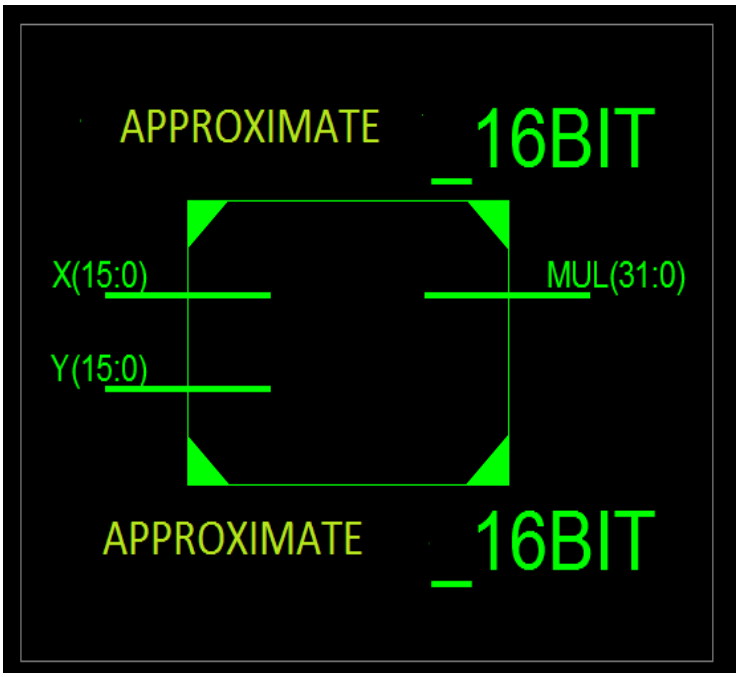

Figure 3.3 Schematic of Approximate Multiplier

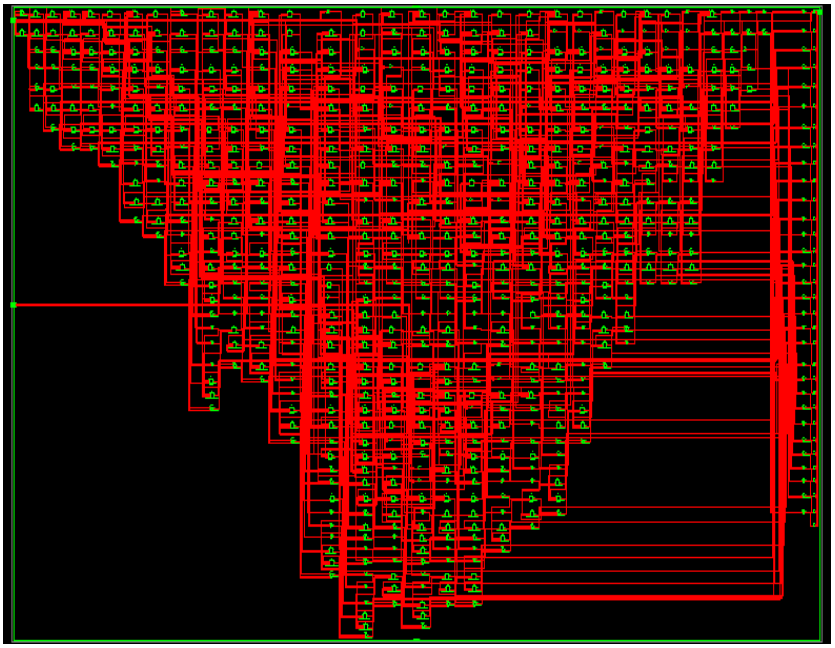

Figure 3.4LUT of Approximate Multiplier

So here we proposed a novel architecture for calculation of sine & cosine trigonometric functions.

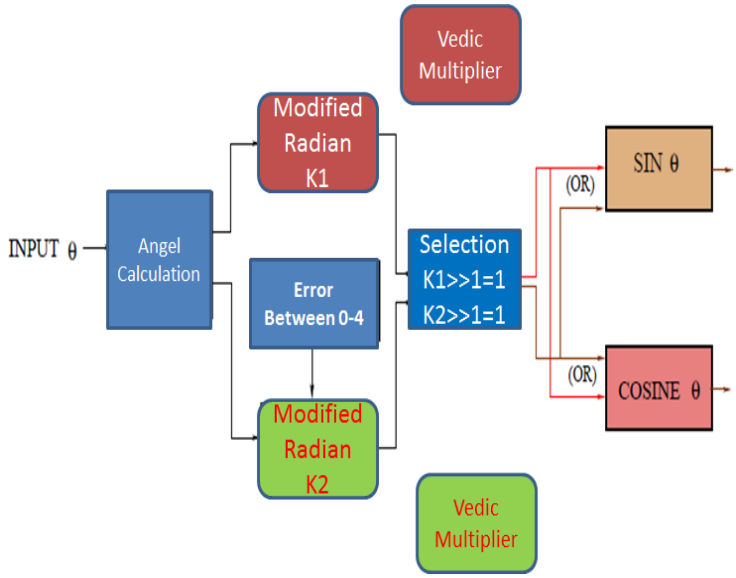

Fig.3.5 Proposed Architecture

As we can see on fig. 3.5 its shows that out proposed architecture id follows the three steps which are:

1. **Angel Calculation**
2. **Use of Vedic Multiplier**
3. **Calculation of K1 & K2**

So as per the first step we calculate angel value by using of angel rotation concept. Once angel calculate than we calculate the K1 & K2 value by using of radian calculation where we apply the approximation logic & approximate Vedic Multiplier.

4. Result & Analysis

In this section we are doing the comparative analysis based on different kind of parameters.

In this part we introduce the relative investigation of all with previous existing methodology. For analysis factor of view we use these parameters:

1. Power
2. Speed
3. Hardware (LUT)

Here we use FPGA technology:

1. Spartan 3
2. Spartan 6
3. Spartan 7
4. FSIM

Table 4.1 Error Analysis

Θ	CORDIC	Scaling Free	Efficient CORDIC	Taylor Based	Proposed
0-90	0	0-0.008	0-0.009	0-0.01	00-0.007
90-180	0	0-0.006	0-0.008	0-0.008	0-0.007
180-270	0	0-0.036	0-0.00256	0-0.009	0-7
270-360	0	0-0.096	0-0.002369	0-0.008	0-0.007

Comparative Multiplier Analysis:

Approximate Multiplier Accuracy Level is 85-90%. The FPGA comparison analysis of approximate and accurate are shown below, here hardware analysis is done on Vertex 6 FPA which is 45nm based technology.

As per the correlation table obviously approximate multiplier in more productive to utilize in light of the fact that it has less deferral as contrast with other multiplier. Less postpone that implies when rough multiplier has utilize then processor result will be get in a couple of Nano/Pico seconds. This multiplier likewise have less LUT Logic implies this is a less cost multiplier and the recurrence Column of the table is demonstrating that it recurrence are Very high as contrast with other multiplier.

Comparative Proposed Vedic CORDIC Processing Unit:

Table 4.2 Reasonable Time Analysis

FPGA TYPE	Taylor Based	Efficient CORDIC	Scaling Free	Proposed
Spartan 3	140.52us	120.33us	135.63us	110.25us
Spartan 6	97.25us	77.67us	80.32us	68.62us
Spartan 7	65.42us	54.56us	58.86us	52.56us

Table 4.3 Reasonable Multiplier Analysis

S.NO.	Multiplier Name	LUT	Delay	Frequency
1	Add_Shift	591	7.29	137.17
2	Wallace Tree	504	10.591	94.41
3	Urdhav	441	7.299	137
4	BWSM	413	9.102	109.86
5	BOOTH	536	7.536	132.69
6	Approximate	364	6.998	142.89

Table 4.4Reasonable Power Analysis

FPGA TYPE	Taylor Based	Efficient CORDIC	Scaling Free	Proposed
Spartan 3	1.823mw	1.325mw	1.51 mw	1.35mw
Spartan 6	1.057mw	0.826 mw	0.946 mw	0.722mw
Spartan 7	0.699mw	0.502mw	0.560mw	0.185mw

Table 4.5 Comparative LUT Analysis

FPGA TYPE	Taylor Based	Efficient CORDI	Scaling Free	Proposed
Spartan 3	247	197	207	178
Spartan 6	127	93	106	87
Spartan 7	85	62	73	58

In terms of architecture level analysis our proposed approach is far better than with others.

Comparative Analysis:

Using the sin and cosine I have analyzed the error difference between the sin wave and cosine individually and Trigonometric Identities $\sin^2(x) + \cos^2(x) = 1$ after analyzing the results in conventional approach, the results:

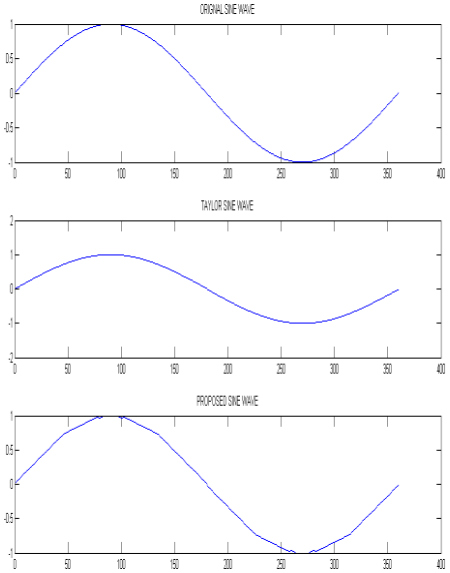

Figure 4.1 Sine Wave

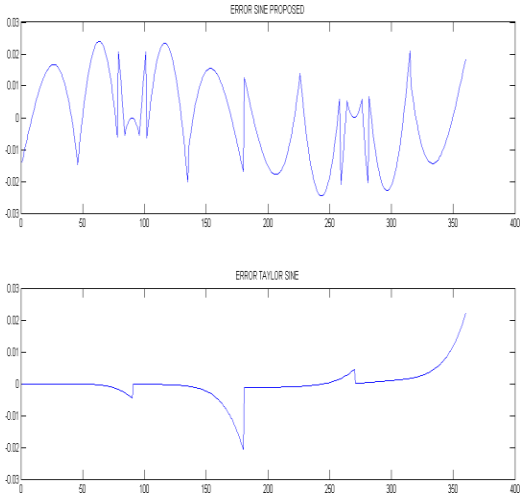

Figure 4.2 Error In Sine Wave

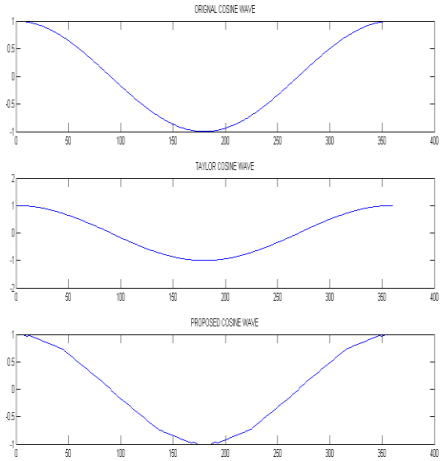

Fig. 4.3 Cosine Wave

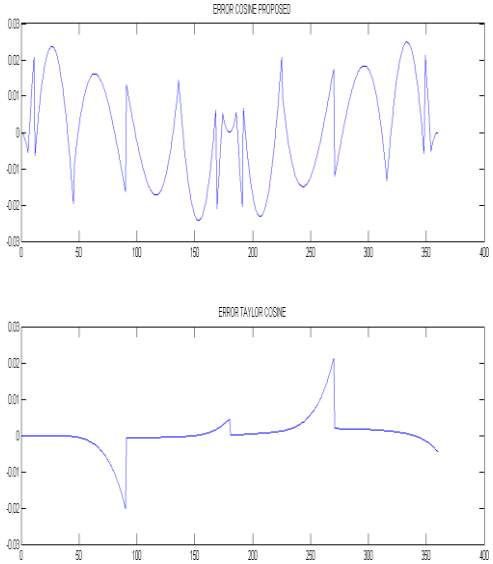

Figure 4.4 Error in Cosine Wave

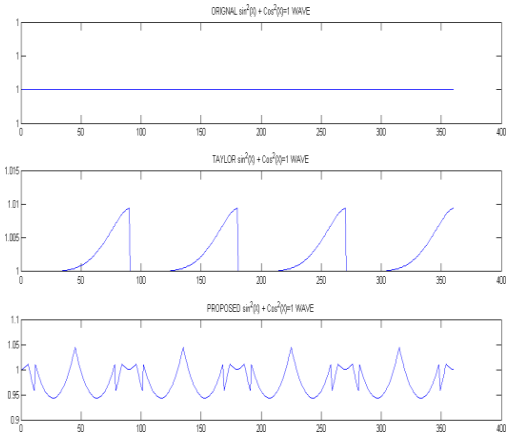

Figure 4.5Trigonometric Identities

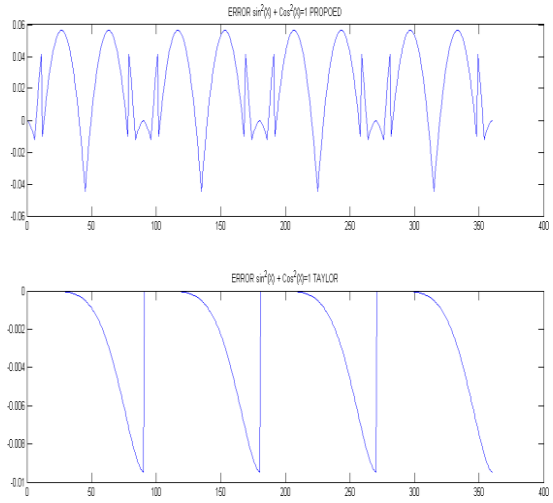

Figure 4.6 Trigonometric Identities Error

5. Conclusion

CORDIC is an effective algorithm, and a famous algorithm of preference when it comes to a number Digital Signal Processing applications. Implementation of a CORDIC-based processor on FPGA gives us a effective mechanism of imposing complicated computations on a platform that affords a lot of assets and flexibility at a rather lesser cost. Further, given that the algorithm is easy and environment friendly the graph and VLSI implementation of a CORDIC primarily based processor is without problems achievable. According to cutting-edge development future is definitely hooked up on digital world. Right now every lessens depends upon on-line like shopping, films, pictures, instructions assessed time of appearance. So for these type of use there is want of some different stable gadget which are recognized as communitarian structure, arranging, Internet of things, etc. As we probable am conscious cordic dealing with unit is essentially produce from the cordic calculation, it implies if cordic calculation is fine as some distance as calculation boundaries with the purpose that strategy will be desirable as a long way as the engineering level. Here we use the VLSI science to construct a CORDIC processing uni , on that evaluation we create processing unit on more than one FPGA like Virtex 4, Virtex 6 & Virtex 7 and primarily based on the comparative evaluation we discovered our proposed structure I a ways higher than in phrases of velocity strength & area. Our proposed machine proper makes a justice with the SPAA matrix. As per propped strategy we are in a position to get the enhancement of 20-25%.

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