Implementation in Direct Digital Synthesizers (DDS) Based on CORDIC Algorithm

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Abstract: The universality of computerized signal handling (DSP) has made expanding request to create territory effective and precise structures in completing numerous nonlinear math tasks. One such design is CORDIC unit which has numerous applications in the field of DSP including actualizing changes dependent on Fourier premise. This paper offers structure of CORDIC, inserted with a pipelined unit that has exclusively negligible scope of adders and shifters. It tends to be applied in pivot mode as appropriately as vectoring mode. The reason for the arrangement is to get a pipelined CORDIC unit keeping up the format of valid calculation. Preparing and discussion structures work CORDIC in round organize contraption and in both of pivot or vectoring modes.

Keywords: Trigonometry, CORDIC, FPGA, DCT, Fourier Transform

1. Introduction

Organize Rotation Digital Computer (CORDIC), an unmistakable explanation PC to process numerous non-straight and supernatural capacities, used to be proposed by utilizing Volder in 1959 [9]. The highlights that can be registered the utilization of a CORDIC PC comprise of trigonometric, logarithmic, exponential, hyperbolic, duplication, division, rectangular root, and so forth [10]. Despite the fact that it toward the beginning served the explanation of route frameworks, it later developed to be a well-known gadget to place into impact many computerized structures specifically in the zones of advanced sign handling, correspondences, PC designs, and so forth [20]. The effortlessness of CORDIC is that it can figure any of the above alluded to highlights the utilization of movements and increments which are of the structure the working mode and the arrange gadget picked are two key components to register the supported highlights in the CORDIC. Many sign handling and discussion structures work CORDIC in round organize device and in both of revolution or vectoring modes.

2. Literature Review

An embedded system is a hardware computer system that is dedicated to specific functions to serve in a larger mechanical or electrical system when response time is the primary concern. Embedded systems are very general purpose systems due to its qualities like low power consumption and economical low cost. The micro-controller and DSP, embedded systems has the disadvantage of instruction execution, it executes the instruction sequentially [27],[28]. The sequential execution starts which fetches the instruction appended by decoding an execution. After fetching it starts fetching the next code while decoding the previous code. So it is inherently a sequential system that will take more clock cycle to execute an algorithm. So our primary goal is to develop a hardware that executes an algorithm with less number of clock cycles. This facility is available in FPGA platform. A field-programmable gate array (FPGA) is an integrated circuit designed which can be arranged by a client or a designer subsequent to assembling, consequently "field-programmable", which is the most favorable advantage of FPGA over micro-controller. We can have the processes done according to the written HDL code "in parallel" which means simultaneously. The ability of FPGA parallel processing is one of the most important features that separate FPGA from theprocessors and made it superior in many areas. This facility is adopted in our work.The image processing techniques are validated using some high-level languages that will increase the bugged, and the algorithms are also sequential. Embedded micro-controller can be a better choice for design and economic cost system. From the above discussion, we have concluded that, for real-time operation the embedded system like micro-controller and DSP, not a right choice for real-time image processing system [20][24]. FPGA platform is giving a better advantage to implementing the sequential image processing algorithms in the parallel platform. The FPGA hardware works as shown below. In FPGA, the processes are concurrent means the produces output simultaneously. So the algorithms can process in parallel. Due to this advantage in FPGA we chose FPGA as the hardware platform.

It seen from sampling theorem, that the representation of the sparse signal in some basis of the dictionary is possible with less number of coefficients. DCT is a commonly used sparse representation

dictionary for image signal in the frequency domain. So, it can help to reduce the memory allocation for storing the signal for further use as in JPEG. Also, it reduces the bandwidth of channel. So it will be very convenient that if we can find the information about the image in DCT domain, then we can analyze that this image is acceptable for display or not. DCTis a unitary transform, and it obey the Parseval theorem. Using this property and SSIM spatial equation, the relation between spatial components in terms of DCT coefficients can be found out. To speed up the operation, it is required to do some parallel architecture to find SSIM in DCT domain. So the assessment of distortion of the image in DCT domain is possible. So we can calculate the SSIM in DCT domain.

The rotation of a two dimensional vector with an angle θ, to obtain a final rotatedvector. Here the initial vector and rotated final vector are $P_0 = [x_0,y_0]$ and $P_n = [x_n,y_n]$

$P_n = RP_0P_n = P'_n\ Cos\theta$

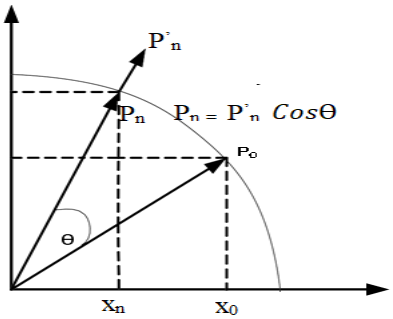

Fig.1 Graphical Representation of CORDIC

Where R is given as

$$R = \begin{bmatrix} Cos\theta & -Sin\theta \\ Sin\theta & Cos\theta \end{bmatrix} \qquad (1)$$

Also write as

$$R = [1 + \tan^2\theta]X \begin{bmatrix} 1 & -tan\theta \\ 1 & tan\theta \end{bmatrix} \qquad (2)$$

$$R = K_pR_p$$

Where

$$K_p = [1 + \tan^2\theta]$$

$$R_p = \begin{bmatrix} 1 & -tan\theta \\ 1 & tan\theta \end{bmatrix}$$

3. Procedure and Operation

3.1 Calculation of Cosine and Sine Function using CORDIC Algorithm

$$\lim_{n\to\infty} \begin{pmatrix} x_n \\ y_n \\ z_n \end{pmatrix} = KX \begin{pmatrix} x_n Cosz_n - y_n Sin\ z_n \\ y_n Sin\ z_n + x_n Cos\ z_n \\ 0 \end{pmatrix}$$

So, if we put some specific values in above equation sine and cosine function. The final output as sine and cosine function is calculated below. Where $x_0 = K$, $y_0 = 0$ and $x_0 = \theta$ is taken.

$$\lim_{n\to\infty} \begin{pmatrix} x_n \\ y_n \\ z_n \end{pmatrix} = \begin{pmatrix} Cosz_n \\ Sin\ z_n \\ 0 \end{pmatrix}$$

Calculation of cosine and sine function has been validated with MATLAB. From the above simulation, it concludes that using this algorithm a core can be developed to calculate cosine and sine function. In this work,

we are considering only the cosine function so we developed core that will produce only cosine output for a particular input. So the cosine core is designed.

3.1 Proposed Methodology

As referenced before, the proposed plan of DDS depends on pipelined CORDIC, which goes about as stage to sufficiency converter. The stage aggregator has an exactness of bits, which compares to that of the information, which is recurrence control word. The yield of stage gatherer is given as contribution to planned CORDIC square, which has a planning component that maps the pipelined CORDIC over the whole 2π territory. The planning instrument works by considering the three hugest bits of the sources of info. That is, contingent upon the estimations of the three MSBs, the points are referenced in one of the eight octants. Figure 2 shows the stage collector schematic of proposed plan.

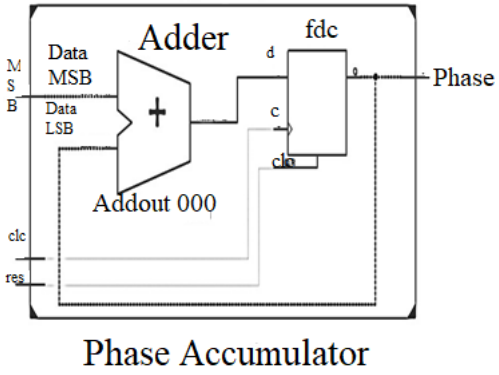

Fig.2 Proposed Phase Accumulator

The moving in moderate stages in the proposed structure is made designed, along these lines improving inactivity and lessening the deferral of the plan. The check yield of the top module guarantees the right addition of the aggregation step. In the proposed plan, the sufficiency is spoken to utilizing input bits. In this way, the absolute number of plenty fullness quantization levels since the most noteworthy piece speaks to the indication of the abundancy. There are two yields of the proposed structure relating to the quadrature yields of sine and cosine. Consequently, the proposed structure creates quadrature yields utilizing single design. All in all, the data sources and yields of the proposed plan are recurrence control word for setting the yield recurrence, clock for setting testing recurrence, quadrature waves and check signal for checking aggregation file.

5. Conclusion

With standing that, the proposed plan produces quadrature yields which have better stage coordinate subsequently making the structure more valuable for the vast majority of the correspondence frameworks. The straightforward structure of DDS dependent on CORDIC consistently is a superior decision since actualizing this in circuits, for example, blenders, advanced down/up converters is less complex as far as equipment use. The higher the stage collector information width, the lesser is the stage quantization blunder. Henceforth, abundance exactness of the yield waveforms is improved. The most extreme recurrence of activity is 155.751 MHz. The cut postpone result of the proposed plan is 2.45. The complete force utilization of the proposed structure at the most extreme recurrence of activity is 638.61mW.

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