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Research Article

Performance Analysis of Adiabatic Vedic Multipliers

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Abstract: Energy dissipation and reliability are the two important design constraints in the high performance processor design. With the advancements in the IC manufacturing and reduced feature sizes the energy dissipation increases in exponential manner at the lower technology nodes. So, there is a need to design energy-efficient and reliable circuits and systems. The reliability with temperature is also one of the major challenges in today's smart systems as they are operated in harsh environments. Most of the works till date analyzed the reliability with respect to DC constraints. The basic operation in the high performance Digital Signal Processing (DSP) is the multiplication is used to simplify various operations like convolution, filtering and correlation. In this work, a Vedic multiplier with 4x4 size is implemented with FinFET based energy recovery Modified PFAL (MPFAL) logic at 45 nm technology node. The designed multiplier performance is analyzed and compared with our earlier work in terms of energy dissipation and delay. The results indicate a reduction of 55% in energy dissipation over ECRL based Vedic multiplier. Linear variation of power dissipation with temperature in the order of pW shows that design MPFAL Vedic muliplier is more reliable compared to CMOS multiplier.

Keywords: Vedic Multiplier, MPFAL, FinFET, Energy Dissipation, Reliability.

1. Introduction

In the fields of image processing and DSP multipliers plays a crucial role. The fundamental algorithm like FFT requires more number of addition and multiplication operations. As the adder is one of the basic building blocks in the multiplier architecture, it is mandatory to optimize the adder while implementing multiplier. Several high speed multiplier architectures are available in literature. Among which a multiplier circuit makes use of vedic principles is found to be a faster one. The literature survey shows that these multipliers are found to operate at high speeds with reduced power dissipation as compared to Baugh-Wooley multiplier [1].

The main reason for significant increase in dynamic power in arithmetic circuits is due to its faster switching [2]. Several researchers proposed different low power design techniques at various levels of VLSI design abstractions [3-6]. The most attractive design technique at the circuit level is energy recovery logic [7-8] which make use of thermodynamic principle. In theoretical means, zero consumption of power can be attained using energy recovery principle with a constant current source as a power supply.

The continuous reduction in device size leads to exponential increase in the leakage power due to Short Channel Effects. At the device level several alternative structures like CNTFET [9], FinFET and TFET [10] are proposed in place of conventional MOSFET. The use of FinFET as an alternative to CMOS further improves the energy recovery of the adiabatic logic. The performance comparison of different adiabatic circuits based on FinFET is analyzed with a Brent-Kung Adder as a test module[11].

A 4x4 vedic multiplier is implemented with FinFET based MPFAL logic using Brent-Kung Adder (BKA) is presented in this paper. In our earlier work Vedic multiplier is implemented with FinFET based ECRL logic using (RCA) [12]. The design metrics are analyzed by performing simulations with BSIM-CMG FinFET model at 45nm technology node, in 1-1000MHz frequency range and compared with existing works.

The remaining part of the work is structured in the following manner. The background of energy recover, Modified Positive Feedback Adiabatic Logic, and dual gate FET (FinFET), are given in section II. 4-bit Vedic multiplier design is discussed in section III. Section IV gives the performance of the design. Finally section V concludes the paper.

2. Background

A. Adiabatic Logic

The major source of energy dissipation in conventional CMOS circuits is the dynamic power due to node switching activity. One of the prominent alternatives to reduce this energy dissipation is the adiabatic charging [13]. In these circuits the energy loss is reduced by recycling and reuse of energy and are operated with a variable voltage source. The over view of an adiabatic gate is given in Figure 1. In these circuits in order to store the data without erasing latch structure is required and is implemented with cross coupled connection of PMOS transistors or back to back connection of inverters.

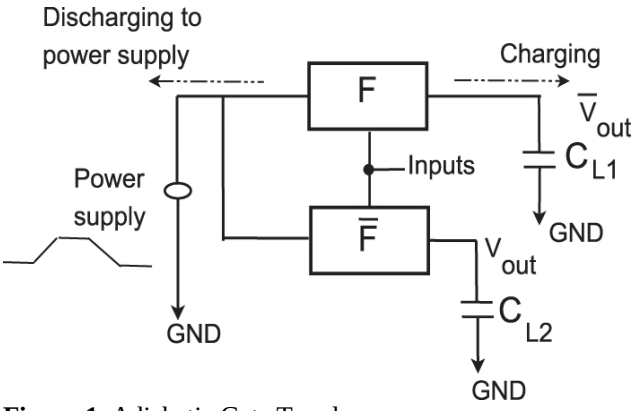

Figure 1. Adiabatic Gate Topology

In the literature, different adiabatic logic structures with single and dual-rail nature have been reported. The logic families like Efficient Charge Recovery Logic (ECRL), Positive Feedback Adiabatic Logic (PFAL) are the basic dual-rail logic families. The reliability characteristics with respect to temperature play a important role in high performance computing devices. Due to increase in power dissipation, temperature on chip increases and it will degrade the performance as well as reliability. Till date most of the reliability works with temperature are concentrated on DC parameters only. Hence there is a need to analyse this when the circuit is working [14]. So, in this work the variation of power dissipation with temperature range of 0 to 100ºC are analysed at a power clock frequency of 10MHz. During last few years many arithmetic modules are implemented using several energy recovery adiabatic families and their performance is evaluated. Even though, the previous works shown ECRL and PFAL energy dissipation is less compared to other families there exists a non-adiabatic power loss of ½ CV_{th}^2 [15] shown in figure 2.

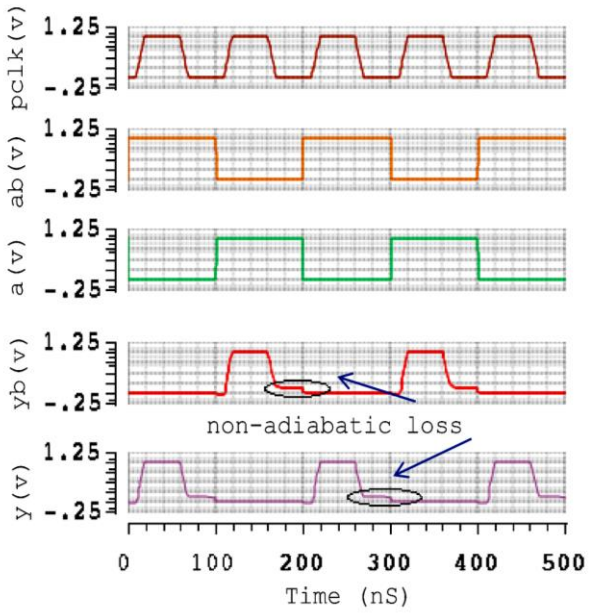

Figure 2. Output of PFAL Inverter/Buffer with ½ CV_{th}^2 Loss [15]

B. Modified Positive Feedback Adiabatic Logic (MPFAL)[15]

This logic family is derived from the PFAL Adiabatic Logic and is presented in figure 3 operated with trapezoidal power clock. The latch structure to hold the state is formed by two CMOS inverters connected in back to back fashion and is operated with complementary power clocks. Figure 4 depicts the timing diagram of MPFAL inverter/buffer.

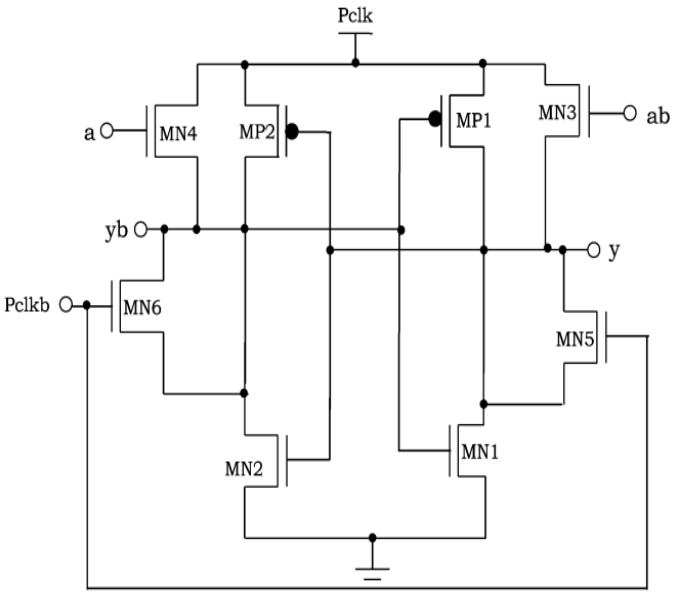

Figure 3. Topology of Modified PFAL gate.

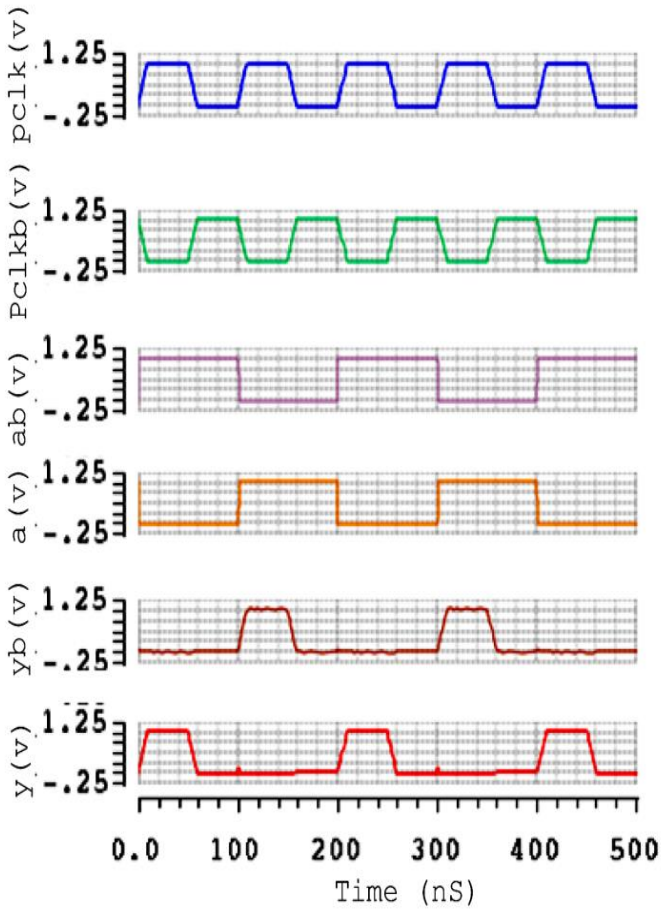

Figure 4. Functionality View of Modified PFAL Inverter/Buffer.

C. FinFET Device

The leakage power is the significant in nanometer CMOS due to reduced channel length. Different alternative device structures are proposed in the literature. Along with this several researchers proposed as gate oxide thickness reduction, and strained silicon technology usage, metal gate structures and high K dielectrics [16]. Among all these FinFET is the attractive solution and cross sectional structure is shown in Figure 5.

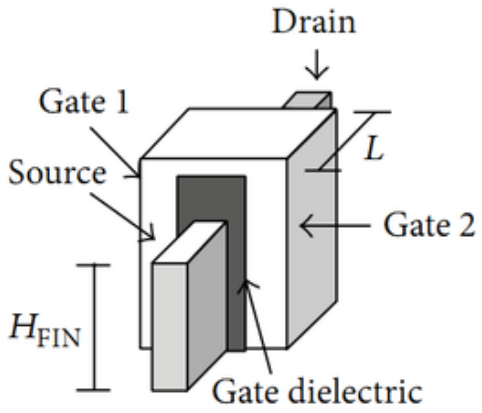

Figure 5. The FinFET Structure

3. Multiplier Design

Vedic sutras are used to implement this multiplier. This UT sutra means vertical and crosswise and provides simplest form of multiplication for any number of bits and also the speed of the vedic multiplier is fast since it the partial product generation and sum in parallel [17]. The basic building blocks of 4x4 vedic multiplier are N, (N/2) multipliers, (N-1), N-bit adders and (N+1) buffers as shown in figure 6. In this work two different structures are analysed. Design 1 employs vedic multiplier with 4-bit Ripple Carry Adder (RCA) using ECRL Logic. Similarly design 2 employs vedic multiplier with Brent Kung Adder implemented using ECRL and MPFAL adiabatic logic families.

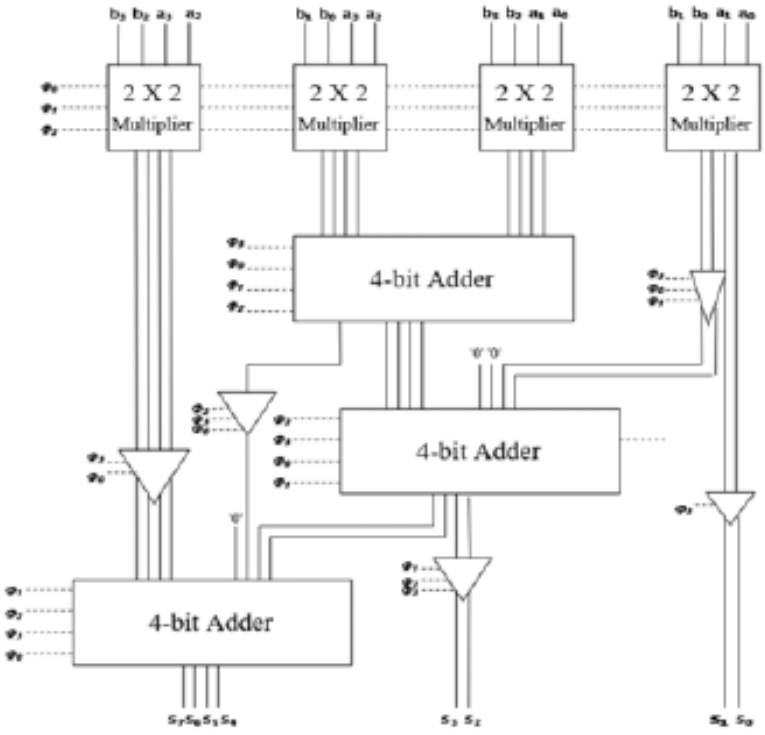

Figure 6. The Structure of 4x4 Adiabatic Vedic Multiplier

4. Simulation Results

Specter simulator is used to verify the functionality of the designed circuits BSIM CMG FinFET models at 45 nm technology node. The different device parameters selected are as follows, Channel Length (L) as45nm, Fin Thickness (T_{fin}) as 15nm, Height of the Fin (H_{fin}) as 30nm, Oxide Thickness (T_{ox}) = 1nm, and threshold voltage of 0.4V. Simulations are carried out over a power clock frequency range of 1-1000MHz and amplitude of 0.7V. The variation of power dissipation of the designed multiplier circuit with power clock frequency using ECRL and MPFAL logic families are compared as shown in figure 7.

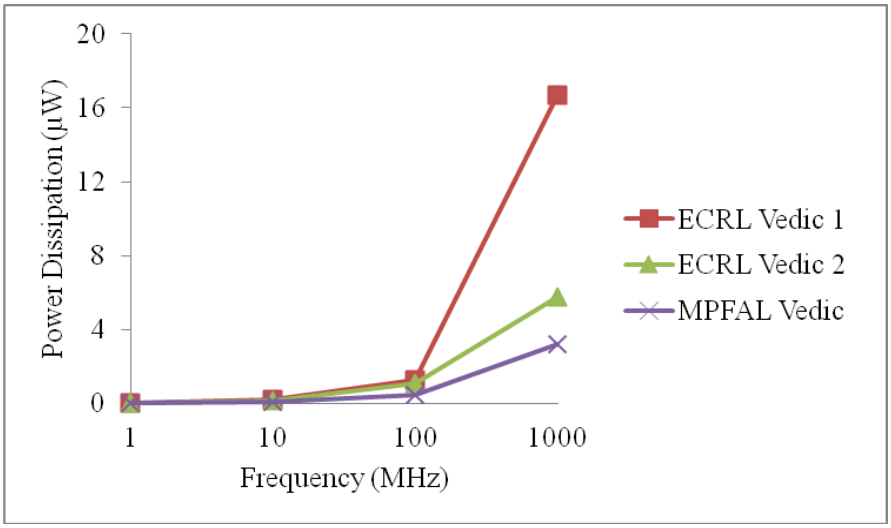

Figure 7. Variation of Power Dissipation with Power Clock Frequency.

The simulation results revealed that the maximum power savings achieved by the ECRL Vedic 2 design using BKA over ECRL Vedic 1 design with BKA is 83. 5%. Similarly the power savings in the range of 40-55% are obtained with MPFAL vedic multiplier compared to ECRL Vedic 2 design, Further, the results are compared with the existing results in the literature as shown in table 1.

Table 1. Power Dissipation Of MPFAL 4-Bit Vedic Multiplier With Exsisting Results

Reference	Technology Node	Power Dissipation (µW)	Delay (nS)
[9]	45 nm (CMOS)	0.675	0.070
[18] Design1	45 nm (CMOS)	0.955	0.138
[18] Design 2	45 nm (CMOS)	0.842	0.268
[11]	180 nm (EEAL) V_{pc}=1V	45.76	0.67
[17]	45 nm (DCPAL) V_{pc}=0.9V	0.484	---
This Work	45 nm (FinFET based ECRL) Vpc=0.7V	0.236	
ECRL Vedic 1			0.105
ECRL Vedic 2		0.161	0.091
MPFAL Vedic	45 nm (FinFET based MPFAL) V_{pc}=0.7V	0.095	0.085

Further, the reliability with temperature is assessed by plotting the variation of power dissipation with temperature in the range of 0-100ºC at a supply frequency of 10MHz illustrated in figure 8.

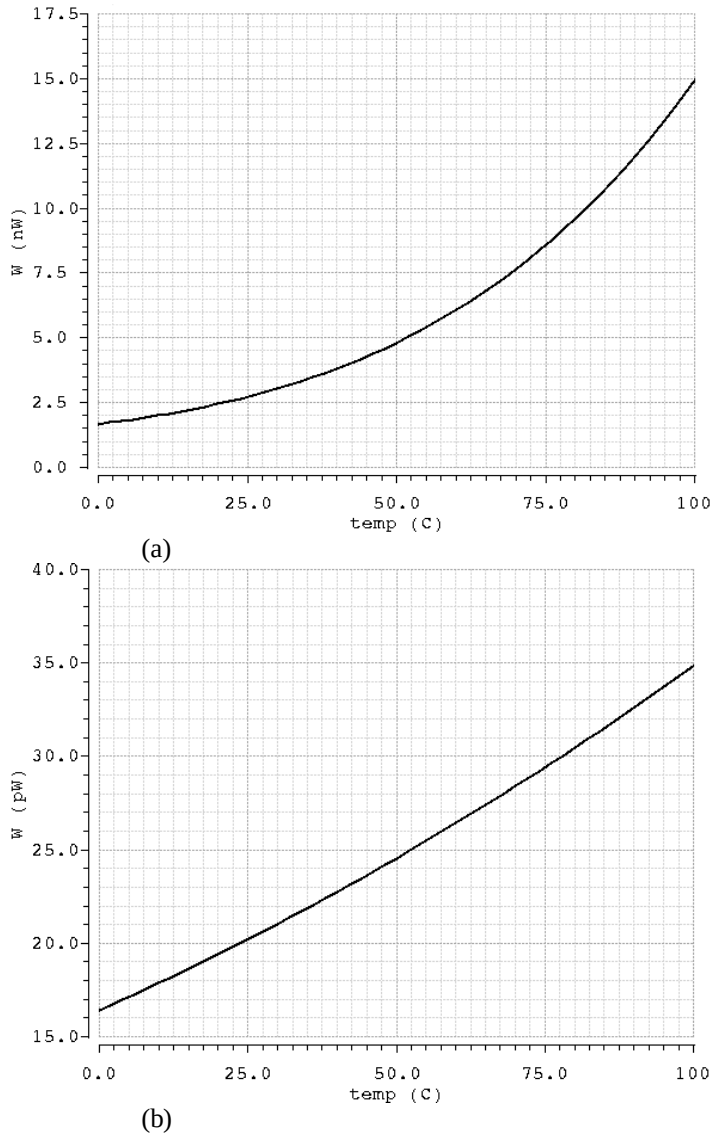

Figure 8. Variation of Power Dissipation with Temperature of (a) CMOS, (b) MPFAL Vedic Multipliers

It is inferred that for the FinFET based MPFAL Vedic multiplier the power dissipation varies linearly with increase in temperature and is found to be of the order of pW. However, for the CMOS based multiplier, the power dissipation varies in a quadratic manner with temperature and it is of few tens of nW. The variation in power dissipation with increase in temperature for the FinFET based MPFAL multiplier is an order of magnitude less compared to CMOS design, indicating the increased reliability of MPFAL circuit at high temperatures.

5. Conclusion

In this paper, MPFAL based multiplier Vedic multiplier is proposed. The performance of the designed module using MPFAL adiabatic logic family is compared with ECRL. The results indicate that power savings of 55% achieved with the MPFAL based vedic multiplier over ECRL designs. The designed module is good choice for ultra-low power applications. The variation in power dissipation with increase in temperature for the FinFET based MPFAL multiplier is an order of magnitude less compared to CMOS design, indicating the increased reliability of MPFAL circuit at high temperatures.

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