

## Multilevel Converter based System Fault Analysis

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**Abstract:** Direct Current deficiency security is the procedure to improve the Direct current system distribution, transmission structure in this review paper examinations the transitory attributes of Direct current responsibilities in a particular (MMC) staggered converter based Direct current the system connection with a numerical technique. Then, loads are reproduction like pretending by using on MATLAB/Simulink has been done by testing the exactness for the hypothetical examination. At last, the mechanical troubles of and necessities for the assurance and confinement are talked about to give the hypothetical establishment to the structure of direct current flow insurance system.

**Keywords:** Direct Current Fault Safety, Direct Current (DC), Error Analysis, Direct Current (DC) Fault Protection, Modular Multilevel Converter MMC, VSC Voltage Source Converter.

### 1. Introduction

Wide development of the distribution generations like the non-conventional energy sources corresponding wind power and solar power [1] and the consistently development of battery-powered vehicles [2] the other DIRECT CURRENT stacks, the Direct flow framework is creating research acceptable enthusiasm because of remunerations of low force misfortune, low speculation, high unwavering quality, etc [3, 4]. Bolstered by the development of the force electronic innovation [5], the adaptable DIRECT CURRENT framework is picking up ubiquity because of the favourable circumstances, for example, having an autonomous force manage and have being insusceptible for [6] recompense disappointment.

In a building method, the two-level VSC gets remained recognized as reasonable gadget interested in incorporating to the dispersed ages and Direct current loads. In any case and it has the disadvantages, for example, high-level exchanging recurrence, extraordinary exchanging power misfortune and poor influence quality [7]. Right now, thought of the MMC system proposed [8, 9] independent for the secluded plan having a low exchanging recurrence and well force quality [10].

Presently, a few specialized difficulties to the advancement of the direct current framework are going up against to us, including the Direct Current flaw insurance, with the issue identification, and issue segregation.

The regular converters, containing the Voltage source converter and modular multilevel converter, are not willing to confine the direct current shortcoming without anyone else. Indeed, at the same time, the SMs in the converter are completely obstructed, the freewheeling diodes despite everything go about as an unrestrained rectifier. These days, near the regularly three Direct current issues (shortcoming) separating strategies.

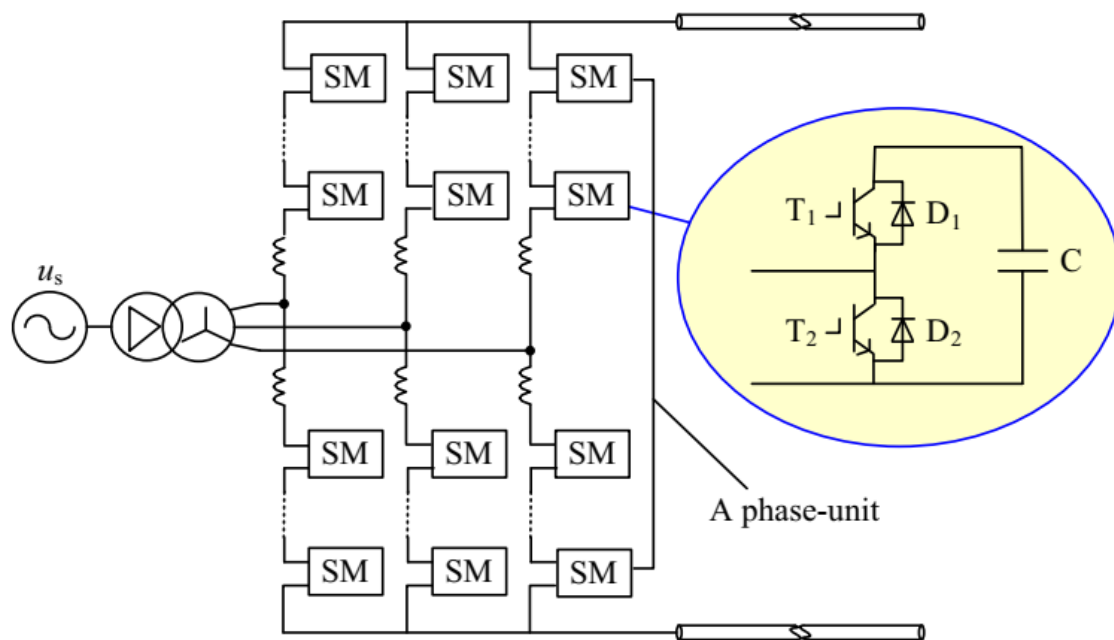
1. The best separating technique is interfering with the issue in-circuit system by Direct current CBS [11] which, be that as it may, are as yet not accessible for building application. Since there is no Direct current electrical switch can meet up the necessities for interfering with limit, activity velocity.
2. Because of the specialized trouble of the Direct current electrical switch, and AC-electrical switch founded separating strategy which could interfere with the Direct current shortcoming design dependably existed in [12]. In any case, the disadvantages of this technique are self-evident: slow reaction of the automatic AC shift equipment and enormous power outage zone in the framework.
3. Because the explanations above specialists exist investigating the 3<sup>rd</sup> strategy, is disposing of the Direct current issues in current by the present converter. Reference [13] introduced another Modular multilevel converter sub-module with Direct current deficiency existing current disposing of capacity. After a Direct current deficiency occurs the problem exciting current might be disposed of because of the inverted voltage in the capacitors to MMC Converter SMs [14] projected the double thyristor control mechanism conspire with the forestalls the AC side current commitment and it permits the direct current link current unreservedly rot to comes to zero. Be that as it may, the downsides in the same way as the thyristors bearing high-pitched  $dv/dt$ , the typical activity ought to be considered. Reference [15] structured a secluding strategy which might be decreasing in the degree of  $dv/dt$  in the thyristors must survive.

There maintain remained a great deal of effort concentrating upon the problem segregation, in any case, the work on shortcoming discovery with id capacity is still infrequently done. In this manner, we need to comprehend direct current deficiency transient attributes. Reference [16] has done a point by point investigation designed for

the direct current blames in the 2-level voltage source converter VSC built dc framework. Since the topology of an MMC is unique to 2 level voltage source converter (VSC) it is imperative towards examine the transitory attributes of direct current blames in a Modular multilevel converter (MMC) based direct current framework. Constructed in this paper exist as per the following: Initially in this paper investigations the momentary qualities of a direct current flaw in the Modular multilevel converter (MMC) based direct current framework, which remains not quite in the same as the attributes in a voltage source converter (VSC) one in reference [16], giving the hypothetical establishment to the structure of the direct current issue insurance. furthermore, in light of the deficiency qualities, this paper talks about the innovative troubles and necessities in the security against direct current faults in the direct current framework. Likewise, the accuracy of a hypothetical examination occurs, checked the reproduction simulations in MATLAB/Simulink.

**1.1 Fault Investigation**

Fault investigation in Modular staggered converter system in DC framework: Figure 1 demonstrates an even bipolar DC framework associated along by the AC framework in the MMC. An MMC comprises to 3 equal associated stage units. One stage unit includes 2 arms, each one is indistinguishable SM arrangement associated, such as appeared in figure one Attributable points of interest like low exchanging misfortunes, minor complete consonant contortion and secluded structure, and so on, MMCs demonstrate unrivalled for developing effective DC conveyance and transmission framework.



**Figure 1.** Block Diagram of the MMC based Direct Current System

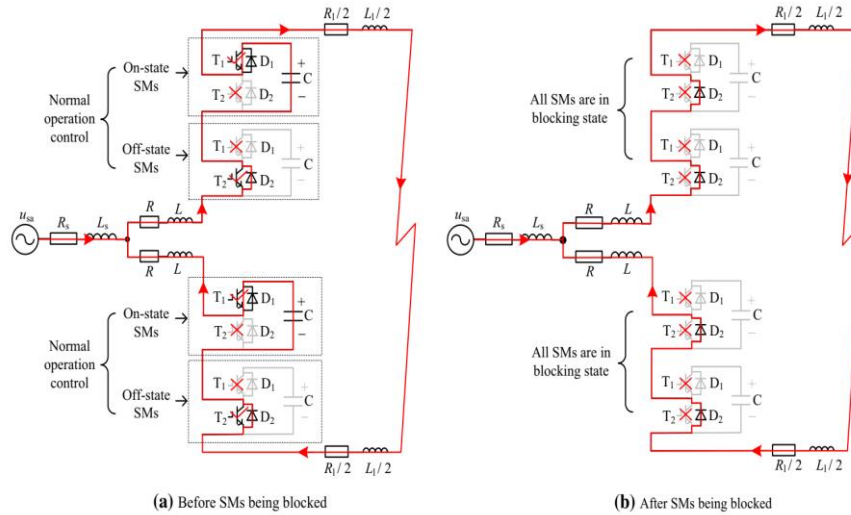
Every SM is primarily included 2 IGBTs (Thyristor 1, Thyristor 2), two freewheeling diodes (Diode1, Diode 2), just as a unit capacitor (C). Contrasted and the traditional 2 level Voltage Source Converter (VSC) the main distinction for the duration of the ordinary activity remains the regulation methodology. Modular multilevel converter (MMC) receives the progression beat tweak which has favourable circumstances, for example, low exchanging misfortunes, high quality of waveform conversely within the waveform regulating (PWM), the 2 level Voltage Source Converter embraces [9].

Deficiency current separating method and security methodology are fundamental to the steadiness and unwavering quality of the force matrix. Thus, in the basic to research direct current shortcoming temporary qualities and the effect on the Direct Current-side framework, alternating current (AC) side framework and converter. Around are 3 sorts of direct current issues, i.e Direct Current detachment shortcoming, direct current post-to-earth issue and direct current shaft-shaft issue. The most part, the harm of a direct current shaft to-post issue is the simplest [17].

In these paper investigations of the ephemeral attributes of a direct current shortcoming under the direct current post-shaft deficiency situation. In these applications, all the thyristors (IGBT) should be before long killed after a direct current cut off. FIGURE 2 outlines the deficiency current way when killing the IGBTs. Subsequently, the direct current issue transient procedure could be separated into three phases 'SMs typical activity arrange', 'Introductory stage in the wake of hindering submodules (SM) and unrestrained rectifier arrangement.

**1.2 Sub Modules Operation in Normal Period**

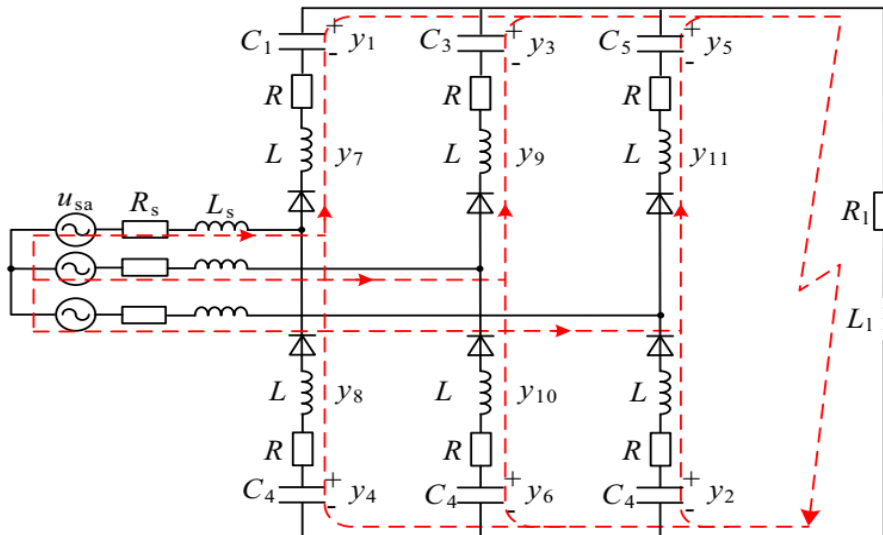
In this period, the Modular Multi level Converter is even at work in the usual switching approach. The DC burden current is delivered into the Alternating current side supply and set of capacitors in the on-state-run of the submodules. Consequently, the burden current transient path might be demonstrated as represents in the red line in figure 2a, anywhere we have done a basically investigate phase-1 below a direct current pole to pole burden situation, and the evaluation would be used to stages 2 and 3. in the figure.2a,  $U_{sa}$  phase-1 Alternating current voltage,  $R_s$  &  $L_s$  exist the approximate impedance total of the Alternating Current side scheme & the transformer, the resistance, inductance of the support reactors,  $R_l$ ,  $L_l$  are the corresponding resistance,



**Figure 2.** Corresponding Circuit of Direct Current End to End Fault

the inductance of direct current SC line. normally, the direct current scheme is grounded across high similar resistors, and the resistance in the circuit system fault is actual insignificant, the equivalent resistance will be neglected, likewise, the circulated capacitance of the capacitor in the direct current wire is also neglected in the cell capacitors.

The SC will be redrawn as the shown in the figure. 3. it also will be known that the number of on state Sub Modules in individually limb are not identical while a direct current fault occurs, affording into the standard process governor approach. for the alternating current side scheme, the direct current system fault will be restrained as an irregular fault and the solution of its provisional procedure includes elevated order two or more dimensional mathematical solutions for the equations it makes difficult to find the logical result. So, we can obtain for the mathematical scheming solution.



**Figure 3.** Comparable Fault Circuit During Sub-Modules Normal Functioning Stage

In Figure 3, around sixteen power storage area elements and five cut-sets just containing inductances(L), therefore we get eleven state variables, we can take choice of six capacitor voltages ( $y_1$ \* $y_6$ ) and five-arm reactor currents ( $y_7$ \* $y_{11}$ ) in the same way the state variables, the advancing instructions to the state variables remain renowned. Formerly the passing state would be conveyed by equation1 can be communicated by a matrix form demonstrated as

$$\left\{ \begin{array}{l} y_1 - Ry_7 - Ly'_7 - Ly'_8 - Ry_8 + y_2 \\ \quad = y_3 - Ry_9 - Ly'_9 - Ly'_{10} + y_4 \\ y_1 - Ry_7 - Ly'_7 - Ly'_8 - Ry_8 + y_2 = y_5 - Ry_{11} \\ \quad - Ly'_{11} - L(y'_7 + y'_9 + y'_{11} - y'_8 - y'_{10}) \\ \quad - R(y_7 + y_9 + y_{11} - y_8 - y_{10}) + y_6 \\ y_1 - Ry_7 - Ly'_7 - Ly'_8 - Ry_8 + y_2 = \\ \quad R_1(y_7 + y_9 + y_{11}) + L_1(y'_7 + y'_9 + y'_{11}) \\ u_{sa} - R_s(y_7 - y_8) - L_s(y_7 - y_8) - Ly'_7 - Ry_7 + y_1 \\ \quad = u_{sb} - R_s(y_9 - y_{10}) - L_s(y'_9 - y'_{10}) - Ly'_9 - Ry_9 + y_3 \\ u_{sa} - R_s(y_7 - y_8) - L_s(y_7 - y_8) - Ly'_7 - Ry_7 + y_1 = u_{sc} \\ \quad - R_s(y_8 + y_{10} - y_7 - y_9) - L_s(y'_8 + y'_{10} - y'_7 - y'_9) \\ \quad - Ly'_{11} - Ry_{11} + y_5 \\ C_1y'_1 = -y_7, C_2y'_2 = -y_8, C_3y'_3 = -y_9, C_4y'_4 = -y_{10} \\ C_5y'_5 = -y_{11}, C_6y'_6 = -(y_7 + y_9 + y_{11} - y_8 - y_{10}) \end{array} \right. \quad (1)$$

The above Equation 1 can be conveyed in a matrix form showed as shown in equation 2.

$$\begin{bmatrix} y'_1 \\ \vdots \\ y'_{11} \end{bmatrix} = -A^{-1}B \begin{bmatrix} y_1 \\ \vdots \\ y_{11} \end{bmatrix} - A^{-1}C \begin{bmatrix} u_{sa} \\ u_{sb} \\ u_{sc} \end{bmatrix} \quad (2)$$

Where

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -L & -L & L & L & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -2L & L & -L & 2L \\ 0 & 0 & 0 & 0 & 0 & 0 & -(L+L_1) & -L & L_1 & 0 & -L_1 \\ 0 & 0 & 0 & 0 & 0 & 0 & -(L_s+L) & L_s & L_s+L & -L_s & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -(2L_s+L) & 2L_s & -L_s & L_s & L \\ C_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & C_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_3 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_4 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_5 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_6 & 0 & 0 & 0 & 0 & 0 \end{bmatrix};$$

$$B = \begin{bmatrix} 1 & 1 & -1 & -1 & 0 & 0 & -R & -R & R & R & 0 \\ 1 & 1 & 0 & 0 & -1 & -1 & 0 & -2R & R & -R & 2R \\ 1 & 1 & 0 & 0 & 0 & 0 & -(R+R_1) & -R & -R_1 & 0 & -R_1 \\ 1 & 0 & -1 & 0 & 0 & 0 & -(R_s+R) & R & R+R_s & -R_s & 0 \\ 1 & 0 & 0 & 0 & -1 & 0 & -(2R_s+L) & 2R_s & -R_s & R_s & R \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 1 & -1 & 1 \end{bmatrix};$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T.$$

Form the above matrix we will write the state calculation arrangement as follows

$$\begin{cases} y'_1 = f_1(t, y_1, y_2, \dots, y_{11}) \\ y'_2 = f_2(t, y_1, y_2, \dots, y_{11}) \\ \vdots \\ y'_{11} = f_{11}(t, y_1, y_2, \dots, y_{11}) \end{cases} \quad (3)$$

The above equations know how to be solved by using Runge Kutta methode

$$\begin{cases} y_{i,n+1} = y_{i,n} + \frac{h}{6}(k_{i1} + 2k_{i2} + 2k_{i3} + k_{i4}) \\ k_{i1} = f_i(t_n, y_{1n}, y_{2n}, \dots, y_{11n}) \\ k_{i2} = f_i(t_n + \frac{h}{2}, y_{1n} + \frac{h}{2}k_{11}, y_{2n} + \frac{h}{2}k_{21}, \dots, y_{11n} + \frac{h}{2}k_{m1}) \\ k_{i3} = f_i(t_n + \frac{h}{2}, y_{1n} + \frac{h}{2}k_{12}, y_{2n} + \frac{h}{2}k_{22}, \dots, y_{11n} + \frac{h}{2}k_{m2}) \\ k_{i4} = f_i(t_n + h, y_{1n} + hk_{13}, y_{2n} + hk_{23}, \dots, y_{11n} + hk_{m3}) \\ i = 1, 2, \dots, m \quad m = 11 \end{cases} \quad (4)$$

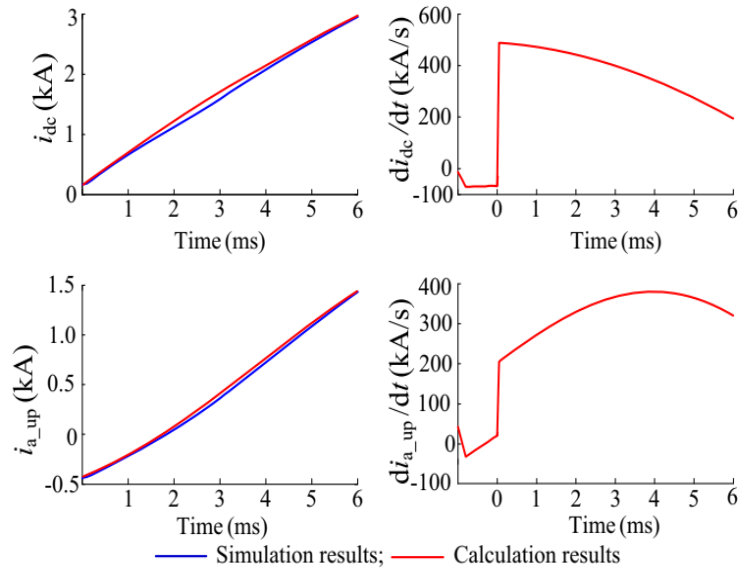
where  $t_n$  is the examining succession number;  $y_i, n$  and  $y_i, n+1$  are the estimations of variable  $y_i$  at the snapshots of  $t_n$  and  $t_{n+1}$ , and  $h$  is the iterative guessing stage. Through comprehending equation number 3 by acquire temporary reaction of initial state issues. In the Figure number 4 demonstrations the reenactment in addition to estimation the results, someplace indirect current is present coursing complete the Direct Current link; ia upper side is the upper limb current of stage A. since in Fig. 4, the hypothetical examination consequence of the deficiency current right now extremely near the reproduction result. What's more, the outcome likewise shows that the deficiency current goes up quickly, yet in addition the present derivative rate of change  $di/dt$  remains in an elevated level probably am aware, the types of electric gear might be not able to hold up under huge short out flow, and an extreme derivative of current with respect to time  $di/dt$  could be prompt by consuming of IGBTs on account to the nearby hotness. Along these lines, in turf application, for the shortcoming recognition isn't sufficiently quick to hinder the SMs, they would likewise be obstructed on the double the issue current or derivative of current with respect to time  $di/dt$  surpasses the edge estimations of the identity-insurance for IGBTs. From same point forward, the ephemeral procedure will come to following show identified as 'Starting stage in the wake of blocking Sub modules are to be blocked.

Primary stage in wake of blocking Sub modules in the circuit appeared as Fig 2b, D2freewheeling diodes in any case, take an enormous issue current regardless of whether the total of what IGBTs have been killed. Right now, capacitor chambers in blocking Sub modules are avoided by the deficiency current and in this way would be stop releasing. As such, the capacitor chambers release completely just main period examined in before 2.1 section. Nonetheless, the apparatuses in the arms empower every single freewheeling diode set apart as D2 to direct constantly much after the capacitor releases breaks. In the meantime, the AC-side the source takes care of the flawed current over diodes, arm reactors as well as the diodes empower the progression in the alternating current completely the moment despite the unidirectional trademark as a result of the freewheeling diode current as of reactors. Right now, in these the deficiency network is proportionate shows in Fig. 5. As per the superposition hypothesis, the issue currently is underwritten by the present took care of by the alternating current block side, it provided by the arm reactor. Subsequently it should keep all the diodes  $D_2$  operational below the situation, and the direct current issue will be examined as a 3 stage cut off from the alternating current block side framework, the network is equal to as shown in Fig. 6a. In meantime, the release of the support reactors is outlined as shown in Fig. 6b. Right now, Sub modules are to be blocked, we accept the voltage, current of the stage and are  $u_{sa}=Um \sin(\omega t+\phi_0)$  and  $I_{sa0}$  individually, and the current of the direct current link is  $I_{dc0}$  current. As per the fathoming strategy for the energetic circuit in the stage A the current  $i_{sa}$ , the dc link current  $i_{dc}$  are illuminated as

$$i_{sa} = I_m \sin(\omega t + \phi_0 - \varphi) + [I_{a0} - I_m \sin(\phi_0 - \varphi)] e^{-\frac{t}{\tau_1}} \quad (5)$$

$$i_{dc} = I_{dc0} e^{-\frac{t}{\tau_2}} \quad (6)$$

where  $I_m = \frac{U_m}{\sqrt{(R_S+R/2)^2 + [\omega(L_S+L/2)]^2}}$ ;  $\varphi = \arctan \frac{\omega(L_S+\frac{L}{2})}{R_S+\frac{R}{2}}$ ;  
 $\tau_1 = \frac{L_S+\frac{L}{2}}{R_S+\frac{R}{2}}$ ;  $\tau_2 = \frac{\frac{2L}{3}+L_l}{\frac{2R}{3}+R_l}$ .



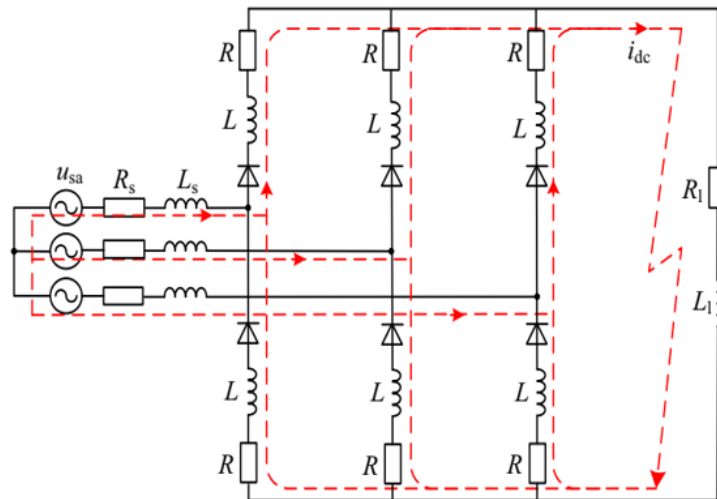
**Figure 4.** Find Fault With current and ratio of di/dt of Direct Current responsibility during Sub modules are in standard operating point

The higher and lower armaments of every stage into the modular multi-level converter remain carefully balanced, so that flows took care of interested in the two arms by the air conditioner adjacent source are equivalent in esteem. In like manner,  $i^{dc}$  is equally isolated into the three stage units. In this way, the flows of the higher and lower arms of stage an ( $i_{a\_up}$  and  $i_{a\_low}$ ) could be communicated as

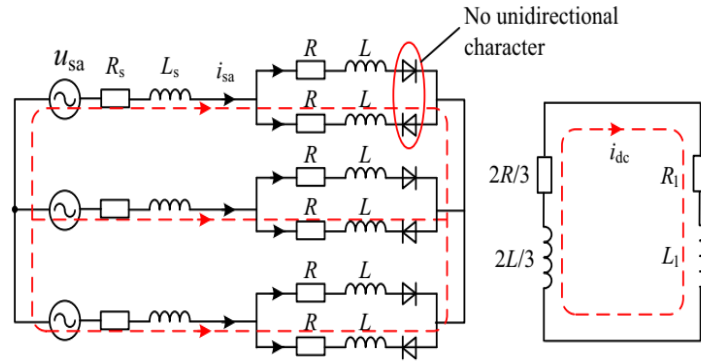
$$\begin{cases} i_{a\_up} = \frac{i_{dc}}{3} + \frac{i_{sa}}{2} \\ i_{a\_low} = \frac{i_{dc}}{3} - \frac{i_{sa}}{2} \end{cases} \quad (7)$$

Figure 7 shows the reproduction and hypothetical computation brings about this stage ( $t_1 * t_2$ ). What is more, the previous confirms the accuracy of the hypothetical examination, likewise be understood the current of DC link rots step by step by, the current from the AC side has a similar waveform as 3 stage shortcoming current, the support current in MMC is the superposition of the earlier dualistic.

Even though the entirety of the submodules is hindered right now, of being diminished, the shortcoming flows from the AC source side, in the converter rise altogether, which would reason for system damage.



**Figure 5.** Equivalent circuit for fault during primary stage after stopping Submodules



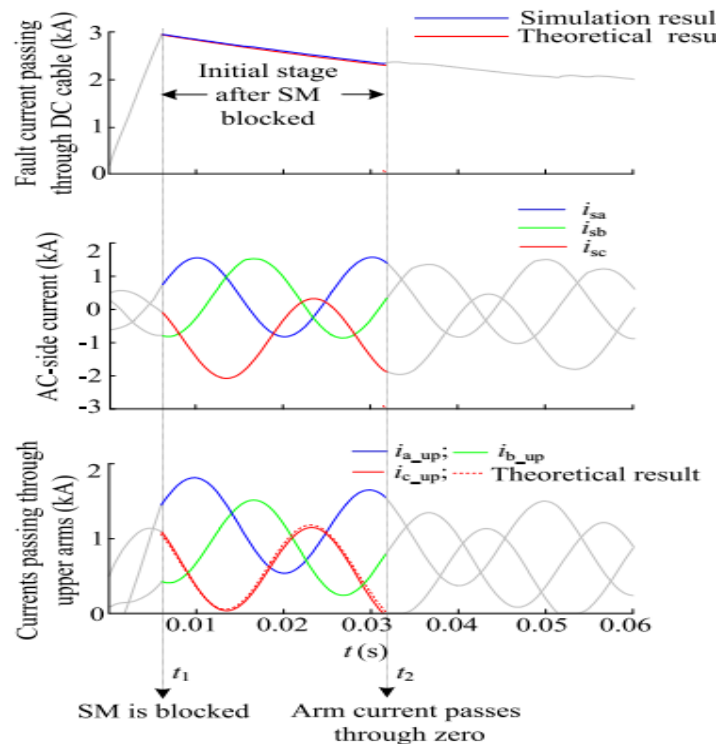
(a) Input power from AC side (b) Supply from the arm reactors side

**Figure 6.** Fault current disintegration during introductory stage in the wake of blocking SMs

harm to the framework, particularly to the Alternating Current side framework and the semiconductor diodes in the converter. As appeared in Figure. 7, the current of the higher arm of stage C shows zero at the time  $t_2$ , from when the semiconductor diode D2, the comparing arm start to demonstration the unidirectional trademark. The 3 stage shortcoming state stops, the issue momentary procedure would come into the following period.

Hysterical rectifier organize in this point, the proportionate circuit is still appeared as Figure. 5. Be that as it may, with slowly rotting of the immediate current deficiency current indirect current, there will be the point at which every one of the 6 arms has experienced a minute once its present arrives at 0 and afterward it need to take thought the unidirectional attribute of the semiconductor diode D2 in all the 6 arms, which causes the MMC to proceed as an uncontrolled rectifier. So, the last transient time frame can be considered as an uncontrolled rectifier arrange approximatively.

Figure 8 represents the reproduction aftereffects in the Stage 3. After individual of the arm flows ( $i_{c\_up}$  right now) at zero, the remnant arms despite everything have flows moving through them, formation of the reactors in them continue releasing and the freewheeling diode flows keep on rotting. bit by bit, in the momentary procedure becomes into a steady state similar to the uncontrolled rectifier. Because of the presence of the enormous device in each arm, in attendance must be a compensation covering wonder in the MMC due to the freewheeling diode flows. Relating examination technique resembles the way that we ascertain the current in an uncontrolled rectifier which deliberates the effect of the inductance [18]. In derelict, this issue flows at the Direct Current side, air conditioning adjacent and in the converter exist constantly. Since the proportionate impedance of shortcoming circuit is very little, the flows would be extensively enormous.



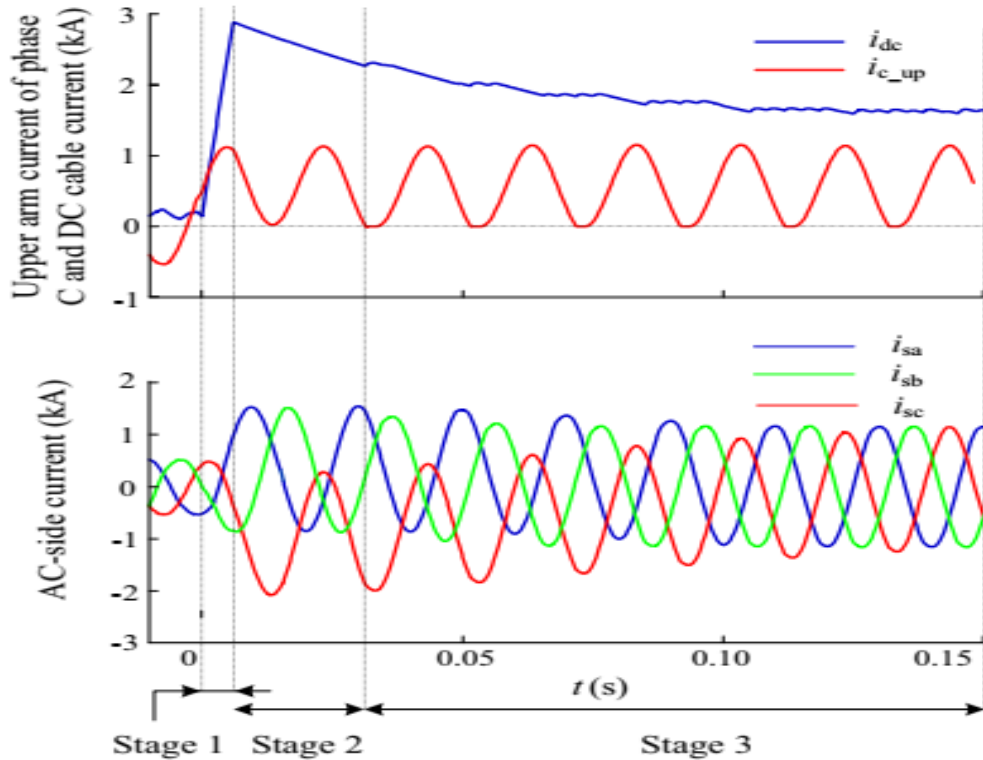
**Figure 7.** Results of Introductory Period after SMs are Blocked

**2. Security Prerequisites**

Security prerequisites for direct current framework figure 8 additionally illustrations the entire passing procedure of the direct current shaft to-post flow. As indicated by the hypothetical examination and the reproduction results, the transient procedure can be divided into three phases.

phase 1: right now, submodules are not blocked in the sub modules the capacitors and the alternating current side sources provender the current problem synchronously. The current in the arm, the current in the dc link ascent quickly. As per the transient attributes of the direct current issue, margarine this type of stage can diminish the overcurrent equal altogether, do profit the recuperation in the framework.

Phase 2: right now, reactors from the network system the arms release consistently the input ac side feed three stage deficiency current from the entire direct current framework, particularly the air conditioner side framework and the gadgets in the mmc arms, the overcurrent right now the most genuine on account of the three stage flow current from the input ac-side sources. In this way and should take measures to limit the damaging impacts applied to the framework.



**Fig. 8.** Total procedure of Direct Current shaft to-post deficiency

One technique is abbreviating to the term of present stage, which relies upon its zero intersection period of the arm current the prior the arm current demonstrations up at zero position, the extra rapidly the stage will end. From equation (5) to equation (7) would be getting the inference deterioration speed of the proceeding with current in the reactors having a course on the zero intersection time the littler the rot constants  $T_1$ ,  $T_2$  are, at that point, the previous the arm current shows up at zero and the a smaller amount of time this stage goes on along these lines, can abbreviate the length of this phase by diminishing the estimation of  $T_1$ ,  $T_2$  which could be acknowledged by expanding the opposition in the flaw circuit falsely.

Phase 3: right now, activity condition of the modular multi-level converter (MMC) is like that of an abandoned rectifier. Meanwhile the ohmic resistance of the direct current short link is inconsequential, the flaw current in the entire framework is still nearly huge. In any case, the direct current deficiency cannot be hindered with fast and security on the grounds that there is no dependable business direct current electrical switch up to now. In that capacity, the security procedure for the mmc based direct current framework must have following properties.

1. Observing the transient procedure of the direct current deficiency, the overcurrent top is subject to the blocking snapshot of the IGBTs. In another word, if the flaw location is sufficiently quick to give a blocking sign to the SMS (before the IGBT self-assurance), the overcurrent level of the framework could be decreased altogether.
2. Even if all the IGBTs are killed during a direct current deficiency, the flaw current exists constantly because the freewheeling diodes go about as an uncontrolled rectifier. In this way, under the condition that enormous limit direct current electrical switch is still far away from the business application, the quick and



proficient flaw detaching strategy must be proposed, which is likewise founded on the quick deficiency identification.

3. In a multi-terminal direct current framework, a comparable transient procedure happens at every converter station. In this manner, distinguishing the shortcoming area utilizing single-end data turns into a key system.

### 3. Conclusions

In this presentation investigations the passing qualities of the direct current issue. Hypothetical investigation and reenactment scrutiny demonstration that the passing procedure would be partitioned into 3 phases. In stage 1, the primary harm to be brought about the extraordinary di/dt level from the force electronic gadgets and the over current to direct current link. In step 2 and 3, the extreme overcurrent happens in the ac block, direct current block and in the converter itself. Thus, the fundamental plan an effective direct current protection methodology, particularly the rapid deficiency discovery, quick issue disconnection and solid shortcoming id. Index the modular multilevel converter based direct current framework is based on MATLAB/Simulink. modular multilevel converter has a similar design through it appears in figure 1. The solid constraints of the framework remain recorded in table 1. Table 1 parameters of modular multilevel converter direct current framework constraints value.

**Table 1.** Modular Multi-level Converter-based DC Framework

S.NO	PARAMETERES	VALUES
1	Rated power	100MVA
2	Rated direct current voltage	±12 Kv
3	Rated AC voltage	12.8 kV
4	Arm reactor	80 mH
5	Sub-module capacitor	1000 µF
6	DC Wire Resistance	0.189 X/km
7	DC Wire Inductance	0.160 mH/km

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