Design and Simulation of variable gain amplifier using cadence Tool

Dr. Usthulamuri Penchalaiah [1], Devandla Vamsi[1], Aata Siddardha[1], Banka Pavan Kumar Reddy[1], Bachu Gnaneswar[1]

[1]Department of Electronics and Communication Engineering, Geethanjali Institute of Science and Technology, Nellore.

Abstract: The radio frequency (RF) amplifiers are widely used in a variety of communication systems. However, the conventional analog RF resulted in reduced volage gain, magnitude, and phase responses. So, this work provides an overview of a research paper focused on the design and analysis of a single-stage variable gain amplifier (SSVGA) utilizing cascaded linear transconductance amplifier (Gm cell) and linear transimpedance amplifier (TIA) blocks with feedback via shunt resistors. The SSVGA architecture aims to maintain constant bandwidth while offering controllable voltage gain, making it versatile for applications with varying input signal strengths. The first stage of the SSVGA is realized as a current mode TIA, converting the input voltage signal to an output current efficiently. The second stage features a Gm cell with source degeneration, enhancing bias current efficiency and transconductance at the supply voltage. The proposed SSVGA design offers flexibility and adaptability, making it suitable for diverse communication systems and signal processing applications. The incorporation of feedback control ensures consistent performance across different voltage gain settings, resulting in a robust and efficient solution for varying signal strengths.

Keywords: Variable Gain Amplifier, Transconductance Amplifier, Transimpedance Amplifier, Voltage Gain.

1. Introduction

With the rapid advancement of wireless communication technologies, modern RF receivers [1] are required to operate efficiently with low power consumption while maintaining high-performance characteristics. One crucial component in an RF receiver is the VGA, which plays a vital role in dynamically adjusting the signal strength to optimize the receiver's performance under varying signal conditions [2]. The VGA is responsible for controlling the gain of the received signal, allowing the receiver to adapt to different input signal levels and noise environments [3]. It enables the receiver to maintain a stable output signal with minimized distortion, maximizing the overall system performance in terms of dynamic range, linearity, and signal-to-noise ratio (SNR).

This research focuses on the design and implementation of a Low-Power Compact CMOS VGA, emphasizing its suitability for modern RF receivers. CMOS (Complementary Metal-Oxide-Semiconductor) technology [4] is chosen for its advantages in terms of low cost, low power consumption, and compatibility with integration on a single chip with another RF circuitry [5]. Power efficiency is a critical requirement in modern RF receivers, especially in battery-operated devices such as smartphones, IoT devices [6], and wireless sensors. The proposed VGA aims to minimize power consumption while maintaining high gain accuracy and linearity [7]. Modern RF receivers demand miniaturization to meet the requirements of portable and wearable devices. The compact VGA design ensures a smaller footprint, making it suitable for integration into highly integrated RF systems [8]. The VGA must provide a wide range of gain control to accommodate different signal levels while preserving a constant output signal level. Precise and linear gain control is crucial to avoid distortion and maintain the receiver's desired performance metrics [9].

2. Literature Survey

Non-linearities in the amplifier's gain response can lead to distortion, intermodulation, and unwanted signal artifacts. The VGA should exhibit high linearity over the entire gain range to ensure accurate signal reproduction and minimize signal degradation [10]. Modern RF receivers often operate across a wide range of frequencies to accommodate multiple communication standards. The VGA should be designed to cover the required frequency range without compromising its performance. The VGA's noise figure directly impacts the receiver's sensitivity and ability to detect weak signals. Minimizing noise contributions from the VGA is essential to improve the receiver's sensitivity and overall system performance.

Panchal et al. [11] introduced a VGA using a Dynamic Threshold MOS transistor (Combined Bulk-Gate Driven-DTMOS) to stabilize the varying signal intensity received at the antenna, thereby ensuring effective baseband processing. Santos et al. [12] proposed a new low-power and low-voltage configurable-gain small-signal amplifier based on an active negative resistance circuit. The design incorporates an improved technique for controlling output common-mode voltage stability in all gain ranges using a replica bias strategy. Ramakrishna et al. [13] presented an Inductor Less Low Power Low Noise Amplifier for Wireless Applications. This inductor-less LNA, implemented in a 45 nm GPDK CMOS technology, is based on a common-gate configuration embedded with a common-source stage to enhance the overall transconductance of the circuit. Khan et al. [14] conducted a correlative analysis of dissimilar mixer architectures, investigating efficient methods to design mixers with wideband operation, lower power consumption, small size, high noise performance, minimal cost, and high conversion gain (dB). Ceolin et al. [15] introduced LNA capable of operating at 2.4 GHz with a 0.4 V power supply. It utilizes an inverter-based amplifier

with improved gate bias voltage and automatic forward bulk biasing to achieve moderated channel inversion levels. The study explores a biasing metric to analyze the best dimensions and bulk bias voltages for the NMOS transistor.

3. Proposed Methodology

Figure 1 depicts the component parts that will make up the SSVGA circuit that has been suggested. A VGA is an electronic component used in communication systems, receivers, and other applications where the incoming signal's strength may vary. The purpose of a VGA is to provide controllable gain to the input signal, allowing the system to adapt to different signal strengths and maintain a consistent output level. A SSVGA typically consists of two amplification stages, each responsible for a portion of the total gain. The first stage is often a transconductance amplifier (Gm cell), which converts the input voltage signal into an output current proportional to the input voltage. The second stage is typically a TIA, which converts the output current of the first stage back into an output voltage signal. This two-stage design allows for greater flexibility in controlling the overall gain of the amplifier. The feedback via shunt resistors in each stage helps maintain a constant bandwidth regardless of the amount of voltage gain applied. This feedback mechanism stabilizes the amplifier's frequency response, ensuring that the amplifier operates consistently across different gain settings. The control circuitry in the VGA allows the gain to be adjusted based on the input signal's strength or other system requirements. By adjusting the gain, the VGA can handle signals with a wide range of amplitudes while still delivering a stable and consistent output.

Figure 2 shows the diagram of the VGA circuit's single stage. The first stage is a Current Mode TIA, which is responsible for converting the input voltage signal into an output current. It is represented by transistors P1 to P6 and N3 to N6 in the circuit diagram. The TIA's primary function is to provide transimpedance, which means the output current is directly proportional to the input voltage. The second stage is a Gm cell with source degeneration, represented by transistors N1 and N2 along with resistor Rs in the circuit. The G_m cell's main function is to convert the output current from the first stage back into an output voltage signal. Source degeneration using resistor R_s helps in improving bias current efficiency and enhancing transconductance (g_m) at a given supply voltage.

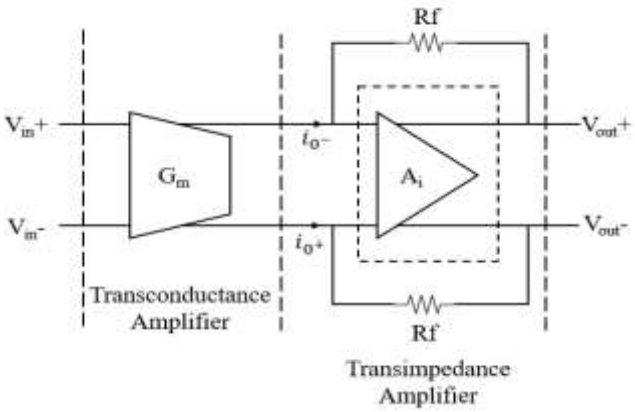

Figure 1. Circuit design of variable gain amplifier.

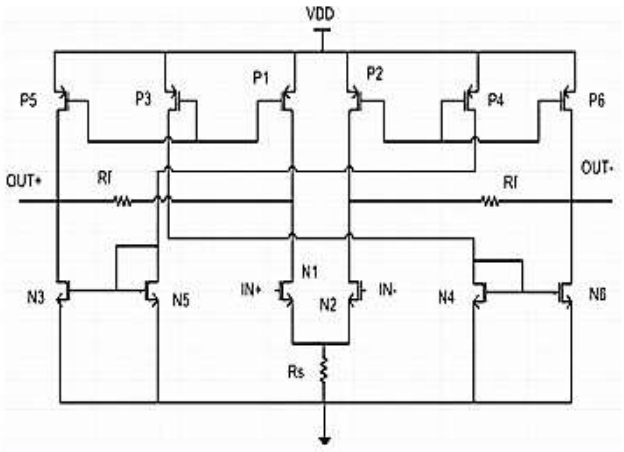

Figure 2: Transistor layout of VGA.

4.Results and Discussions

This section gives a detailed analysis of simulation results, which are developed using Cadence software. Figure 3 illustrates the circuit diagram or schematic of the SSVGA, providing a visual representation of its internal components, connections, and topology. It might include transistors, resistors, capacitors, and other electronic components arranged in a specific configuration to achieve variable gain amplification. Figure 4 presents the results of simulating the SSVGA circuit. It could include metrics such as frequency response, gain, distortion, or other performance parameters, providing insights into how well the SSVGA performs under simulated conditions.

Figure 5 shows the simulation results of the SSVGA for different feedback resistor (R_f) values. It may demonstrate how changing the feedback resistor affects the performance characteristics of the amplifier, such as gain, bandwidth, or distortion. Figure 6 displays the relationship between frequency and gain of the SSVGA. It helps visualize how the amplifier's gain varies across different frequencies, providing insights into its frequency response characteristics. Figure 7 illustrates the magnitude response of the SSVGA across different frequencies. It shows how the amplitude of the output signal changes with frequency, which is essential for understanding the amplifier's frequency-dependent behaviour. Figure 8 depicts the phase response of the SSVGA across different frequencies. It shows how the phase shift of the output signal changes with frequency, which is crucial for applications where phase coherence is essential, such as in communication systems or audio processing.

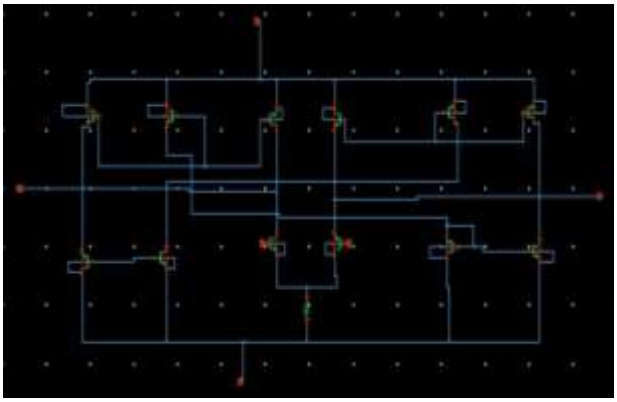

Figure. 3: Schematic diagram of SSVGA.

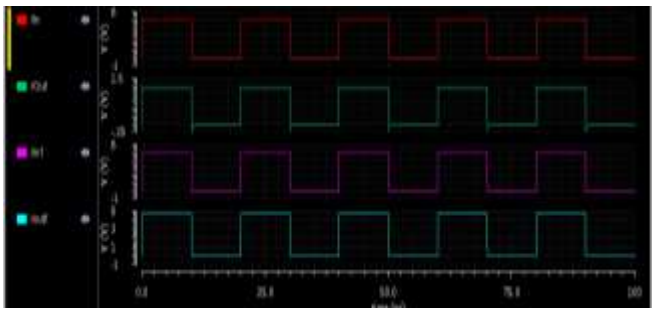

Figure. 4: Simulation outcome of SSVGA.

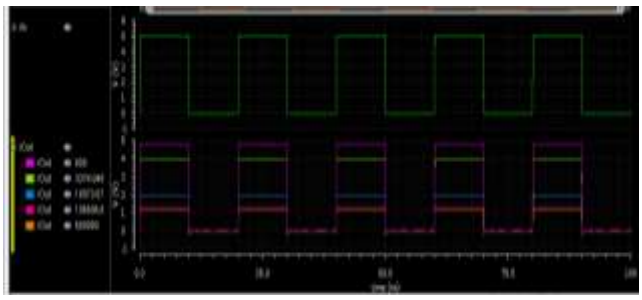

Figure. 5: Simulation outcome of SSVGA for various R_f values.

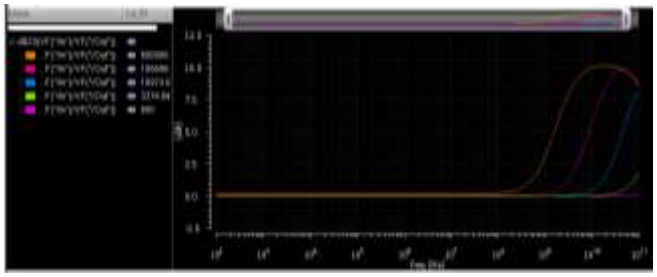

Figure. 6: Frequency vs Gain plot.

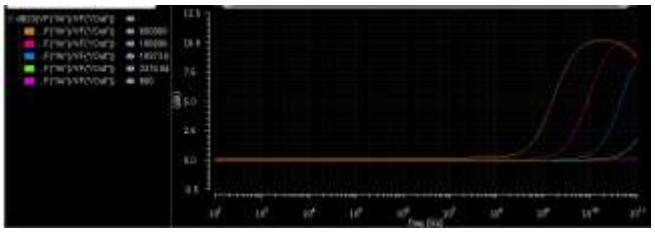

Figure. 7: Frequency vs Magnitude plot.

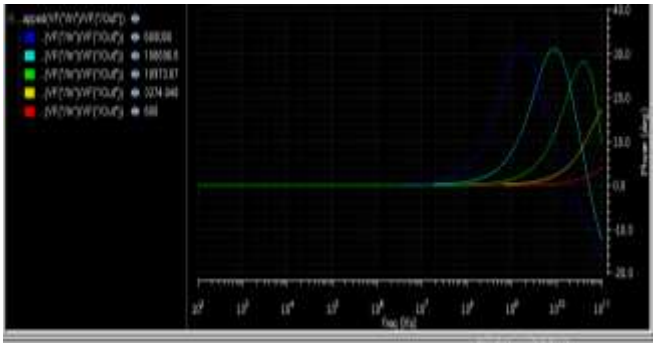

Figure. 8: Frequency vs Phase plot.

5. Conclusion

The proposed SSVGA design offers flexibility, adaptability, and improved performance over conventional analog RF amplifiers. Its ability to provide constant bandwidth and controllable voltage gain makes it an excellent choice for a wide range of communication systems and signal processing applications. The combination of the TIA and Gm cell stages, along with the incorporation of feedback control, results in a powerful and reliable amplifier solution for handling varying input signal strengths efficiently. This research work presents a significant contribution to the field of RF amplifier design and holds promising potential for future advancements in communication technology. The SSVGA design can be further optimized and tailored to meet the specific requirements of 5G systems, such as wider bandwidths, higher data rates, and varying signal strengths.

References

[1] Salem, Jebreel M., Fariborz Lohrabi Pour, and Dong Sam Ha. "High temperature RF transceiver design for high-speed downhole communications." Microelectronics Journal 129 (2022): 105609.

[2] Wang, Qing, et al. "A reconfigurable wireless superheterodyne receiver for multi-standard communication systems." International Journal of Electronics 110.5 (2023): 882-897.

[3] Tasci, Eyyup, et al. "Robust Task-Specific Beamforming with Low-Resolution ADCs for Power-Efficient Hybrid MIMO Receivers." arXiv preprint arXiv:2212.00107 (2022).

[4] Sung, Barosaim, et al. "A Single Path Digital-IF Receiver Supporting Inter/Intra 5-CA With a Single Integer LO-PLL in 14-nm CMOS FinFET." IEEE Journal of Solid-State Circuits 57.12 (2022): 3646-3655.

[5] Steinweg, Luca, et al. "8.0-pJ/bit BPSK Transmitter With LO Phase Steering and 52-Gbps Data Rate Operating at 246 GHz." IEEE Transactions on Microwave Theory and Techniques (2023).

[6] Ma, Rui, Florian Protze, and Frank Ellinger. "A 5.5–7.5-GHz band-configurable wake-up receiver fully integrated in 45-nm RF-SOI CMOS." IET Circuits, Devices & Systems 16.7 (2022): 525-542.

[7] Jaya, Gibran Limi, et al. "An equivalent-time sampling millimeter-wave ultra-wideband radar pulse digitizer in CMOS." IEEE Transactions on Circuits and Systems I: Regular Papers 69.10 (2022): 3901-3914.

[8] Özkan, Bahadır, and Ertan Zencir. "A low-power 65-nm CMOS mixer linearized with IM2 injection for V2X applications." Analog Integrated Circuits and Signal Processing 110.3 (2022): 489-497.

[9] Shetty, Darshan, et al. "Ultra-Low-Power Sub-1 V 29 ppm/° C Voltage Reference and Shared-Resistive Current Reference." IEEE Transactions on Circuits and Systems I: Regular Papers 70.3 (2022): 1030-1042.

[10] Zarkos, Panagiotis, et al. "Fully Integrated Electronic-Photonic Ultrasound Receiver Array for Endoscopic Applications in a Zero-Change 45-nm CMOS-SOI Process." IEEE Journal of Solid-State Circuits (2022).

[11] Panchal, Dipesh, and Amisha Naik. "0.5 V Variable Gain Amplifier Using Dynamic Threshold MOS for Ultra-Low Power Applications." 2022 IEEE Delhi Section Conference (DELCON). IEEE, 2022.

[12] Santos, Suzian Mahéli R., et al. "A Negative Resistance-Based ULV Variable-Gain OTA for Low-Power Applications." IEEE Transactions on Circuits and Systems II: Express Briefs (2023).

[13] Ramakrishna, P., et al. " An Inductor Less Low Power Low Noise Amplifier for Wireless Applications." resmilitaris 13.2 (2023): 5766-5778.

[14] Khan, Zohaib Hasan, Shailendra Kumar, and Deepak Balodi. "A comparative analysis of different types of mixer architecture for modern rf applications." Proceedings of Trends in Electronics and Health Informatics: TEHI 2021. Singapore: Springer Nature Singapore, 2022. 429-440.

[15] Ceolin, Giovana, and Lucas Compassi Severo. "A 0.4 V Active Biased LNA for 2.4 GHz Low Energy RF Receivers." Journal of Integrated Circuits and Systems 17.2 (2022): 1-8.