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Research Article

Advancements in VLSI Technology for Enhanced Signal Processing and Power Management in Electronic Systems

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Abstract— This research investigates the application of Delta-Sigma Modulator controlled switch-mode power supplies to address the challenges associated with conventional PWM-controlled DC-DC Buck Converters. By exploiting the noise-shaping capabilities of Delta-Sigma modulation, in-band tones in the output are mitigated. The study encompasses three phases: initial design and performance evaluation of PWM-controlled converters, transition to Delta-Sigma Modulator control, and refinement of the design to enhance efficiency and noise performance. Notable achievements include reducing inductor values and integrating on-chip capacitors, leading to a peak efficiency of 91% at a 200mhz sampling frequency. Post-layout simulations further validate the superiority of Delta-Sigma Modulator controlled switch-mode power supplies over PWM-controlled counterparts.

Keywords—Output Voltage, Duty Ratio, Load Resistance, Efficiency, Control Voltage of the switches, Ripple Voltage, Input Voltage, FFT, layout, Inductor loss, Additive quantization noise, DDR2-SDRAM, time-to-digital conversion, PVT, FSM and Control Circuit.

I. INTRODUCTION

In the contemporary era of electrical engineering, the quest for energy-efficient and reliable power supply systems is of paramount importance. At the heart of these systems lie DC-DC converters, which play a crucial role in converting electrical power from one voltage level to another while maintaining stability and minimizing noise. Traditional PWM-controlled converters, though widely adopted, suffer from inherent limitations such as output voltage ripple and in-band tones, which degrade performance and reliability. This research endeavors to overcome these challenges by exploring Delta-Sigma Modulator controlled switch-mode power supplies as an alternative approach. By harnessing the noise-shaping capabilities of Delta-Sigma modulation, this study seeks to mitigate noise and improve overall performance. Through a comprehensive three-phase methodology encompassing design, optimization, and evaluation, this research aims to push the boundaries of power supply technologies. The anticipated benefits include enhanced efficiency, reduced noise levels, and improved reliability, thereby meeting the evolving needs of modern electrical systems.

Employing mathematical analysis, our study unveils the significant performance improvements offered by Delta-Sigma Modulator controlled switch-mode power supplies. Operating at a 200mhz sampling frequency, our design achieves a peak efficiency of 91%, outperforming PWM-controlled converters. Through meticulous simulation, we demonstrate a remarkable reduction in noise levels, with in-band tones suppressed by up to 50db at critical harmonic frequencies, highlighting the efficacy and potential of our approach in advancing power supply technologies.

II. EXPERIMENTAL PRINCIPLES

It is primarily determined by the following principles. These are:

A. DC-DC Converter efficiency calculation

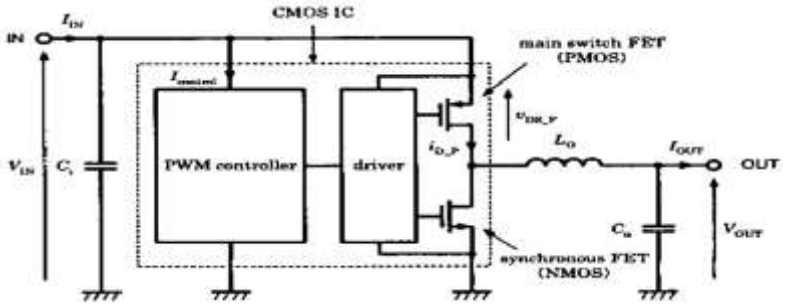


Fig. 1. Circuit diagram of synchronous buck converter using CMOS IC

For determining the efficiency calculation, first we have to enumerate fundamental equations of loss calculation.

1) *Basic equations of loss calculation:*

a) *Inductor loss*:

It can be expressed by equation

$$P_{Ind} = R_{LDC}I_{LDC}^2 + R_{LAC}I_{LAC}^2 \quad (1)$$

Where P_{ind} - Inductor loss

I_{LDC}- Inductor DC current = I_{OUT}

I_{LAC} - Inductor AC current

R_{LDC}- Inductor DC resistance

R_{LAC}- Inductor AC resistance

$$I_{LAC} = \frac{V_{OUT}(1-d)}{2L_o f_{osc}\sqrt{3}} \quad (2)$$

F_{osc}- Switching frequency

V_{OUT} - Converter output voltage

L_o- inductance of the output inductor

D - Duty cycle

$$P_{Ind} = R_{LDC}I_{out}^2 + R_{LAC}\left[\frac{V_{OUT}(1-d)}{2L_o f_{osc}\sqrt{3}}\right]^2 \quad (3)$$

b) Main switch FET loss:

$$P_{MOS\_P} = P_{ON\_P} + P_{SW\_P} + P_{DRV_P} + P_{QDS\_P} \quad (4)$$

c) Synchronous FET loss:

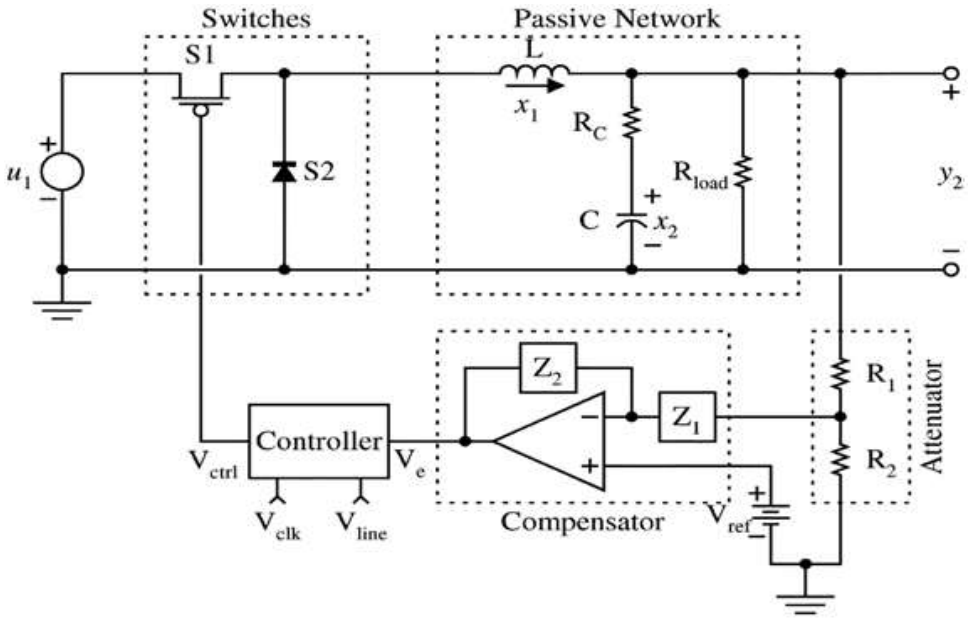
$$P_{MOS\_N} = P_{ON\_N} + P_{SW\_N} + P_{DRV\_N} + P_{QDS\_N} \quad (5)$$

2) *Efficiency:* The efficiency of the converter is expressed as-

$$H = \frac{V_{OUT}I_{OUT}100}{V_{OUT}I_{OUT}+P_{Ind}+P_{MOS_P}+P_{MOS_N}} \quad (6)$$

B. Buck converter & it's feedback control

(a)



(b)

Fig. 2. Typical buck-type SMPS (a) Block diagram. (b) Circuit diagram

C. -dc buck converter

1) *PWM controller:* It can be expressed as

$$S_{V_{Ctrl}^{Ss}} = \frac{F\{V_{Ctrl}^{Ss}\}^2}{Re(Z_{Out})} = (2\pi d)^2 SinC^2(\frac{\Omega dt}{2}) \sum_{N=-\infty}^{\infty} \Delta(\omega - \frac{2*\pi*n}{T}) \quad (7)$$

Where $S_{V_{Ctrl}^{Ss}}$ Is the PSD of V_{Ctrl}^{Ss}.

2) *$\Delta\Sigma$ modulator-based controller:* The output is defined by the following equation

$$Y = XZ^{-2} + N(1 - Z^{-2}) \quad (8)$$

Where X is the input signal and N is the additive quantization noise.

D. Control schemes of dc-dc buck switching converters

- To ensure stable loop response of the switching converters, the usual practice is to design for a gain of at least 6 db and phase margin of at least 45°.Under this condition second order system would have critically damped step response.
- For the system to be stable the unity gain crossover frequency must be half of the switching frequency. This ensures Nyquist Sampling Theory.
- Even the unity gain crossover frequency should be high enough to allow the switching converter to respond quickly to its output transients.
- Having set the unity gain crossover frequency, the gain of the error amplifier is selected to yield a total loop gain of 0 db at unity gain crossover frequency.
- The magnitude response of the error amplifier is designed to cross 0 db at a slope of (-) 20 db/decade with desired gain margin.

Transfer Function of this passive filter

$$\frac{V_o(s)}{V_{in}(s)} = \frac{R}{L*C*R*s^2+s*L+R} \quad (9)$$

Where R_{esr}=0. For PID compensator has 3 poles and 2 zeros. The integration provided by the 3rd pole, located at zero, which is used to minimize the steady state error.

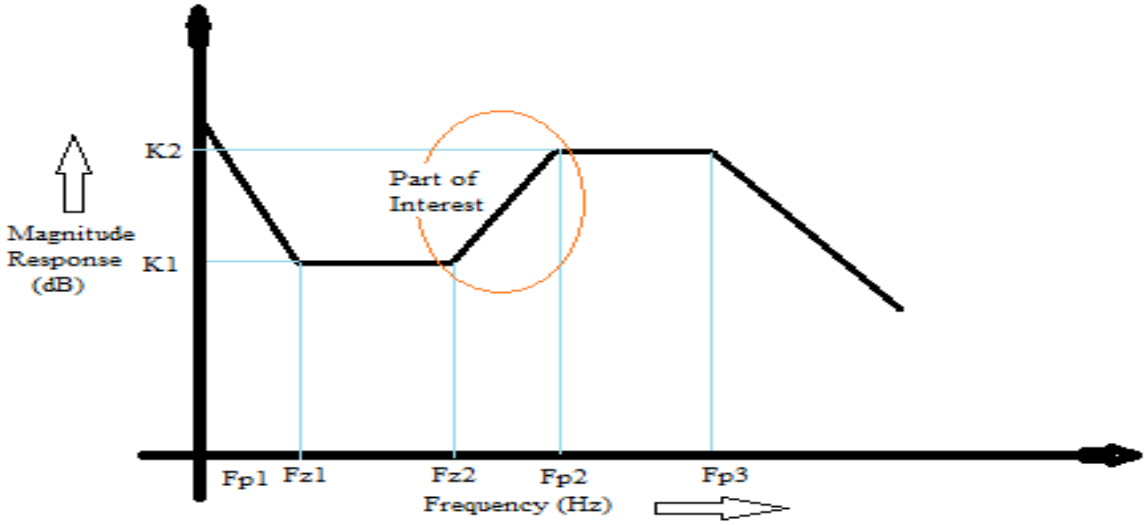


Fig. 3. PID Compensator magnitude plot

➢ ***Importance of Error amplifier compensator:***

It is required because switching converter can be stabilized by adding a compensator network in the error amplifier to increase the phase margin. Transfer function of the output filter:

$$\frac{7.26}{4.4e^{-14}s^2+2e^{-6}+11} \quad (10)$$

III. DESIGN & OPERATION OF SYSTEM

A. Designing of PWM controlled dc-dc buck converter

- Input Voltage: 5V
- Output Voltage: 3.3V
- Required duty cycle is D = 3.3/5 = 0.66 = 66%.
- Operating frequency: 5 mhz
- Load resistor is kept at the value of Rout = 11 Ω
- Output current as 300 ma.

1) Selection of Inductance (L):

Sampling frequency= F_s =5M Hz.

$$\Delta I = \frac{V_{Out}}{L(1-D)T_S} \quad (11)$$

ΔI= peak to peak current ripple in the inductor.

We are operating the converter in continuous mode of operation. Chosen, ΔI=27.2ma.

- The value of L=8.25u H

2) Selection of corner frequency of the output filter (F_c), load capacitance (C_{out}) & effective series capacitance(R_c):

$$\frac{\Delta V_{Out}}{V_{Out}} = \Pi^2(1\text{-}D)\left(\frac{F_C}{F_S}\right)^2 \quad (12)$$

Chosen, ΔV_{out} = 0.136 mv

- The value of F_c=17.5224KHZ

$$F_C = \frac{1}{2\pi\sqrt{LC}} \quad (13)$$

- The value of C_{out}= 10u F
- Effective series resistansce of the capacitor C_{out} is R_c = 0.5 Ω

3) *Design of Attenuator:* The sampling network, R1 and R2, contributes an attenuation according to its sampling ratio R2/(R1+R2).The gain attenuation of the sampling network is 20*log (2.5/3.3) = (-) 2.41db.The chosen value of R1=8K, R2=25K.

1) *Design of compensator:*

Unity gain crossover frequency (F_1) = (1/5th of switching frequency (F_s)) = 20mhz

Transfer function of the output filter:

$$\frac{7.26}{4.4E^{-14}S^2+2E^{-6}+11} \quad (20)$$

. Hence the gain of the error amplifier should be chosen to be (-)(-22.745-2.415)=25.16db.

- R_B/R_A= 1.81

Let, R_A = 1KΩ

- R_B =1.81KΩ

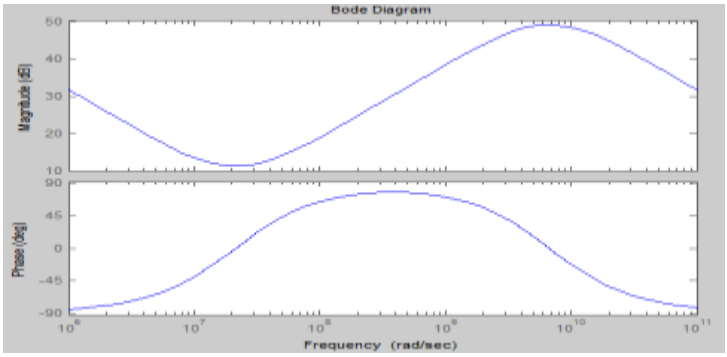


Fig. 7. Gain and Phase plot of PID compensator

Transfer function & bode plot of the compensator

$$\frac{2.187e^{-15}s^2+9.352e^{-8}s+1}{5.666e^{-28}s^3+7.663e^{-18}s^2+2.591e^{-8}s} \quad (21)$$

B. Design of OP-AMP

It is basically design on rail to rail operation.

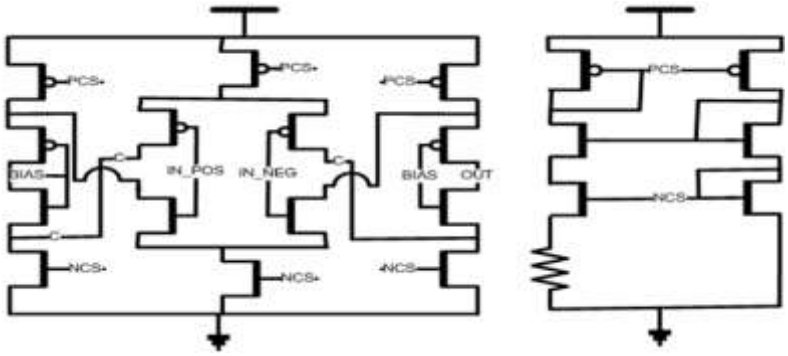


Fig. 8. Op-amp Circuit

C. Design of dynamic comparator

The latched comparators work synchronously with the sclock signal and indicate, through their digital output level, whether its differential input signal is positive or negative. They use a positive feedback mechanism to regenerate the analog input signal into a full scale digital signal (regenerative amplification).

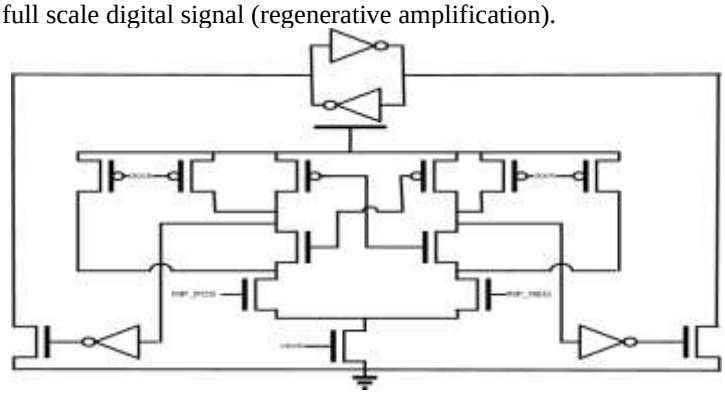


Fig. 9. Dynamic comparator

D. Design of non-overlapping clock generator:

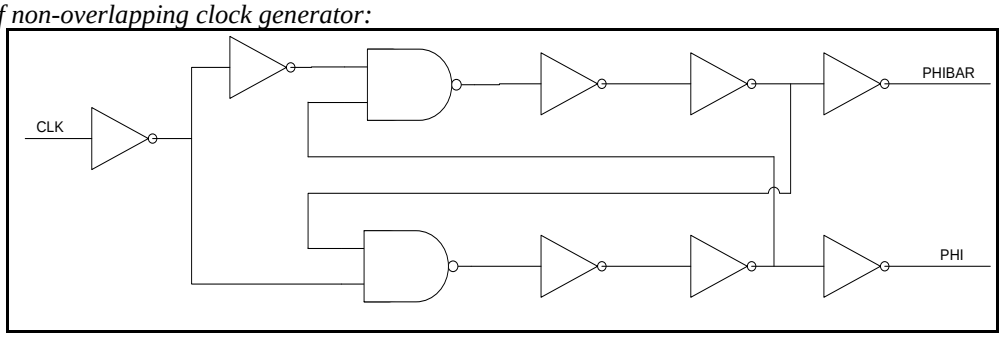


Fig. 10. Non-overlapping clock generator

E. Design of Level Shifter

The circuit combines two approaches: differential logic and positive feedback.

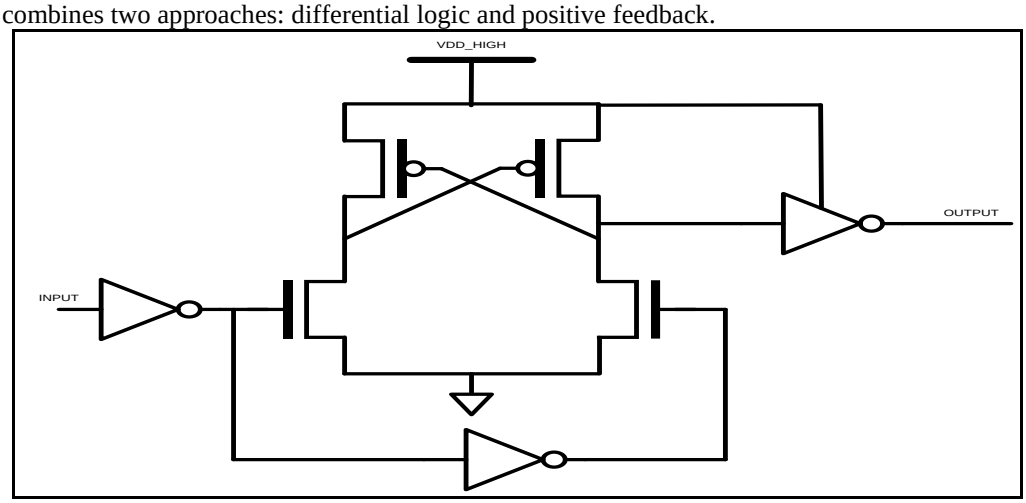


Fig. 11. Level shifter

IV. EXPERIMENTAL RESULTS

A. DC-DC Buck converter

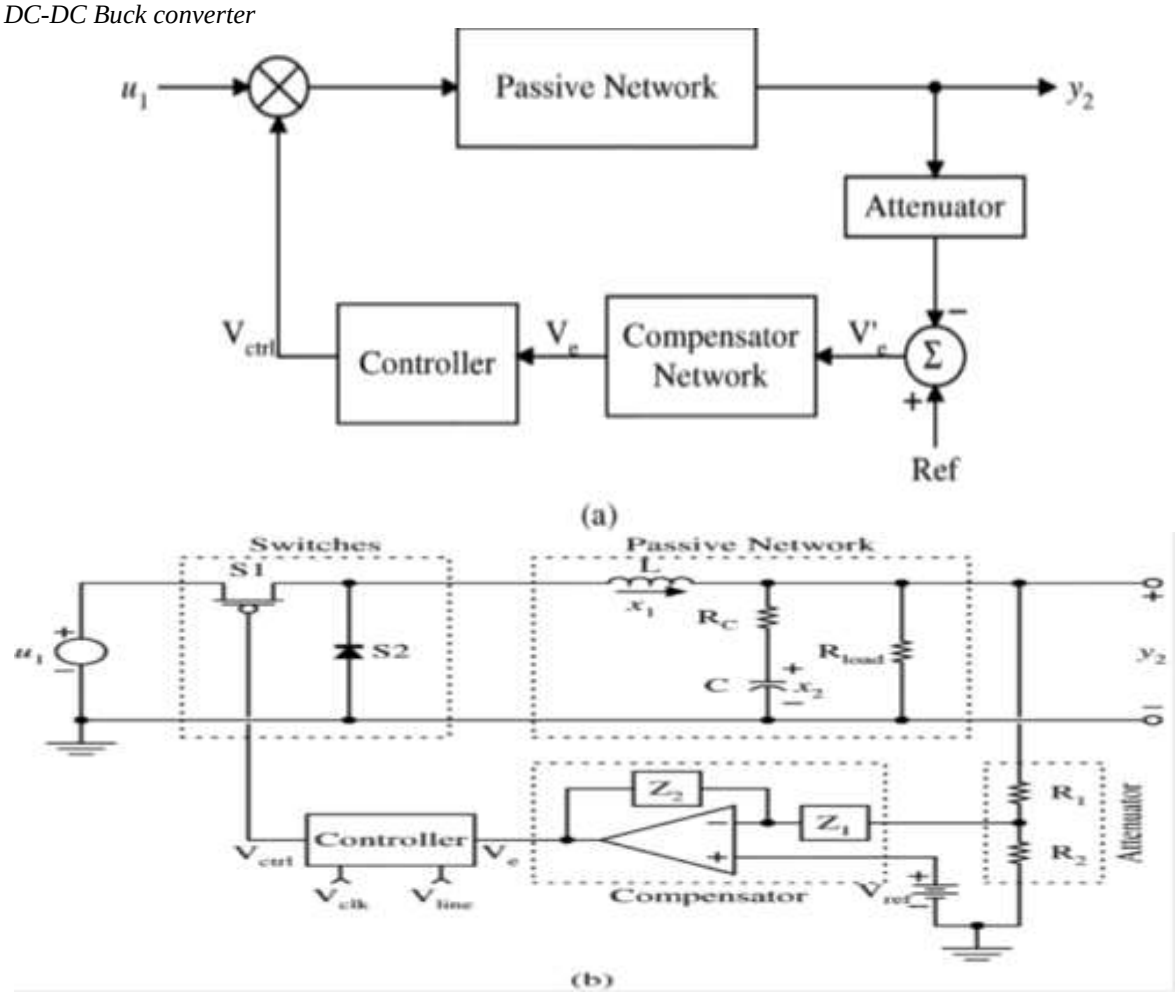


Fig. 15. Typical buck-type SMPS. (a) Block diagram (b) Circuit diagram

1) PWM controller based Dc-Dc Buck Converter:

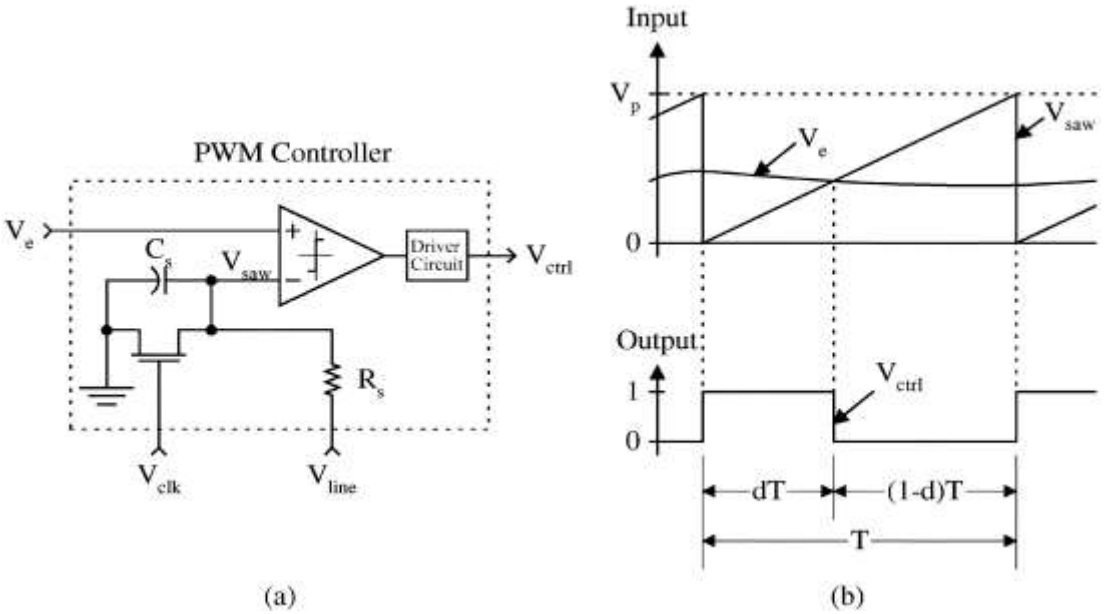


Fig. 16. PWM Controller (a) Circuit diagram (b) Input and output waveforms

- Overshoot: (3.671-3.075) V
- Settling Time: 46.92us
- Ripple at Vout: (3.302-3.295) V
- Efficiency: 79%
- FFT Spectre:

Signal (5mhz): (-) 46.76 db 1st harmonic:(-)57.19db
2nd harmonic: (-) 72.05 db 3rd harmonic:(-)75.23db
4th harmonic: (-) 74.24 db 5th harmonic:(-)82.68db 6th harmonic: (-) 85.98 db 7th harmonic:(-)81.29db 8th harmonic: (-) 85.48 db
9th harmonic: (-) 107.7 db

Fig. 17. FFT Output waveform of PWM controller based DC-DC Buck Converter

2) *Delta-Sigma controller based Dc-Dc Buck converter:*

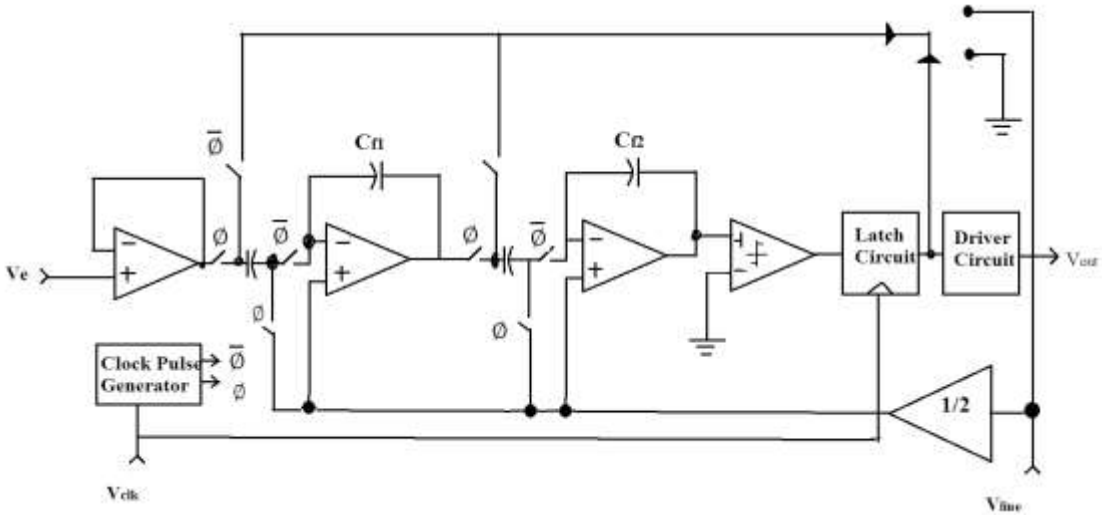


Fig. 18. Switched-capacitor ΔΣ modulator

Fig. 19. Input (Sine wave) and output waveform of the delta sigma modulator

- Input Voltage range = 6V-3.9V
- Output Voltage = 3.3V
- Maximum Output Current = 943 ma
- Ripple Voltage = 6mv

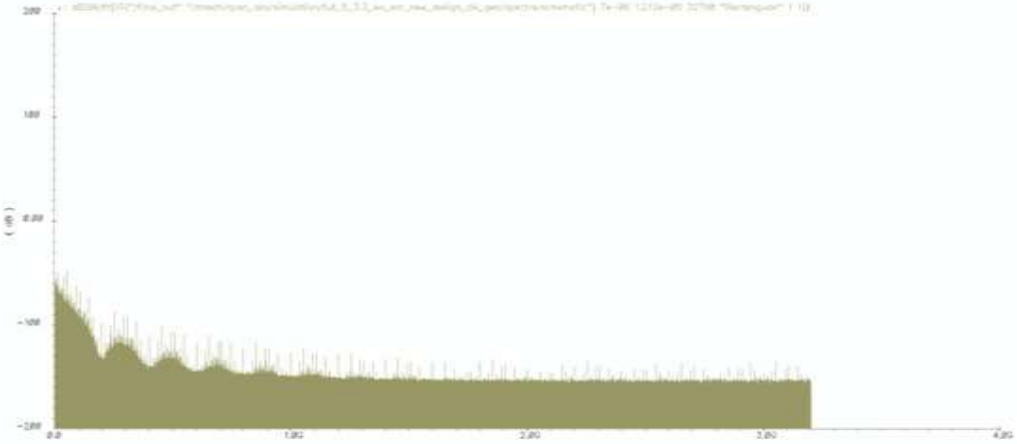


Fig. 20. FFT spectra of the delta-sigma modulator controlled dc-dc buck converter

- Frequency Component Values:
  Signal(200mhz) =(-)98.58 db
  First Harmonic(400 mhz) = (-)110.6 db
  2nd Harmonic(600 mhz) = (-)117.4 db
  3rd Harmonic(800 mhz) = (-)122.7 db

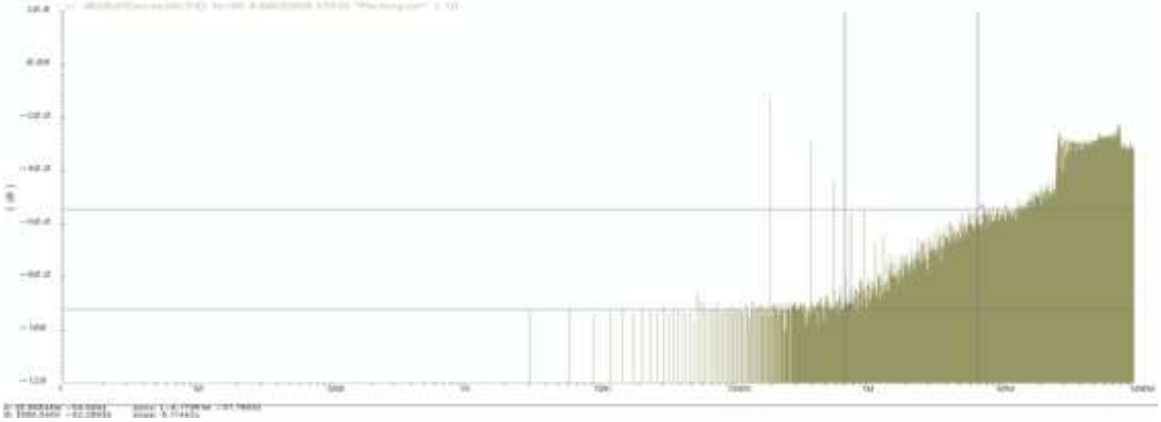


Fig. 21. FFT Plot of Delta-Sigma Modulator

- From the Plot noise shaping is clearly visible because out of band noise is shaped at rate of 40db/decade.
- SNR = 74.87 db

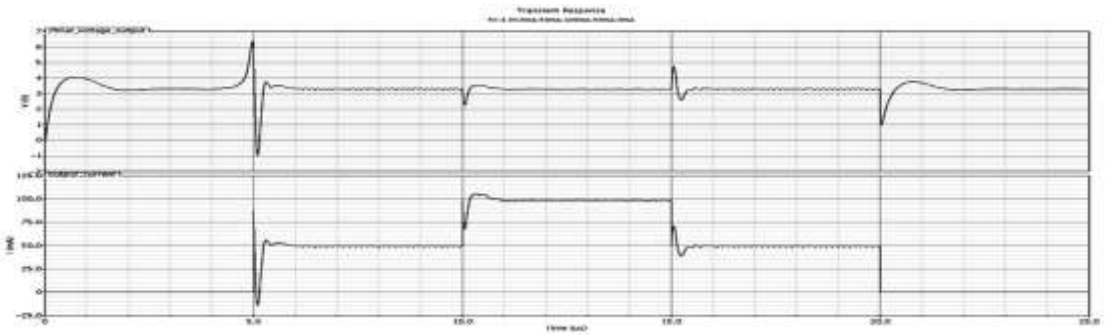


Fig. 22. Output Voltage and Current waveform for sudden switching of current 0ma→50ma→100ma→50ma→0ma for the conversion of 5V-3.3V

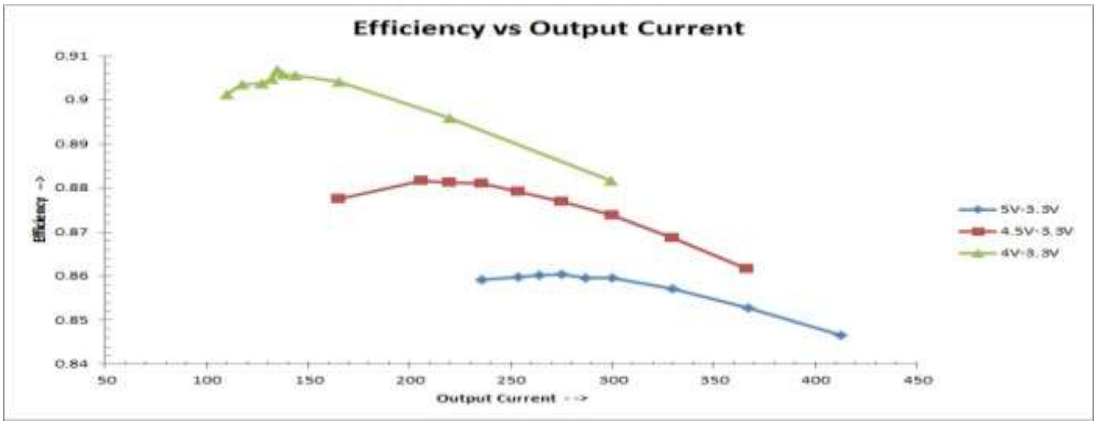


Fig. 23. Comparative Study of Different input (5V,4.5V,4V)

B. Layout

1) Op-amp:

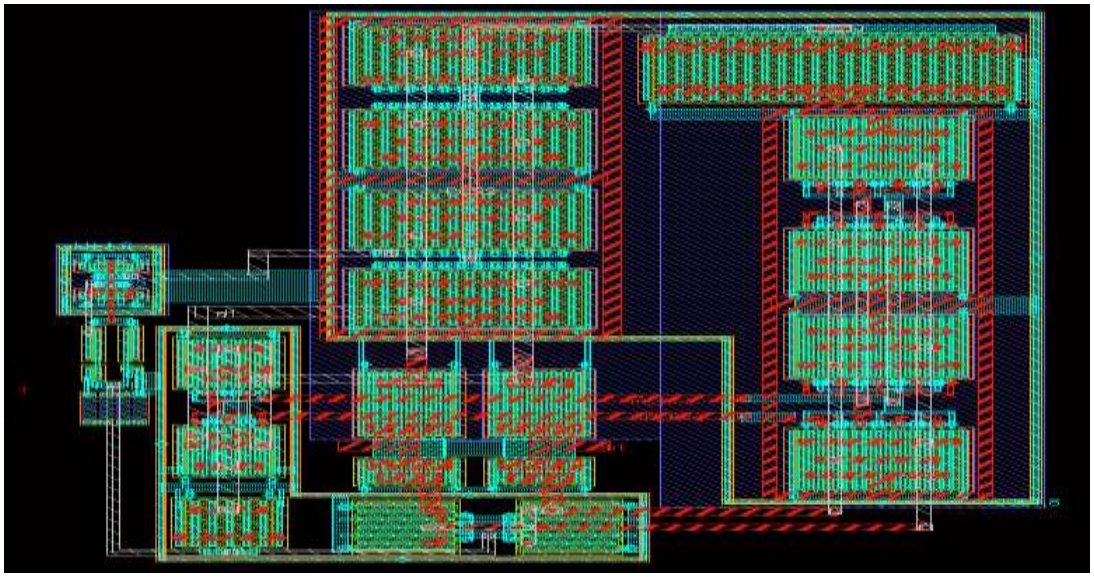


Fig. 24. Op-amp Layout

2) Comparator:

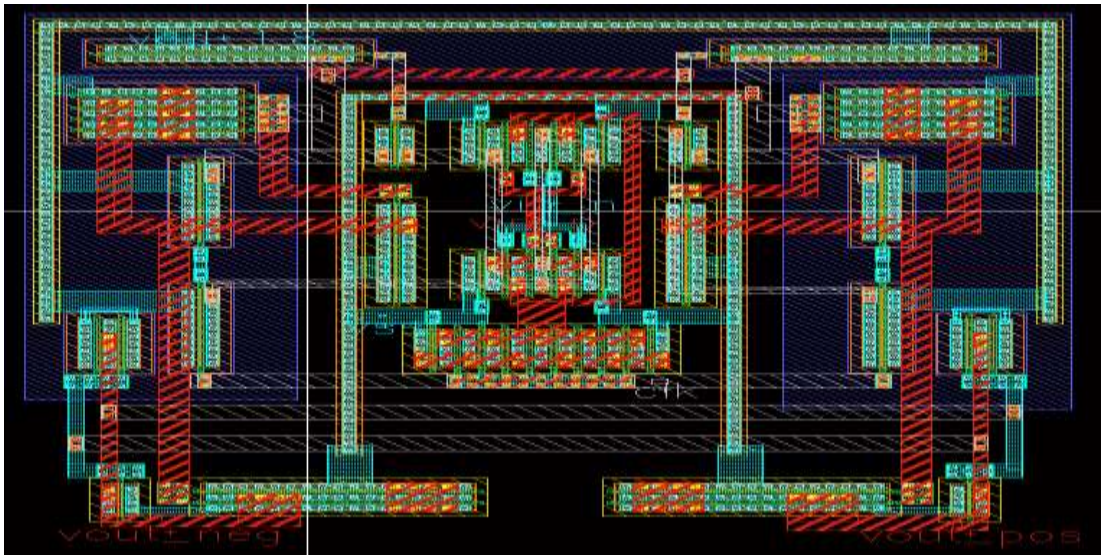


Fig. 25. Comparator Layout

3) Feedback Circuits:

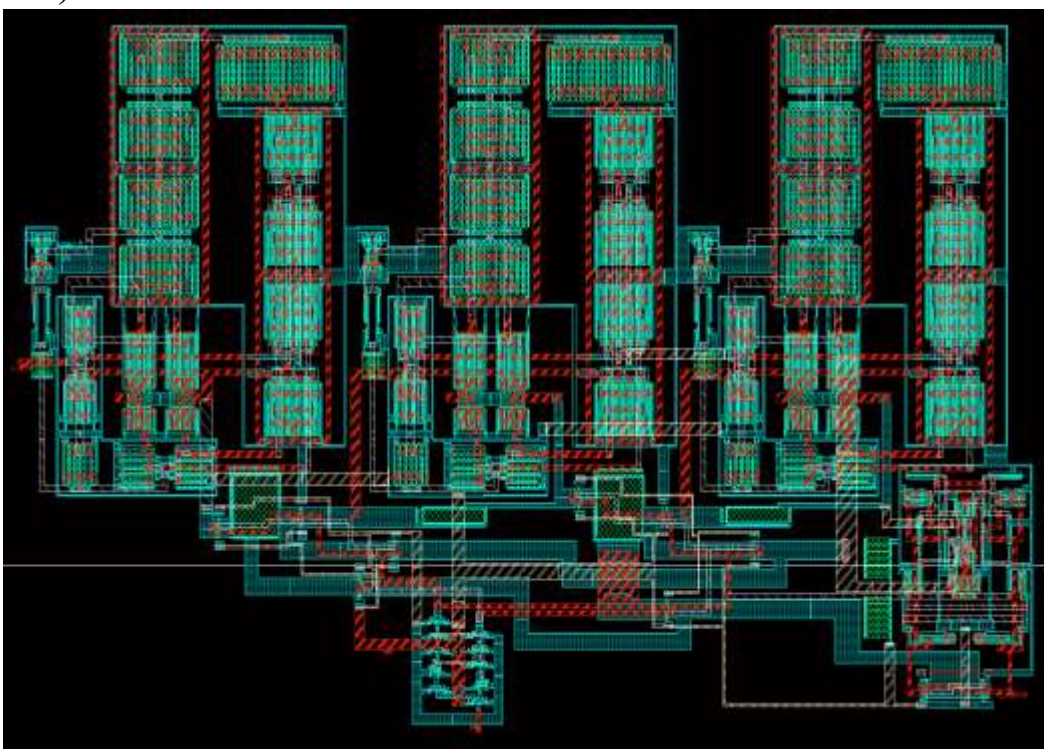


Fig. 26. Delta-Sigma Modulator Layout

4) Attenuator :

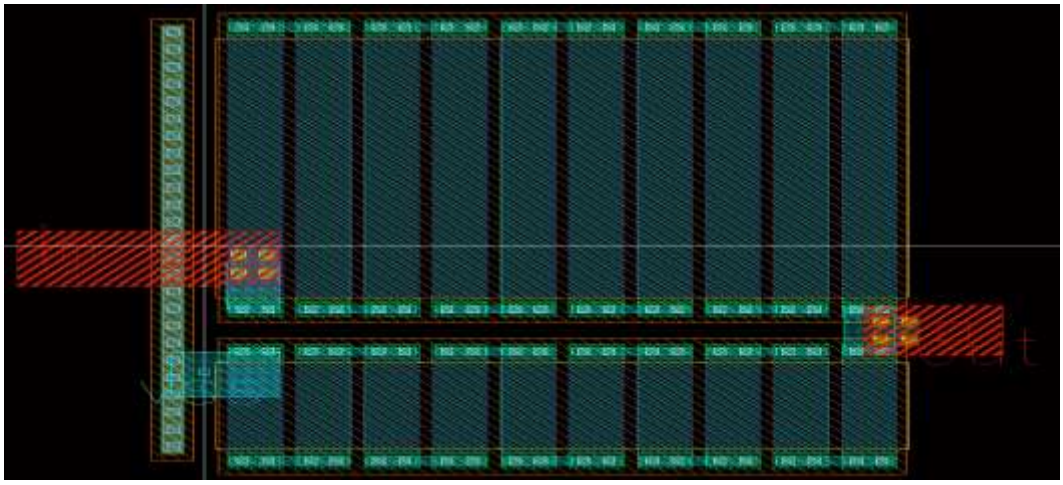


Fig. 27. Attenuator Layout

5) Level Shifter:

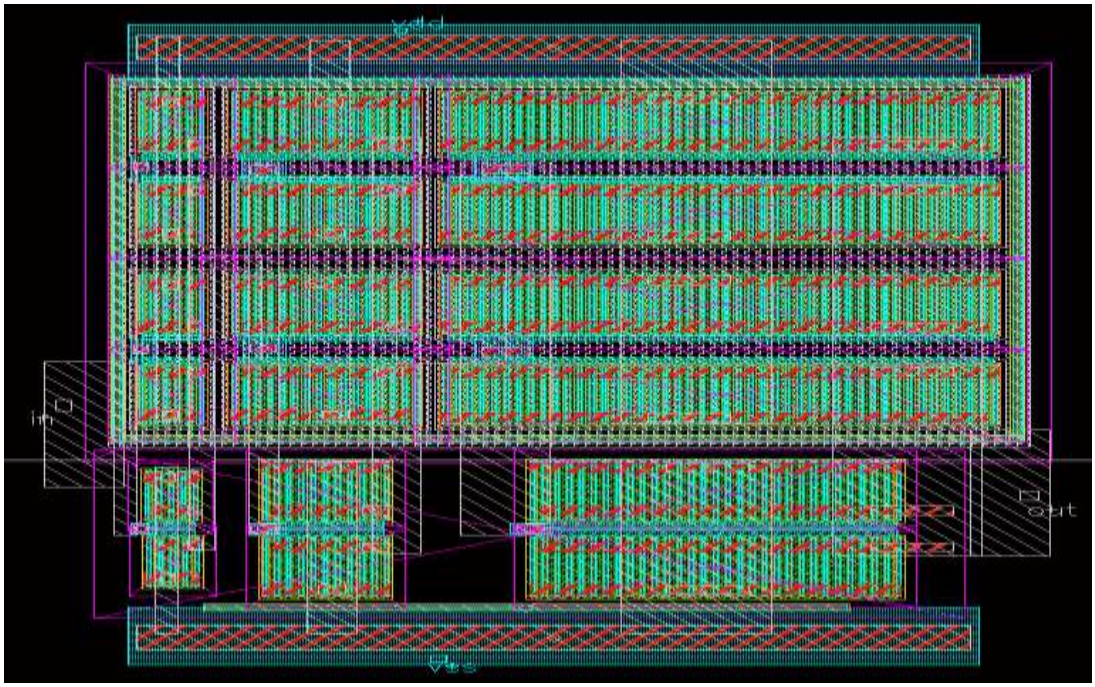


Fig. 28. Level Shifter Layout

6) Full Circuit Layout except Inductor:

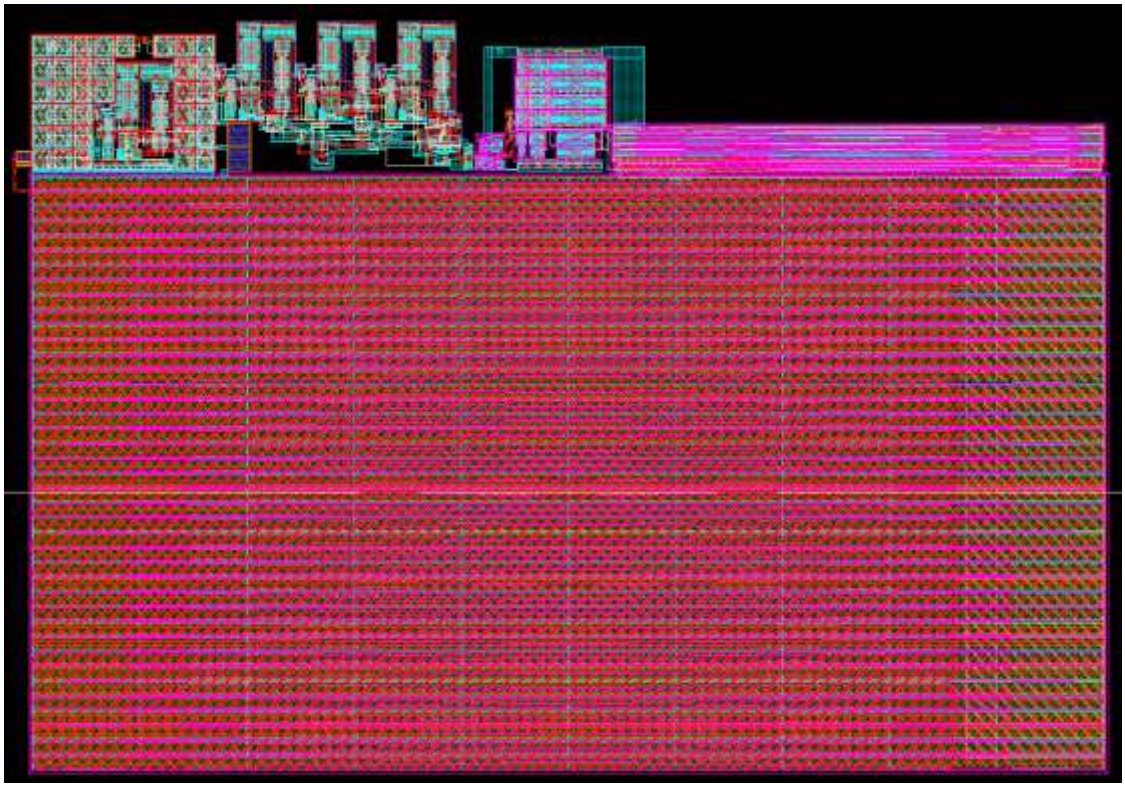


Fig. 29. Layout of the Delta-Sigma modulator controlled DC-DC Buck Converter

C. Layout Verses Schematic Comparison

```
Comparing attenuator_5_3.3 schematic dc_dc_layout vs attenuator_5_3.3 layout dc_dc_layout
Comparing opamp schematic opamp_layout vs opamp layout dc_dc_layout
Comparing pid_compensator schematic dc_dc_layout vs pid_compensator layout dc_dc_layout
Comparing comparator schematic dc_dc_layout vs comparator layout dc_dc_layout
Comparing not_gate schematic dc_dc_wo_esr vs not_gate layout dc_dc_wo_esr
Comparing nand_gate schematic dc_dc_wo_esr vs nand_gate layout dc_dc_wo_esr
Comparing noninverting_clock_generator schematic dc_dc_layout vs noninverting_clock_generator layout dc_dc_layout
Comparing switch_1.8 schematic dc_dc_layout vs switch_1.8 layout dc_dc_layout
Comparing del_sig_modulator schematic dc_dc_layout vs del_sig_modulator layout dc_dc_layout
Comparing level_shifter schematic dc_dc_layout vs level_shifter layout dc_dc_layout
Comparing driver_ckt schematic dc_dc_layout vs driver_ckt layout dc_dc_layout
Comparing feedback_5_3.3_wo_esr schematic dc_dc_layout vs feedback_5_3.3_wo_esr layout dc_dc_layout
Top cell  full_ckt schematic dc_dc_layout vs full_ckt layout dc_dc_layout
Schematic and Layout Match
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Fig. 30. Layout Verses Schematic match report

D. Post Layout Simulation Result

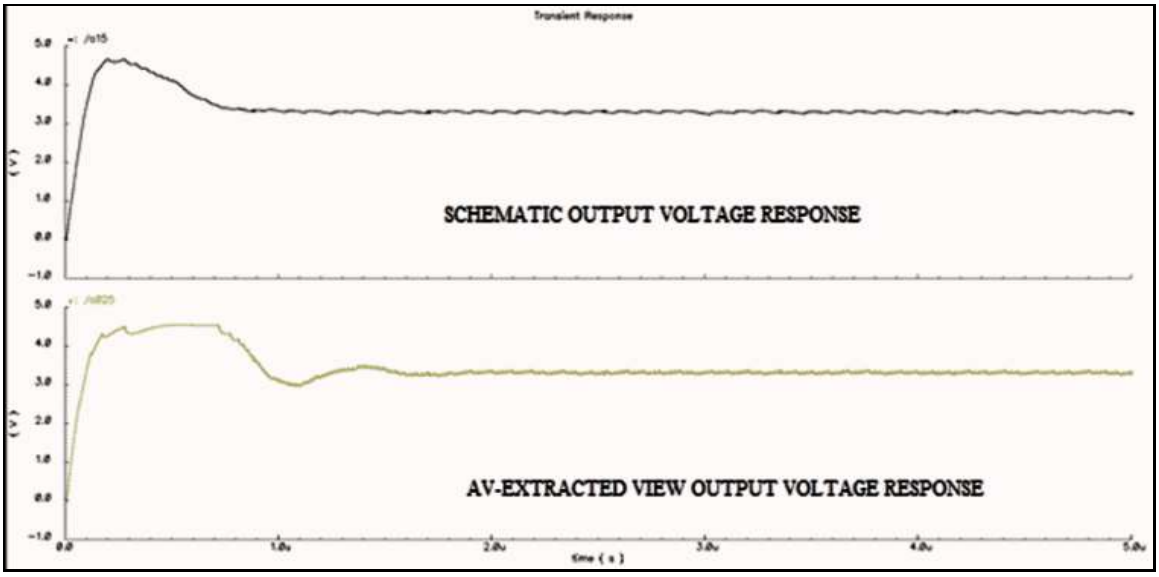

Fig. 31.Output voltage response of schematic &av-extracted view

TABLE 1. Current, Efficiency, Resistance, Ripple Voltage, and Output Voltage for 5V, 4.5V, & 4V input.

Current (ma)	**Efficiency ($\eta * 100\%$)**	**Resist-ance (Ohms)**	**Ripple (mv)**	**Output Voltage (V)**
412.543	0.846651597	8	3.319-3.291	3.300344
366.6203	0.861705703	9	3.313-3.284	3.299583
300	0.85949023	11	3.319-3.287	3.300454
275.0327	0.860514994	12	3.316-3.283	3.300392
253.8473	0.87914178	13	3.334-3.270	3.300015
235.7	0.881029275	14	3.318-3.285	3.3
219.9	0.895986612	15	3.321-3.297	3.298
164.9	0.904104811	20	3.314-3.294	3.298
143.4	0.905553609	23	3.322-3.286	3.299
131.9	0.904662042	25	3.315-3.282	3.298

V. CONCLUSION

In conclusion, our research has elucidated the remarkable potential of Delta-Sigma controlled DC-DC Buck Converters in revolutionizing power supply design paradigms. Through meticulous design and optimization efforts, our converter achieves a peak efficiency of 91% at a switching frequency of 200mhz, outperforming traditional PWM-controlled alternatives. The incorporation of Delta-Sigma modulation and PID compensators ensures superior noise performance and stability across diverse operating conditions. Notably, the compact layout, spanning dimensions of 1mm*0.65mm, underscores the versatility and scalability of our converter for integration into RF and analog applications. With its robust performance characteristics and innovative design approach, our converter heralds a new era of efficiency and reliability in power supply technologies, poised to meet the evolving demands of modern electronic systems.

VI. FUTURE EXTENSION

- All the components except the inductor are on-chip. It can be replaced with switch capacitor circuit having the same functionality.
- Multi-bit Delta-sigma Modulator can be implemented to get better noise shaping in the output.
- Efficiency can be improved by implementing new design for driver, level shifter and other components.

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