

Low Power Circuit Design for Footed Quasi Resistance Scheme In 45NM VLSI Technology

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Abstract: Low power has arisen as a chief topic in these days and hardware enterprises. Power dissipation has become a significant thought as execution and zone of VLSI Chip plan. In this paper, a design of low power for footed quasi resistance scheme in 45nanometer VLSI technology, using appropriate standard digital gates with 45nm technology, considering footed quasi resistance technique for nanoscales is introduced. Transition of logic 1 and 0 is the main problem in the cascading circuits, this problem can solved by employing a basic inverter called as Domino logic at output. Due to the precharge propagation the power dissipation is observed in domino logic, this will be resolved using PDB (Pseudo Dynamic Buffer) model. With the help of PDB nearly 67% of power saved. Even though PDB is succeeded in precharge propagation, it fails in logic transition, this may results erroneous output during cascading. With contracting technology, power utilization can decreased and over all power of the executives on chip are the critical difficulties below 100nm because of expanded intricacy. In this paper execution of low power circuit scheme for footed quasi resistance plot in 45nm VLSI technology. In this paper we will actualize and recreate low power circuit scheme for footed quasi resistance plot in 45nm VLSI technology.

KEY WORDS: 45 nanometer technology, PDB (Psuedo dynamic buffer), GaN on Si pin diodes, Footed Quasi Resistance.

Introduction

Low power and high speed logic circuits are attaining more attention than any device taking in consideration. Since for delay and optimized power, several logic families are designed [1]. The main aim of these logic circuits is to reduce delay, speed of operation and to decrease the power dissipation. In present scenario, the major role played by Dynamic logic circuits, these are used in the circuit to decrease the power dissipation.

In comparison with static CMOS, the area occupied by Dynamic circuit is less [2]. These logic circuits can designed with nearly half of transistors used in designing of static CMOS circuits. Total Power dissipated in a CMOS circuit is amount of dynamic power, impede and static or spillage power. The methods which are used to decrease power scattering are not the restriction to dynamic power. This section discuss about circuit and logic configuration ways to deal with limit dynamic, spillage and short out power dissemination. In order to prevent the erroneous output during the design of cascade dynamic circuits, the logic circuits of Domino are modified as dynamic logic at output along with extended simple inverter of static CMOS. To control operations of domino logic, a clock signal is used same as in dynamic circuits.

The operations of a Domino logic circuit are divided into mainly two phases. The first phase is called as precharge phase, if clock is at low, V_{DD} at the output of the parasitic capacitance charges it, that was present before a simple static inverter. This results makes output domino logic circuit as 0 logic and in evolution stage, that is at second stage if the clock high, the capacitance of load will maintain or discharge as per the input. In precharge phase a domino logic circuit uses extra inverter to prevent the logic 0, and logic 1 transitions in evaluation phase, this means at capacitance of output inverter in first phase i.e., pre-charge phase, charging as well as discharging can takes place, if its converse evolution phase has logic 0 as output. This may be cause a significant wastage of power. This problem solved by many methods, in which efficient method is PDB, it saves upto 67% of power.

The exacting impediment on power dissemination in convenient hardware applications, for example, PDAs and tablet PCs must be met by the VLSI chip originator while as yet meeting the computational necessities. While remote gadgets are quickly advancing toward the shopper hardware market, a key plan imperative for compact activity specifically the total power utilization of the gadget must be tended to. Diminishing the total power utilization in such frameworks is significant since it is alluring to augment the run time with least necessities on size, battery life and weight distributed to batteries.

So the main factor to consider while planning SoC for convenient gadgets is 'low power scheme' [4]. The developing business sector of portables, for example, phones, gaming consoles and battery-powered electronic frameworks requests microelectronic circuit's plan with super low power scattering, therefore VLSI technology came into scenario. As the incorporation, size, and unpredictability of the chips keep on expanding, the trouble in giving satisfactory cooling may either add critical expense or cutoff the usefulness of the figuring frameworks which utilize those integrated circuits. Thus, the VLSI technology is used in proposed system based on 45nm technology to overcome power dissipation [5].

II. PSUEDO DYNAMIC BUFFER

a pseudo dynamic buffer method is able to eliminate the pre-charge pulse propagation. Here, in this section different types of domino logics are explained, it's because domino logic circuits plays major role in power dissipation in integrated circuits. This circuit helps in reduction of precharge propagation.

2.1 Conventional Domino Logic Circuit

Designing of a conventional domino logic can be done by using two N type (pull down) and P type (pull up) networks. A simple dynamic logic circuit is as same as a conventional domino logic which designed with a simple buffer of N type network, which operates in two phases, as discussed earlier they are precharge phase and evaluation phase. Clock signal distinguishes these two phases. If clock signal is at low, the PMOS transistor at output charges the capacitance node to V_{DD} is known as precharge phase. If clock signal is at high (one), the NMOS transistor at output is high and node x voltage depends on N type networks input, and this is known as evaluation mode [6]. Moreover, if signal (input) is high (1), thus the node voltages are given to both precharge and evaluation phases. The voltage at V_{DD} is charged during evolution phase and discharged during pre charge phase which leads to pre charge propagation, which results in higher power consumption at output buffer. This precharge pulse propagation issolved by using different techniques like truesingle phase clk model and pseudo dynamic buffer.

2.2 Psuedo Dynamic Buffer Domino Logic

In PDB model source of transistor Q_s in output inverter is connected to node Y instead of ground as shown in figure (1). For this particular model when input A is logic 1, evaluation and precharge will lead to following case. During evaluation phase, node X will discharge to logic 0 which makes PMOS transistor Q_4 ON and output capacitance charge to V_{DD} . In precharge mode, output node X charges to V_{DD} as of node Y which makes NMOS transistor Q_s OFF. Transistor Q_s operates as following. In precharge mode previously source of Q_s is connected to ground, logic high at node X turns ON transistor Q_s because $V_g - V_s (V_{gs})$ is greater than threshold voltage (V_{th}) in PDB source of transistor Q_s is connected to node Y which makes Q_s operation depends on node X only in precharge mode by virtue of when clk signal is low transistor Q_3 turns ON makes source of transistor Q_s connected to ground as in domino logic circuits.

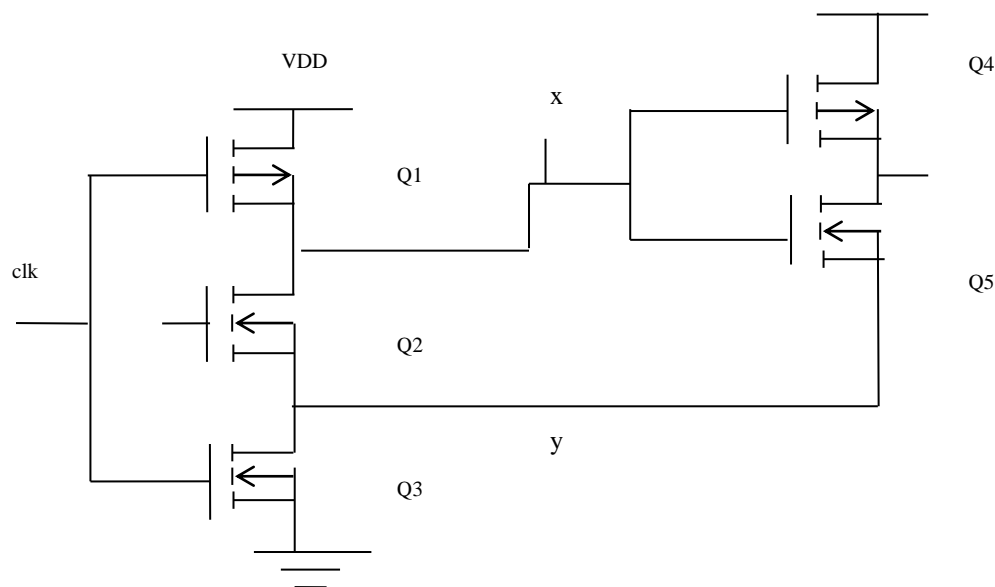


Fig. 1: Psuedo Dynamic Buffer Domino Logic

But when clk signal is high, transistor Q_s operation depends on both voltage at node X and input logic applied for domino logic circuit. But in PDB model there is small problem when logic 0 is applied as input after logic 1 in evaluation state. This is because output parasitic capacitance charge accumulated in evaluation state when input A is logic 1 doesn't have discharge path in precharge state when input A is logic 0. Because of this, logic 1 to logic 0 transition which is not a suitable input for dynamic logic circuits.

2.3 Fault Output in Cascaded Circuits

After overcoming precharge pulse propagation PDB circuit catch on major problem: straightforward perusal of pseudo dynamic buffer logic to design more complex boolean functions gets faulty output logic [7-8]. The issue is best exemplified with the two cascaded pull down n-type pseudo dynamic buffer circuits in reducing of power consumption. Figure (2) shows the circuit of fault output in cascaded circuits this eliminates cascading problem. During the precharge phase (i.e., precharge phase after logic high in evaluation phase), the outputs of

both buffers are already charged to V_{DD} . Consider that the primary input signal A makes a logic 1 to logic 0 transition. On the rising verge of the clk signal, output 01 starts to discharge.

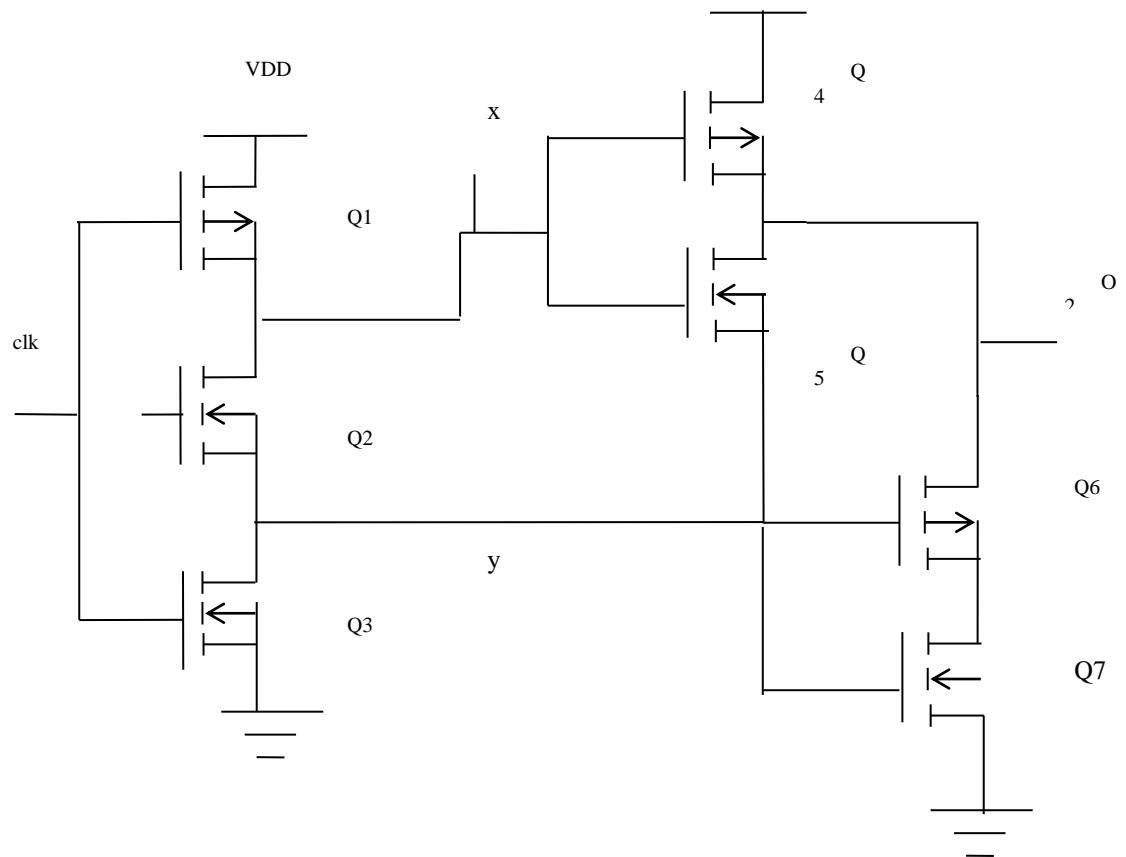


Fig. 2: Fault Output in Cascaded Circuits

The final output O should be logic low as its expected input is logic low. Despite, there is a small propagation delay for the input to discharge O1 to logic low. Therefore, the precharged voltage at node Z gets discharged. By O1 crossing the threshold of the transistor Q7 node voltage at Z gets discharged through Q7 and Q6. This makes final output as logic high, correct logic level can't be retrieved because PDB relies on parasitic capacitance voltage. This leads to erroneous output logic in cascaded PDB logic circuits. Therefore this problem of capacitance and high output is reduced by employing GaN on Si pin diodes of vertical quasi and FQR technique. The proposed system can recreate the low power plan for quasi foot resistance in 45 nm technology [9-10].

III. FOOTEDQUASIRESCISTANCESHEME

To implement low power circuit for footed quasi resistance the main scheme is used is FQR explained in this section along with layout of proposed system.

3.1 Footed Quasi Resistance (FQR) model

The foregoing section illustrates the issue of cascading problem due to logic 1 to logic 0 transition at output node. Suggested footed quasi resistance model overcomes this cascading issue using structure. In proposed circuit used depletion PMOS and NMOS, which are driven by same input node Y. when logic 1 is at node Y depletion PMOS is OFF which makes quasi resistance acting as open circuit, same in case of logic 0 at node Y but this time depletion NMOS is OFF which results same. When input A is logic 1 in precharge phase node Y is connected to V_{DD} and in evaluation phase it is connected to ground which makes footed quasiresistance works as PDB only. When input A is logic 0 the footed quasi resistance functionality in evaluation and precharge phase is: During precharge phase transistor Q2 and Q3 are OFF which will lead node Y as open circuit. Because we use depletion NMOS and PMOS in FQR which provides path to discharge output parasitic capacitance. During evaluation phase NMOS transistor Q3 is ON and NMOS transistor Q5 ON which makes output node logic 0. In output voltage waveform is given where logic 1 to logic 0 transition is removed and is explained in figure(2). Here the proposed layout of low power quasi resistance is given in figure (3).

3.2 GaN- on -Si pin diodes

In comparison with the pin diodes which are grown GaN, diodes which are grown on large area on Si substrate are considered as the enablers those can minimize the cost of using large scale inexpensive Si. These have major advantage over the Si CMOS manufacturing compatibility. In order to date both vertical diodes of quasi which are grown on Si substrate and fully vertical diodes those are grown on GaN are transferred to Si(100) thin films.

After Mesa etching followed by metallization process, the diodes of vertical quasi both anode and cathode are formed side by side on epilayer's same side. The degradation of performance of devices are due to non uniform distribution of crowding effect of currents and electrical field under power operation. Due to this, long term reliability also decreases. In order to overcome this problem, fully vertical PIN diodes are fabricated on Si through bonding of metal.

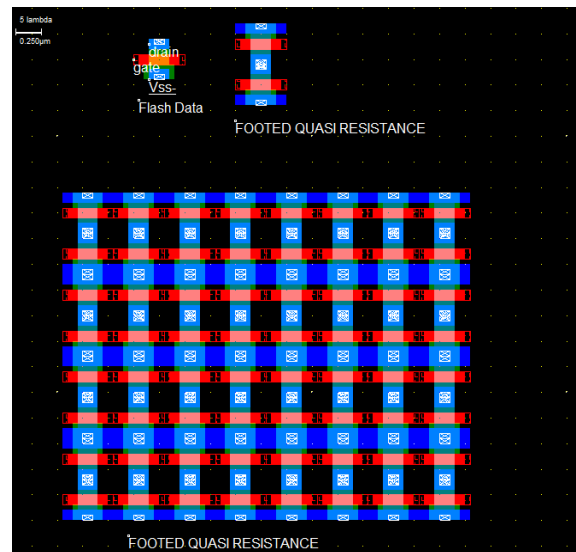


Fig. 3: Proposed layout of quasi resistance

There was far gap between theoretical and practical limits in the characteristics of devices. So there is a lot to improve the fully vertical PIN diodes because of its most complicated process. An efficient technology thus required and comprehensive knowledge about both quasi vertical and fully vertical pin diodes configurations are highly desired in the process of developing of a low power circuit for quasi resistance. Power utilization in the versatile frameworks is also low. Power utilization is one of the significant components of VLSI circuit plan for CMOS, is the essential technology. The power utilization has become a key issue in VLSI circuit plan. The architects are needed to pick suitable strategies that fulfill the application and item needs. Lessening power dissemination changes from application to application.

This proposed system is designed by using 45nm parameters of process technology; at low powers this may offer in turn high speed performance. The main innovation that related to the VLSI 45nm technology is like high-k gate oxide, and very low-k interconnect dielectric and metal-gate are described. Trends, chip fabrication, process design VLSI Technology includes, circuit design and real circuit parameters, electrical characteristics, building blocks of configuration, switching circuitry, CAD, silicon translation CAD, layout design practical experience are included in the process of VLSI technology.

The integration process, gates and diodes used in 45nm technology will help the in reduction of total heat dissipation. The power dispersal of a chip depends on its technology as well as on its execution for example on size, circuit style, working frequency, etc. Due to this technology patterns, transistor spillage power has expanded dramatically supply voltage scaling builds sub-limit spillage current, builds spillage power and represent various spillage in the VLSI plan. Hence static power has become a huge segment of the total power utilization. There are few VLSI procedures to lessen spillage power. Various procedures give a productive method to diminish spillage power, however hindrances limit the utilization of every strategy.

IV. RESULTS

Low power circuit for footed quasi resistance is proposed and designed. The first step in fabrication of circuit in 45nm VLSI technology is isolation of SiO₂. It is shown in figure (4).



Fig. 4: SiO₂ isolation layout

Second step is fabricating polysilicon on isolation layout is shown in figure (5).

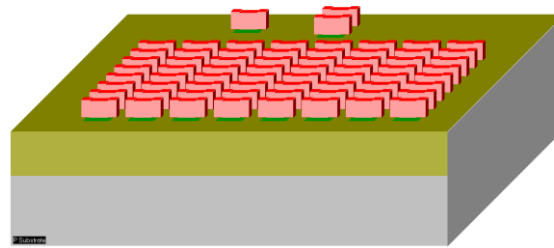


Fig. 5:Polysilicon layout

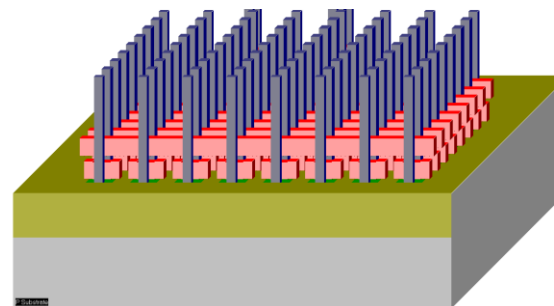


Fig. 6:Final layout

Final layout of the proposed system is shown in figure (6).

V. CONCLUSION

Along with elimination of precharge propagation problem, PDB encounters a new problem of cascading logic. In this proposed footed quasi resistance scheme which solves problem of cascading. 57% of power saved in FQR technique. The digital gates and GaN on Si Pin diode helps in reducing the resistance due to this less heat dissipation was occurred that leads to maximum throughput which in turn produces highly optimized circuits for footed quasi resistance in 45nm VLSI design. But this process can compromise the power saving. This is worthwhile than PBD when considering our proposed system. By reducing power dissipation in circuit, makes a low power circuit for footed resistance. The proposed design of low power circuit for quasi resistance is designed.

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