Research Article

BCD ADDER ENTERPRISE EXHAUSTING NOVEL REVERSIBLE LOGIC FOR STUMPY POWER APPLICATIONS

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ABSTRACT

Reversible logic has garnered tremendous attention in the recent years owing to its capacity to lower the power dissipation which is the major criterion in low power digital design. It finds use in many fields, including nanotechnology, biotechnology, quantum computing, optical information processing, DNA computing, and advanced computing. This work introduces a novel reversible gate and uses it to create an improved reversible BCD adder. The suggested architecture is shown to be more efficient than current ones in terms of gate count, garbage output count, and quantum cost, according to a comparison result.

INTRODUCTION

Because of its relevance to so many different kinds of technology design implementations, reversible logic is a fascinating field that deserves further attention. It's one of the methods being considered for use in nanoscale engineering, where cutting power consumption is a top priority. Heat dissipation is a crucial concern for both designers and end users due to the nature of present technology. When introducing a novel design, for instance a mobile phone, the designer may make use of a voltage or temperature range that is too narrow or too wide for the device's intended application. Reduced power dissipation and thus no heat are the primary benefits of any reversible-logic system. The loss of energy per bit of information, as calculated by using irreversible logic, is kTln2 joules, where T is the absolute temperature and k is the Boltzmann constant.1 Such energy wasted would not occur if the operation employs reversible technique.2 This is due to the fact that the number of bits lost during a calculation is proportional to the quantity of energy lost. Because the reversible computation is carried out by means of reversible gates, no energy is wasted by any piece of information when applying the reversible computation.3,4 Reversible gate designs have been shown to have a minimal power benefit over their CMOS logic counter equivalents, despite their enormous size. Number of gates utilised for the design with less unused outputs, sometimes called trash outputs, is one of the main measurement criteria for reversible-gate logic design. The optimised layout also took into account the fewest possible inputs, all of which were kept constant. Since garbage collection of at least a single digit causes exhaustive and unnecessary execution of the circuit, reducing the number of unused outputs is a significant design feature for reversible logic. Hence, a very significant design component of reversible logic is to employ smaller amount of trash bits. Using a high number of gates in the circuit design is one design component behind lowering trash outputs. The trash count in the synthesis process is lowest for dynamic programming. Toffoli-Fredkin reversible gates provide a low-noise circuit. The usage of "don't cares" switches also reduces waste to a minimum. Reversible logic may be used in quantum technologies. Here we see reversible logic applied in a hidden but potentially distinguishable fashion in a sophisticated antenna simulation architecture. However, the relevance of simulation exposes the reversible modification in the process of propagating a wave.

METHODS AND SUPPLIES

In this work, we provide two implementations of the BCD adder. The necessary algorithmic processes are shown in Figure 1 as a flowchart, with the primary use of conventional logic gates and the same with reversible logic Gates.

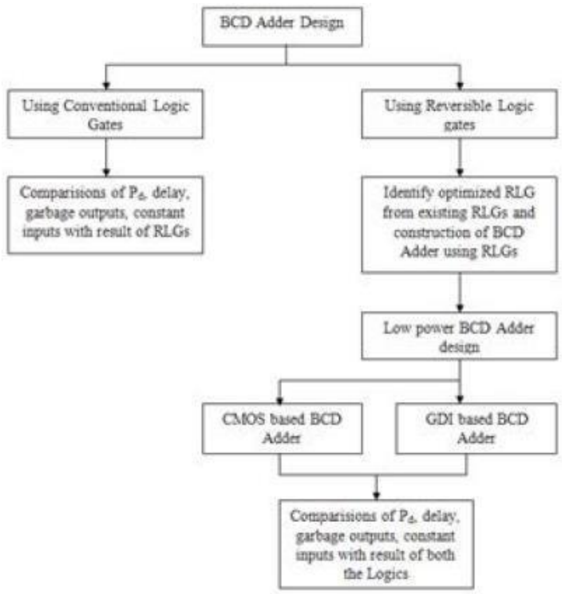
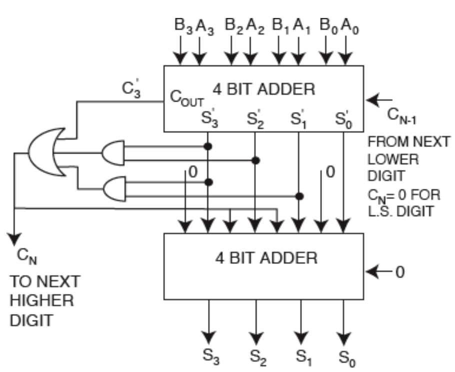


Figure 1. Flowchart.

TRADITIONAL BCD ADDER

Figure 2 depicts how logic gates are used to create the classic BCD adder. It employs OR and AND Gates in its two 4-bit adders and 1-bit correction circuitry.



- ADD **0110** WHEN **C_N=1**
- ADD **0000** WHEN **C_N=0**

Figure 2. Conventional BCD Adder

DESIGN OF BCD ADDER USING RLG

Reversible Logic Gates (RLG) is distinguished depending on their complexity and input/output connection. There are elementary RLGs available with sizes ranging from 2x2 to 5x5. In order to construct a BCD adder, the suggested work took into account three different RLGs: HNG, TSG, and BBCDC.FIVE HONGGATE

Input and output combinations for an HNG (Hybrid New Gate) are determined by four independent factors, as illustrated in Figure 3. The ideal use of this gate is in a ripple carry adder, which uses just a single gate but generates both a sum and a carry as output.

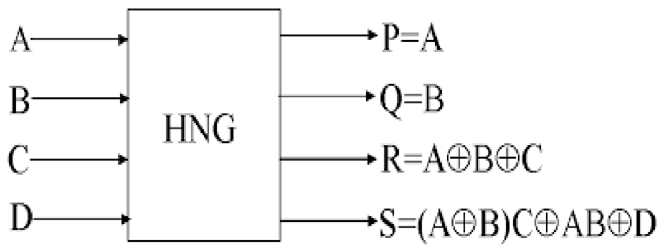


Figure 3. HNG 4x4 Gate.

TSG GATE

Full adder TSG gate implementation is shown in Figure 4.By setting input C to zero, the circuit operates as a complete adder, with the result appearing at output R and the carry appearing at output S.

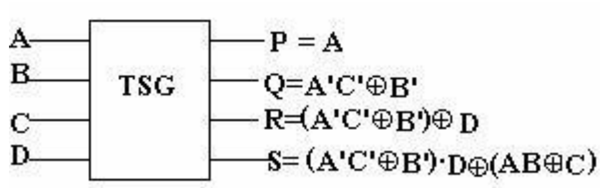


Figure 4. Gate TSG 4x4.

TURNAROUND AT THE BBCDC GATE

The construction of a BCD adder makes use of a BBCDC (Binary to BCD conversion), a 5X5 reversible gate seen in Figure 5.9 The associated input and output vectors are tabulated in Table 1. Figure 6 depicts the design of a BCD adder built using reversible BBCDC gates, which calls for a total of nine inputs (A0-3, B0-3, C0-3, D0-3, and E0-3) and five outputs (four bits for sum bits S0, S1, S2, S3, and Cout.5-17). The augends' encoding into the remaining six bits, plus the circuit carry bit, results in a total of nine bits for the input.

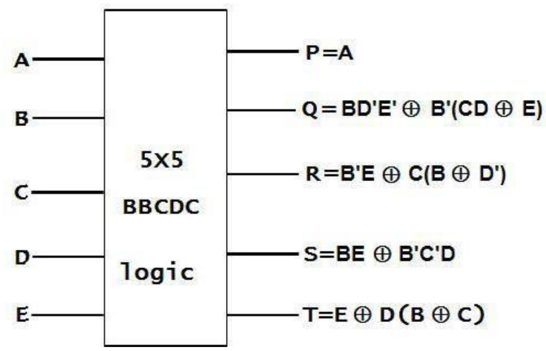


Figure 5. BBCDC 5x5 Gate.

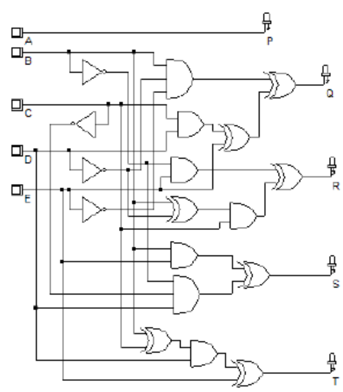


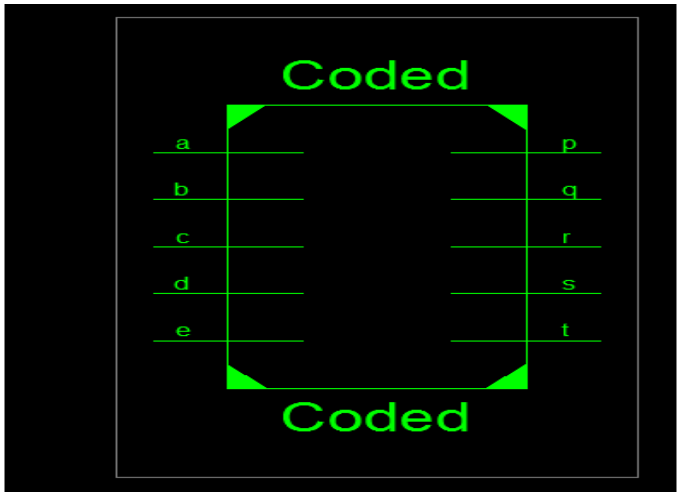
Figure 6. BBCDC 5x5 Gate.

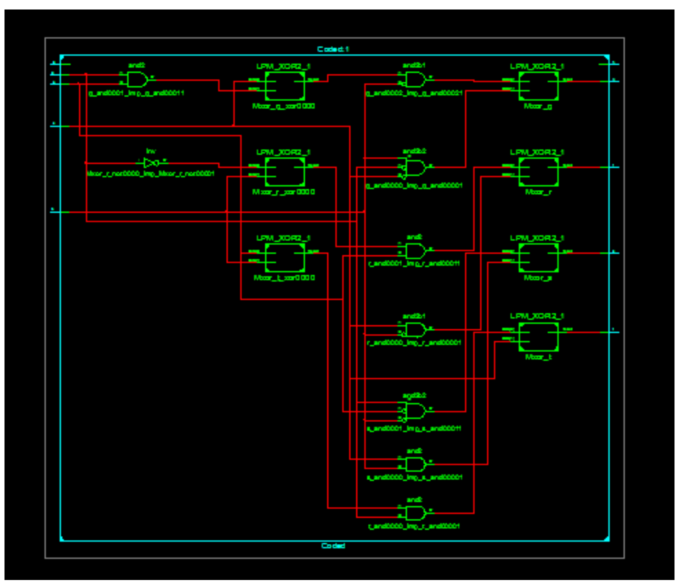
Table 1. Truth table of BBCDC Gate

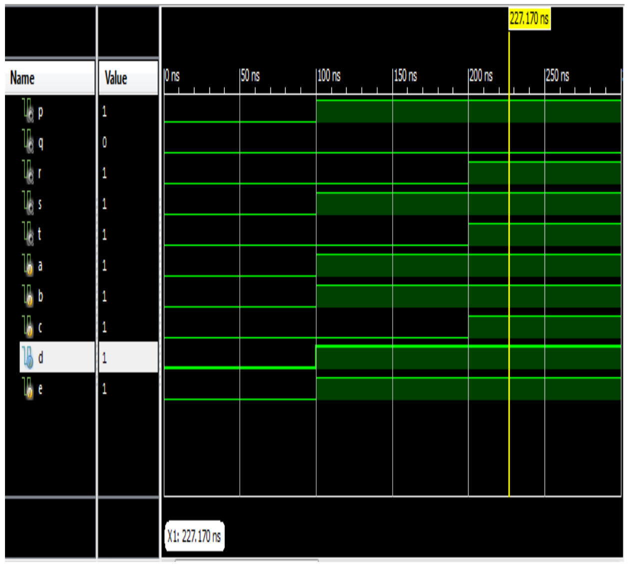
Inputs					Outputs				
E	D	C	B	A	T	S	R	Q	P
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1

To illustrate, in decimal, adding 9 and 9 together yields 19, whereas in straight binary, the result should be 100112, which is not a valid number in BCD. In BCD, the four bits of binary only represent the decimal digits 0 through 9. The binary and BCD representations of the decimal numerals 0 through 19 are shown in Table1.

SIMULATION RESULTS







CONCLUSION

The BBCDC reversible logic was used to construct a low power BCD adder. Multiple BCD adder logic architectures are evaluated with respect to a variety of criteria, including the number of unused outputs, the number of constant inputs, the latency, the area, the number of gates required, the power, and the PDP.

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