A NOVEL DESIGN OF FLIPFLOP CIRCUITS USING QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT

As the chip area is reducing every day the usual transistor model CMOS method suffers with heavy problems because of channel properties such as very low lean gate oxides, increased channel effects, induced drain leakage currents and high power consumption at nano tech standards. Quantum-Dot-Cellular-Automata (QCA) is an advanced technology implemented at quantum levels, it gives an entirely special implementation proposal to develop every integrated circuit based applications utilizing four quantum holes combined in forbidden shell to successfully progress and transmit data at nano tech standards as an opponent of conventional CMOS methodology. In this article, various sequential circuits are designed such as D-FLIP FLOP (FF), T-FF, SR-FF, JK-FF, Shift registers and universal counters. The implementation and simulation results developed using Xilinx ISE simulation tool and results shows that the proposed designs provides the enhanced results compared to the conventional approaches.

Keywords: Flip flops, QCA, Sequential circuits.

1. INTRODUCTION

Any VLSI design aims at optimization of any of three parameters namely power, area and delay. Many researchers have achieved this optimization using CMOS technology. CMOS technology gives very promising results and if we try to extend the same CMOS technology to nanometer range the length and width of the channel becomes too small and hence transistor loses its functionality. As alternative CMOS in nanometer scale a new technology QCA (Quantum Cellular Automata) has been developed. QCA is one of the promising technologies that have been employed in modern VLSI design for optimization of power and area. The crucial feature of a QCA cell is that it possesses an electric quadrupole which has two stable orientations. These two orientations are used to represent the two binary digits, "1" and "0". In simplest form QCA is four dot nano cell composed of four dots at corner of the square. The fig.1 given below represents a QCA cell. The four dots of quantum cell represent holes and electrons. White colored dots represent holes and black colored dots represent electrons. Thus, there are four dots in QCA quantum cell out of which two are filled with electrons and two are filled with holes and now if we apply charge, the two electrons are free to occupy any hole and thus we can have two different combinations of holes and electrons in as illustrated in fig.1. These two different combinations of holes and electrons are used to represent the two stable states binary 0 and binary 1 in QCA technology.

The QCA are an appealing rising innovation reasonable for the improvement of ultra-thick low-control elite advanced circuits. Hence, over the most recent couple of years, the plan of productive rationale circuits in QCA has gotten a lot of consideration. Exceptional endeavors are coordinated to number-crunching circuits, with the primary intrigue concentrated on the twofold expansion that is the essential activity of any advanced framework. Obviously, the models regularly utilized in customary CMOS plans are viewed as a first reference for the new structure condition. The CFA was an advanced RCA that moderated effects of impending cables.

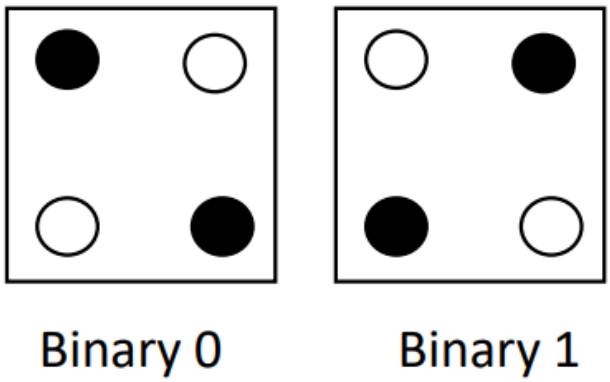

Fig. 1: Structure of QCA.

Parallel prefix structures have been dissected and updated in QCA including Bent Kung adder, kogge-stone adder and Han Carlson adder. For the CLA and RCA, increasingly effective structures have been proposed. In this short, an inventive procedure is introduced to execute fast low-zone adders in QCA. Theoretical definitions displayed for CLA and parallel-prefix adders are here mishandled for the affirmation of a novel 2-piece extension cut. The last empowers the bring to be multiplied through two following piece positions with the deferral of just a single larger part MG. Similarly, the sharp top level building prompts traditionalist configurations, as needs be avoiding unnecessary clock stages as a result of long interconnections. A adder arranged as proposed continues running in the RCA style, yet it shows a computational concede lower than all condition of the-workmanship contenders and accomplishes the most decreased ADP.

2. LITERATURE SURVEY

FLIP-FLOPS (FFs) are fundamental stockpiling components utilized broadly in computerized framework plans, which receive serious pipelining procedures and utilize a few FF-rich modules, for example, register records, move registers, and FIFO. The force utilization of the FFs utilized in a regular computerized framework plan, alongside that of clock conveyance systems, comprises as high as 20%–45% of the absolute framework power. FF plans are in this manner basic to the force utilization execution of the framework structure and may likewise significantly affect the chip territory. FF structures experience ceaseless improvement with the advances in new procedure innovation. Explicit application requests, for example, rapid, low force, and low voltage likewise call for new FF structures. Albeit various FF plans have been created, late structure accentuations have exchanged steadily from ultrahigh-speed flipping to amazingly low-control tasks. Notwithstanding the exchanging power, the spillage power utilization ought to be decreased. The structure is likewise expected to work appropriately for voltage settings underneath the ostensible voltage. Right now, low-power FF configuration meeting these prerequisites is explored. In DET FF, a regular positive-edge-activated flip-flop (FF) faculties and reacts to the control info or contributions at the time the clock input is changing from 0 to 1. It doesn't react at all to alters in the contrary course. Negative-edge-set off FF's act in an integral way. Therefore, these FF's can react all things considered once per clock beat cycle. It is suggested that twofold edgeactivated (DET) FF's, reacting to the two edges of the clock heartbeat would have points of interest as for speed and vitality scattering. In Double edge activating strategy, this technique can be utilized to spare the half of the force on the clock appropriation organize. It utilizes the half recurrence on the tickers conveyance organize by cutting the recurrence of the clock by one half will parts the force utilization on the clock dispersion arrange.

Multiple literatures have been studied about flip-flops uising QCA[1] because they are estimated to be utilized for developing and analysis in real time sequential logics, for example

processers and controllers. In literatures [2-3], QCA based R-S flip-flop was developed. In literatures [4–5] D flip-flop and T flip flop was developed. But this methods does not require any gated clock signals, it only 2-input pins namely reset and set, thus it acts more as latch instead of flip flops. One major problem presents J-K FF presented in[6], level triggered is vulnerable to jitter and noise if logic 1 level drags long period. It indicates that if clock period for logic high level of input is long period, then across output Q race-round condition will generate in flip flop.

3. PROPOSED METHOD

3.1 D-Flip Flop

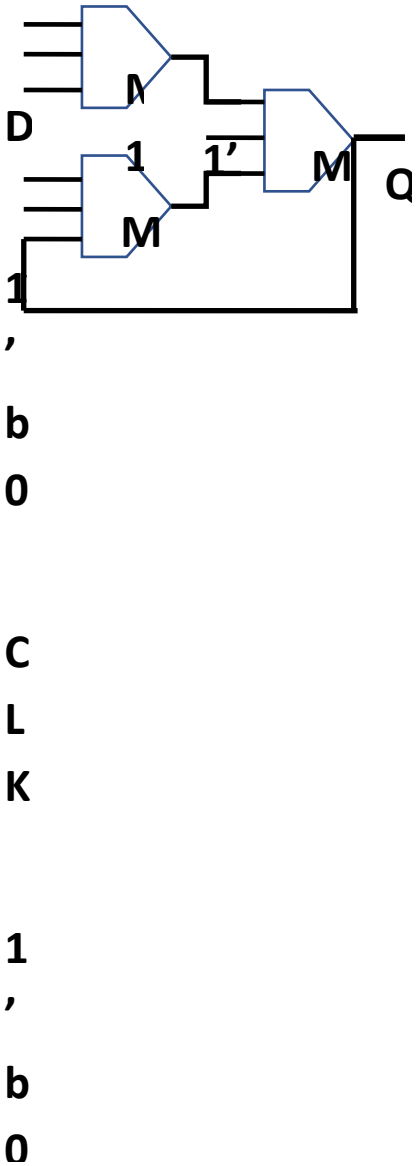

Fig. 2: D-FF using Majority gates.

The above figure 2 represents QCA based DFFs using majority formulations. The M1, M2 are functions as AND operation, M3 functions as OR gate. From the M1 data input D is transferred as output using posedge of clock, from the M2 gate previous state of Q is transferred as M2 output using negedge of clock, across M3 both clock triggered outputs are added and gives final output of present state Q.

3.2 SR-Flip Flop

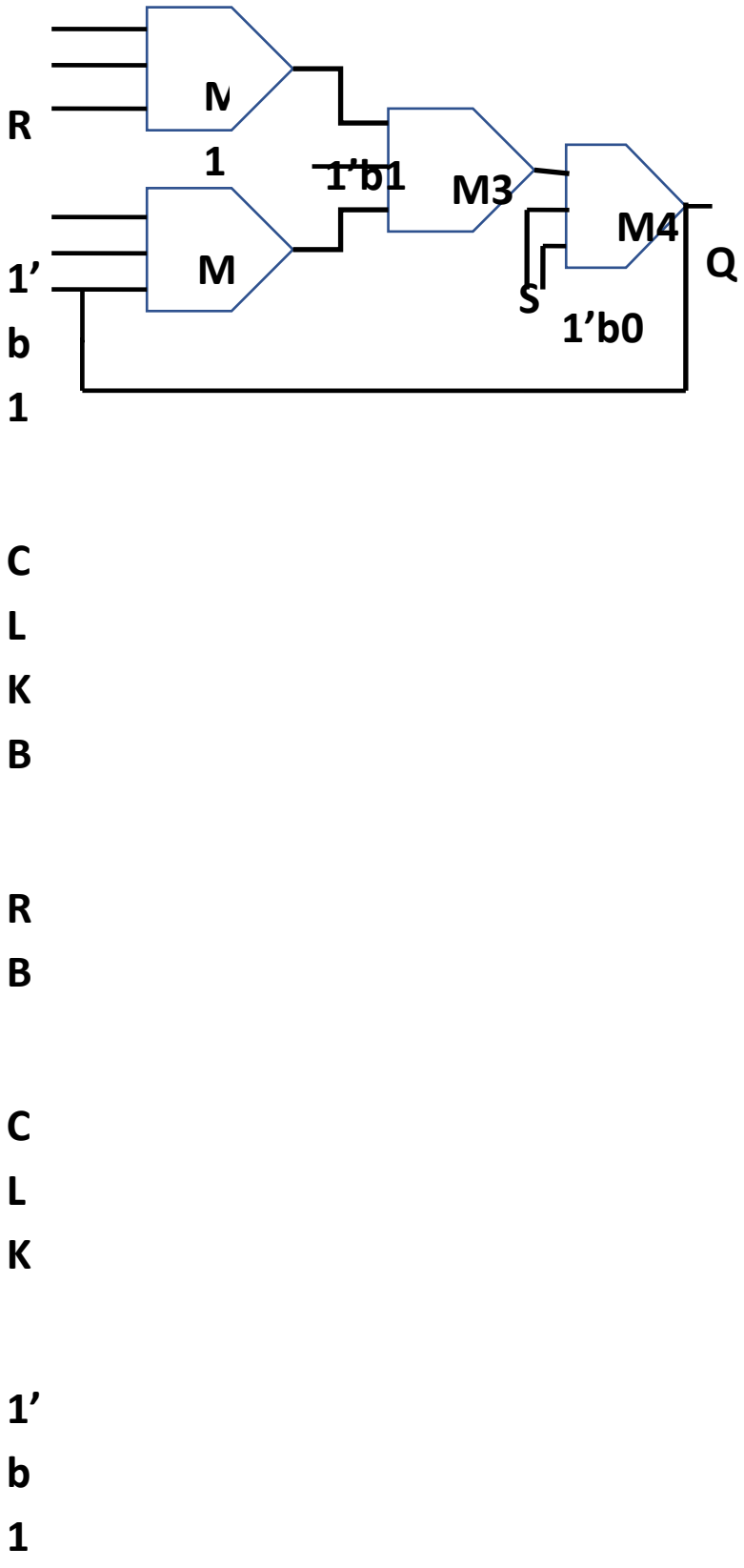

Fig. 3: SR-FF using Majority gates.

The above figure 3 represents QCA based SR-FF using majority formulations. The M1, M2 and M3 are functions as OR operation, M4 functions as AND gate. From the M1,M2 and M3 data input RESET(R) was transferred as M3 output using both the edge triggering of clock, across M4 both M3 output and SET(S) triggered and gives final output of present state Q.

3.3 T-Flip Flop:

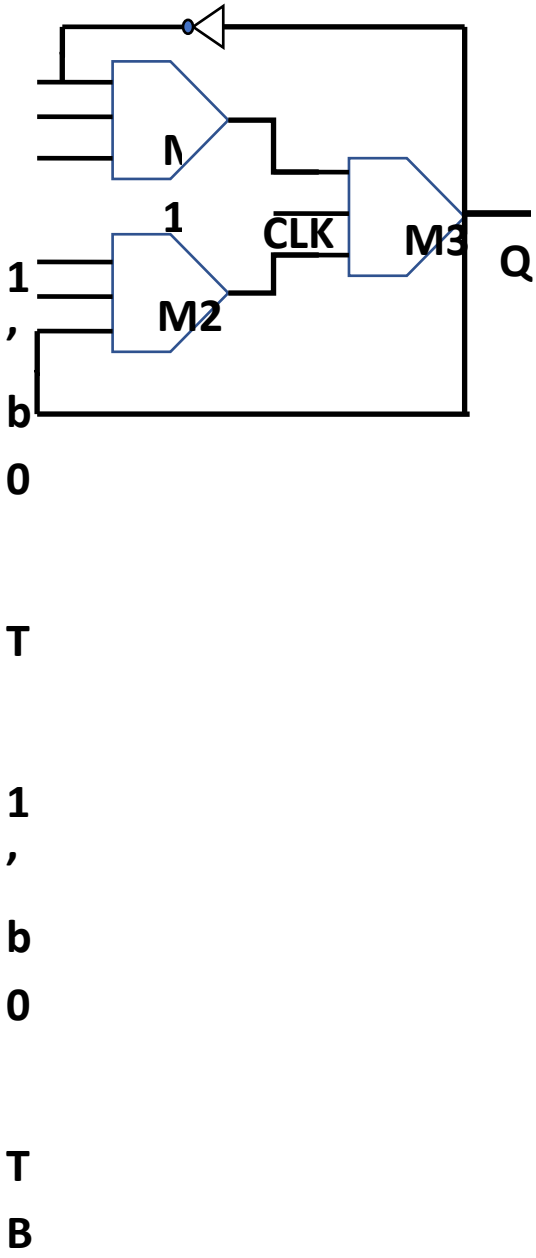

Fig. 4: T-FF using Majority gates.

Sequential logics are arranged with flip flops as the storage blocks. In QCA, storage building blocks are generated by the feedback paths. Furthermore this is implemented by applying clock phase delay to output Q. Fig.4 shows the QCA majority of proposed system of T-FF. It consists of 3 MG gates and 2 NOT gates. The final output Q is same as the exclusive-or function between Toggle (T) input and previous state (Q).

3.4 JK-Flip Flop:

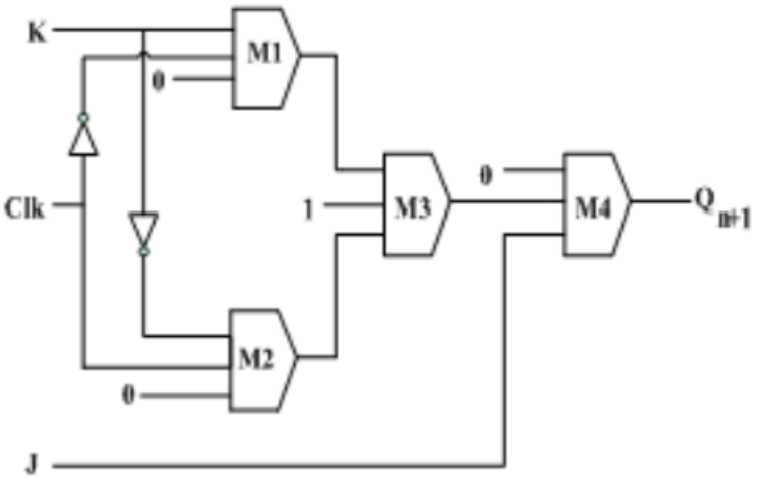

Fig. 5: JK-FF using Majority gates.

The QCA design of proposed JK FF is appeared in Fig. 4. When,J=K=0: then output Q follows its preceding value. It indicates if preceding value in low value then current output is too low. When J, K={0,1}: The current output is equal to '0' for every clock change. When J, K=1,0: the current output is equal to '1' for every clock change. When J=K=1: the current output is the inversion of its preceding value for every clock.

3.5 Counters Using T-Ff

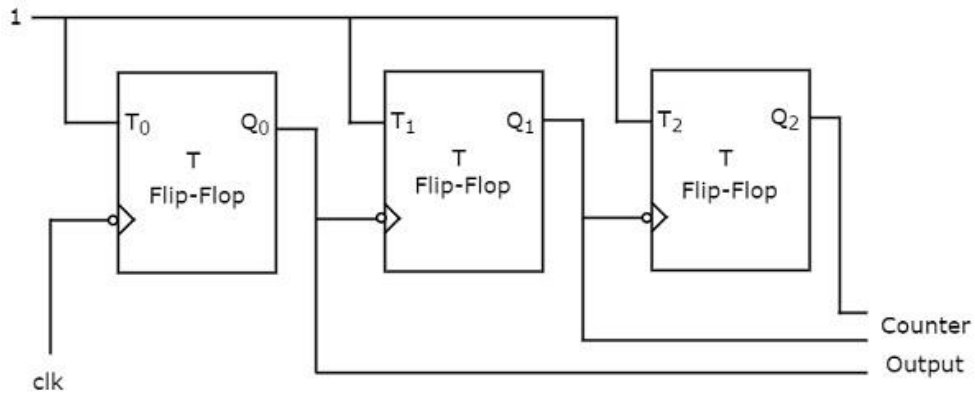

Fig. 6: Asynchronous Up Counter using QCA.

The 3-bit Asynchronous counter consisting of th 3-QCA T-FFs and Toggle-input of all flip-flops are allied to 'high value 1'. All FFs are edge controlled and the outputs alter asynchronously. The original clock is straightforwardly connected to 1st T-FF. So, the present output of first 1st T-FF is straightforwardly connected as clock input to 2nd T-FF. similarly, for N-bit counting operation connections will be same. The counter output observed across all flip flops present states Q at once, and grouped in LSB to MSB format.

3.6 Shift Registers Using D-Ff

The 4-bit synchronous shift register consisting of the 4-QCA D-FFs and clock-input of all flip-flops are allied to single base clock. All FFs are edge controlled and the outputs alter synchronously with

respect to clock, so it will also acts as serial input and parallel output. So, the present output (Q) of first 1st D-FF is straightforwardly connected as data input to 2nd D-FF. similarly, for N-bit shifting operation connections will be same. The shift register output observed across all flip flops present states Q at once, and arranged in LSB to MSB format.

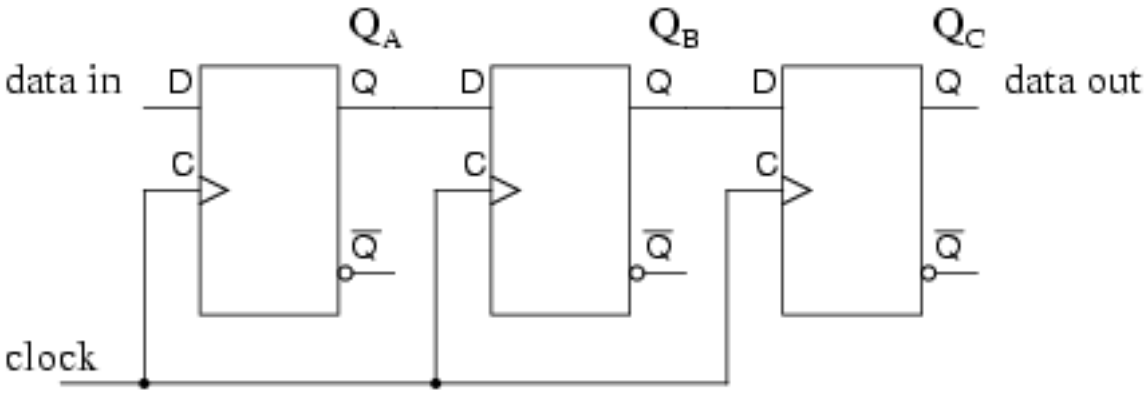

Fig. 7: 4-bit shift register using QCA.

4. SIMULATION RESULTS

All the proposed designs have been programmed and designed using Xilinx ISE software this software tool provides the two categories of outputs named as simulation and synthesis. The simulation results give the detailed analysis of proposed design with respect to inputs, output byte level combinations. Through simulation analysis of accuracy of the addition, multiplication process estimated easily by applying the different combination inputs and by monitoring various outputs. Through the synthesis results the utilization of area with respect to the programmable logic blocks (PLBs), look up tables (LUT) will be achieved. And also time summary with respect to various path delays will be obtained and power summary generated using the static and dynamic power consumed.

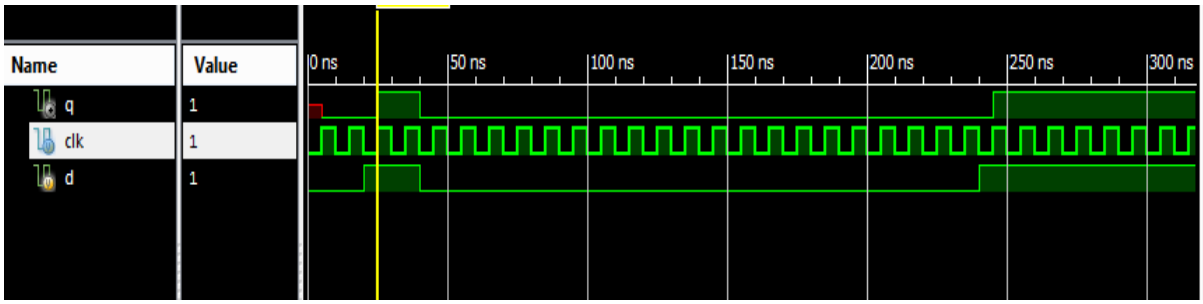

Fig. 8: Simulation output of D-FF.

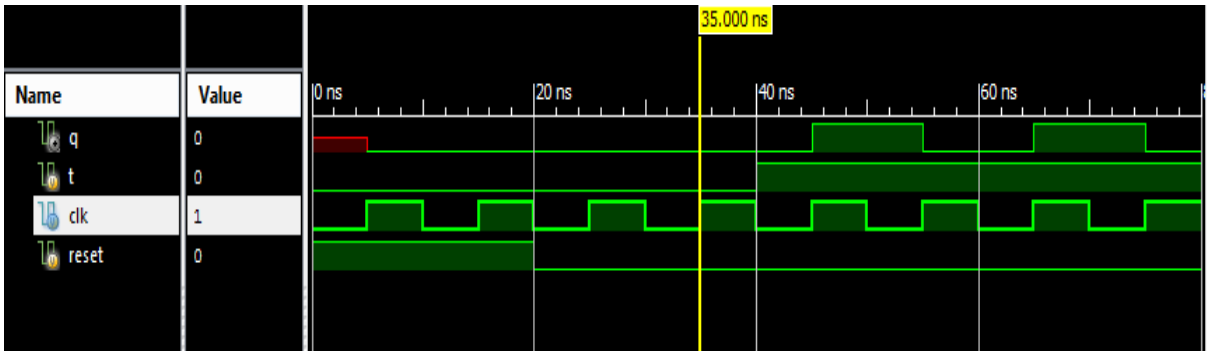

Fig. 9: Simulation output of T-FF.

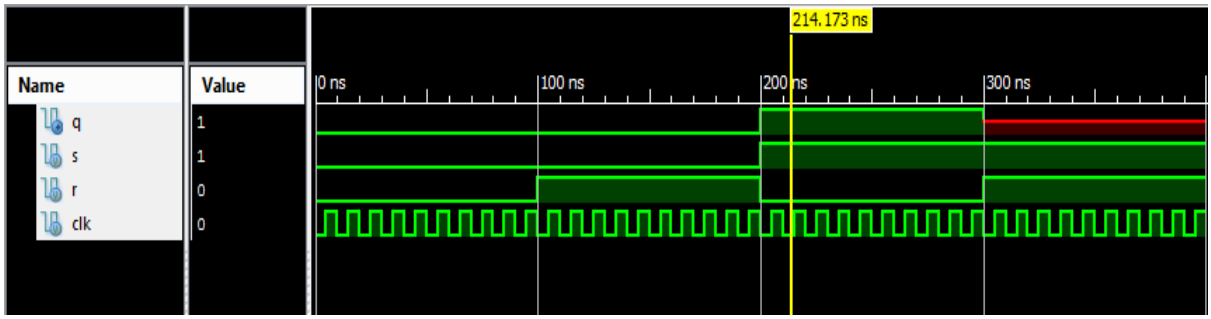

Fig.10: Simulation output of SR-FF.

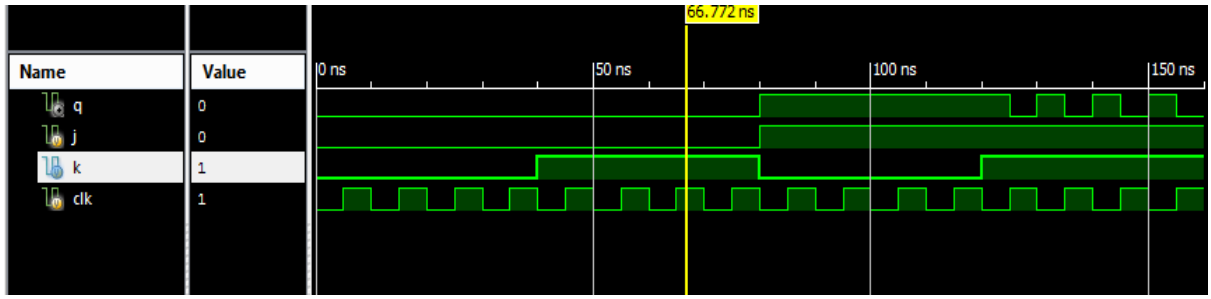

Fig. 11: Simulation output of JK-FF.

The above figures represent the simulation of waveforms by using the Xilinx ISE software for flip flops.

Table. 1: Comparison of Flip-Flops.

Parameter	**CMOS [1]**	**Bi-CMOS [4]**	**QCA-FF**
Time delay(ns)	1.664	3.573	0.882
Power utilized(uw)	0.143	0.384	0.065
Look up tables	3	2	1

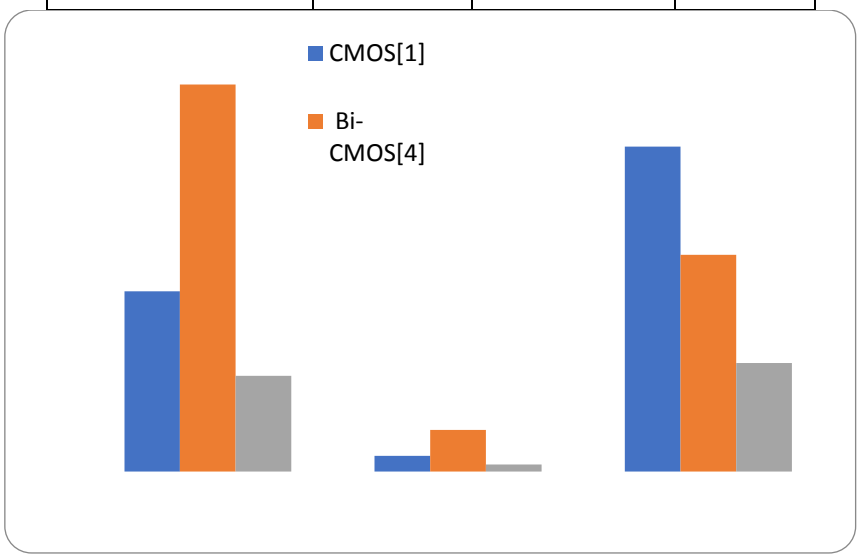

Fig. 12: Comparison of Flip-Flops.

Table. 2: Comparison of shift registers.

Parameter	**CMOS[1]**	**Bi-CMOS[4]**	**QCA**
Time delay(ns)	1.664	3.929	0.356
Power utilized(uw)	0.143	0.065	0.011
Look up tables	3	9	5
Slice Registers	12	28	07

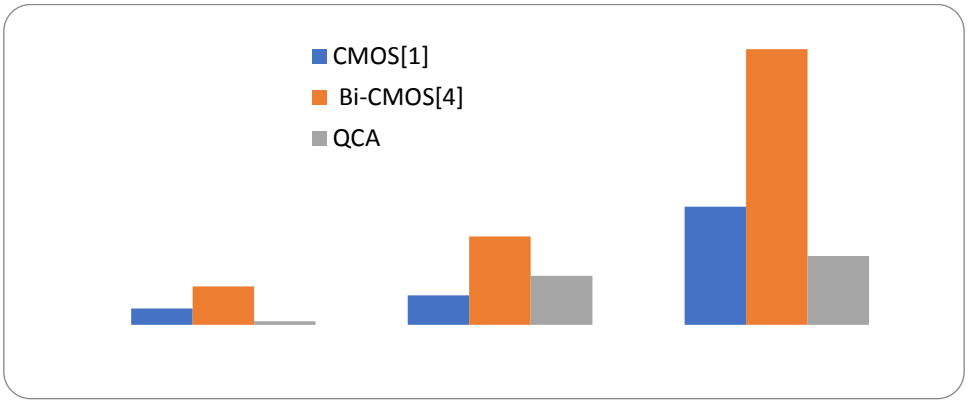

Fig. 13: Comparison of Shift registers.

Table, 3: Comparison of Counters.

Parameter	**CMOS[1]**	**Bi-CMOS[4]**	**QCA**
Time delay(ns)	0.688	3.922	0.521
Power utilized(uw)	1.065	2.019	0.065
Look up tables	4	7	3
Slice Registers	29	23	08

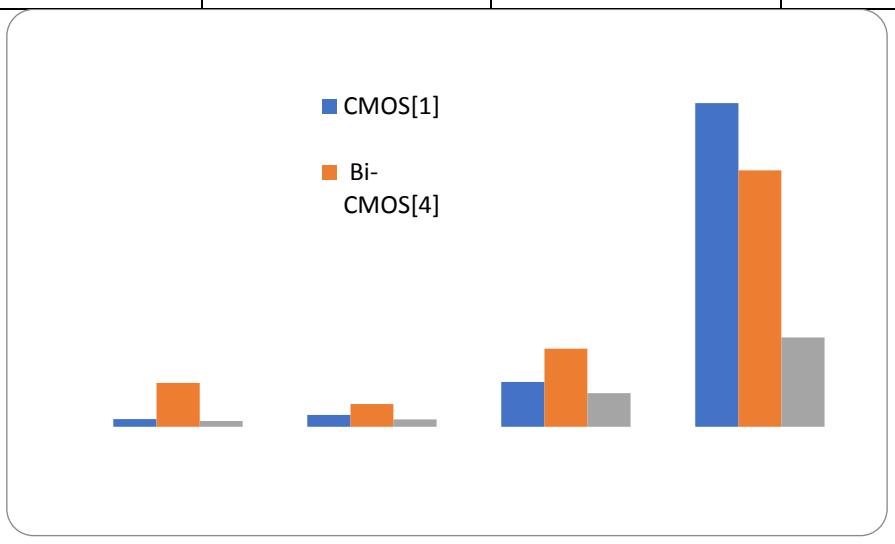

Fig. 14: Comparison of counters.

From table1, table 2, table 3 and Figure 9, figure 10, figure 11; it is observed that the proposed flip flops, shift register and counters developed using QCA showing enhanced area, power and delay properties compared to the conventional approaches CMOS [1] and Bi-CMOS [4].

5. CONCLUSION

In this thesis, a new method of implementing flip-flops, counters and shift registers with smaller amount hardware, area intricacy in nanotechnology. Any storage memory can develop utilizing with these proposed flip-flops. The MG gate designs has been created and simulated using various combinations, finally outputs are generated using Xilinx ISE simulation software. The permanence of the proposed method has been showed better results with respect to area, power and delay compared to conventional approaches.

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