

Protection Schemes for Contemporary Power Systems: FPGA-Based Design and Development

Umang Garg

Asst. Professor, Department of CSE (Computer sc)

GEHU-Dehradun Campus

Abstract: Concurrently functioning relays using FPGA technology are the primary focus of the project. The suggested FPGA-based relays are much faster than microprocessor- or microcontroller-based relays because they use continuous sense-process communicate cycles. The Xilinx Virtex-II FPGA Board's implementation of overcurrent, impedance, reactance, and mho was evaluated using the 400 kv line transmission hardware simulator. Fault currents in power systems may contain a component of direct current (DC) that decays exponentially in the case of transient failures. Extracting the fundamental frequency element is essential for avoiding false tripping. To do this, we make use from the VHDL FFT IP core. A Fast Fourier Transform (FFT) filter is used to implement overcurrent, impedance, reactance, and mho dependence. The FFT filter is also used to evaluate the DC decaying portion.

Keywords: Xilinx Virtex-II FPGA Board, HONALEC, Relays, Fast Fourier Transform (FFT). Microcontroller

Introduction

Modern power systems have evolved from a vertically integrated industry in which a single company was responsible for all aspects of power generation, transmission, and distribution within a given region, to a deregulated power system in which these functions are separated and consumers are free to choose their electricity provider. Despite rising competition and flexibility improving power system efficiency, the presence of several independent entities has made physical power system management very difficult. Power system operating has evolved with advancements in power system protection and power system relaying. The system's first line of defence against power outages and other crises is a network of relays. By cutting electricity to the faulty part while safeguarding the remainder of the system as much as possible, the circuit breaker is operated by relays. Digital relays of today are robust, reliable, and reasonably priced, and they can swiftly adjust to new environmental conditions. When compared to prior relay generations, which used more expensive electromagnetic technology, this is a huge gain. Despite advancements in relay technology, a postmortem assessment of major power system failures from the 1965 US shutdown to the present day has shown that 80% of such catastrophes have been linked to faulty operation of various relays. Some potential reasons why relays stop functioning correctly are as follows:

1. Lapses in the dependability: There was a problem with a relay not working when it should have.
2. Lapses in the security: It seems that an unauthorised relay was activated.

Reliability and security, while both important, are at odds with one another in a relaying arrangement. In classic vertically integrated power systems, reliability has always been prioritised since a large safety margin has always existed on the transmission line. However, with the advent of FACTS devices and the open market structure of today's power networks, it is now favoured to run transmission lines close to their limitations with a little security buffer. In the current context, the security measure is just as crucial. Several unique relaying methods, such as Self-healing power grid, etc., that depend significantly on current ICT have been presented as ways to deal with these technological challenges and keep up with the continuously changing commercial environment in the power system. It is hoped that Measurement, Relaying, and Control of power systems may someday be unified via the use of WAPC, which would be made feasible by the supporting information and

communication technology capabilities. The following are some of the most fundamental needs of a protective relay, in addition to reliability and security.

1. Reliability The dependability of the protective relay is its most important feature. In the absence of a malfunction, relays stay in their inactive state. In the event of an error, however, the relay must function promptly and accurately. High dependability may be attained by paying close attention to such factors as the protective system's design, installation, maintenance, and testing.
2. Selectively When the measured amount is above the set value, the relay should activate. "Pick up value" refers to the minimum detectable signal. The relay should not activate if the measured value is less than its pick up value. For a relay to activate, the measured value must be just higher than the pick-up value.
3. Stability An external failure that is not located inside the protective zone should not affect the stability of the system. The corresponding circuit breaker must be reset to fix the problem. However, the relay will activate to trip the circuit breaker after a delay if the fault is not resolved by the protective system.
5. Fast Operation A relay's problem detection and isolation times must be fast to ensure minimal disruption to the healthy system and continued stability. The stability criterion is of paramount importance in today's power systems, thus the relay's working time must be kept below the crucial clearing time. Keeping the system online for less time will prevent it from breaking down.

Power system protection in general, and power system relaying in particular, have progressed in tandem with the development of power system operating. When power outages or other emergencies threaten to halt system operations, the first line of defence is a set of relays. Modern digital relays are cost-effective, dependable, and resilient, and they can readily adapt to varying physical circumstances. These relays have developed from more costly electromagnetic relays through solid-state relays.

Computer Relay

Advances in VLSI technology have led to the creation of very efficient microprocessors, which are now often utilised in digital relaying.

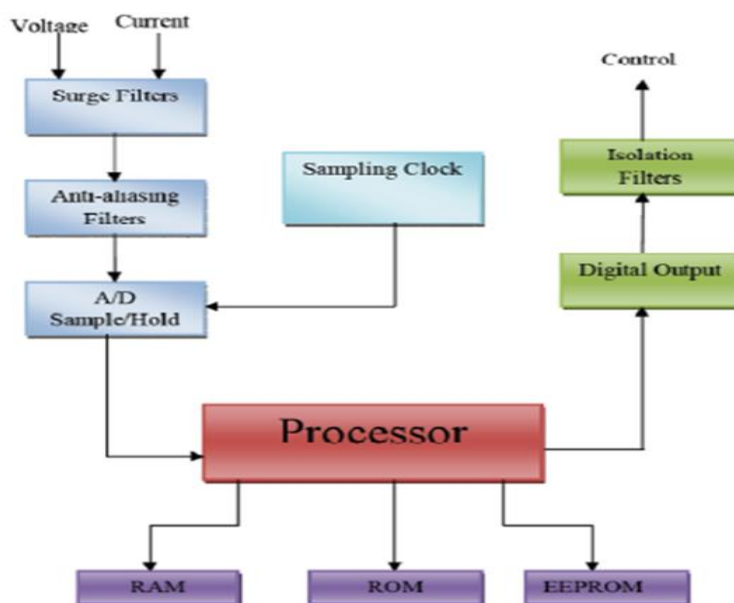


Figure 1: Major Subsystems of a Microprocessor Relay

The use of microprocessors in protective relaying allows for more adaptability, lower costs, reduced space, and easier software testing. It is important to get a digital representation of the system voltages and currents that are typically relay inputs. To do this, the analogue signals are sampled and then converted to digital using an appropriate computer technique. Figure 1 shows a block schematic of the computer.

In this setup, analogue circuits like transducers, surge suppressors, and anti-aliasing filters are used to condition the current and voltage signals coming from the power grid before being sent into an A/D converter for digital processing. In order to sample all analogue input signals at once, independent of the data conversion speed of the ADC, a sample-and-hold circuit is often used. In order to generate a digital output, the relaying algorithm analyses the sampled data.

Conventional protective relays use antiquated transistor technology and should be replaced. The product has been around for a while and has a good track record, but it lacks some of the modern-day conveniences that customers want. This production has a few problems, including:

- Lack of flexibility - Each apparatus is hardware constructed to specific quantity range viz. voltage and frequency.
- Inadequate accurateness and dynamic range - Increased accuracy reduces dynamic range and vice versa
- Communication not possible - Born without communication as no data is available
- Large size - Many components are extend on several PCBs due both to size of components

FPGA Relays

FPGA technology has become the norm in industry and commerce despite these shortcomings. Relays that employ a microprocessor or microcontroller are popular due to the simplicity with which they can be programmed. FPGA stands apart from these devices because of its pipelined architecture, which allows sense, process, and communicate cycles to run concurrently. This work describes the hardware implementation of state-of-the-art power protection relays, which are designed on a field-programmable gate array (FPGA) and use simultaneous sense, process, and communicate cycles. Overcurrent, impedance, reactance, and mho relays are all implemented on a Xilinx Virtex-II Board. It supports both serial and Internet Protocol (IP) connections for communication. This article details the design, fabrication, and testing results of a hardware simulator for a 360-kilometer gearbox line. Communication between relays is also essential in modern electrical networks. For our purposes, we use serial communication between relays. After receiving data from the main relay, the secondary relay makes a call using that data. The secondary relay determines whether the main relay trips or if the load is simply removed. Additionally, a GPS receiver was employed that communicated with the satellites through the NMEA 0183 protocol. The UTC position that the primary relay calculated from the GPRMC data format was sent to the backup relay.

Protective relaying that is based on microprocessors or microcontrollers has several advantages, including adaptability, low cost, small size, and software testing aids. However, microprocessor-based relays follow a sequential order of operations. This chapter provides a hardware implementation of many different types of distance relay using FPGAs. These relays have a pipelined architecture that allows them to process sensor data, assess it, and broadcast signals simultaneously. Distance relay impedance, reactance, and mho are implemented on the Xilinx Virtex-II Board. FFT and serial/IP data transfer are both supported by the remote relay. In this chapter, we detail the results of our in-depth analysis of the design, construction, and operation of a hardware simulator of a 360 km Transmission Line. Relays are getting more complex, with capabilities such as decision making and device compatibility going beyond their basic purpose as programmed emergency response switches. Distance relays are often the first option when looking to safeguard a gearbox's line. Distance relays are based on the voltage and current at the relay's terminals. Distance relays may have a large number of

different features. The process of constructing an FPGA-based impedance, reactance, and mho relay is outlined in this section. FPGA-based distance relays have the advantage of parallel processing over microprocessor/microcontroller-based relays. “In FPGA-based relay, digital circuits may be programmed to operate in simultaneously, enabling the development of multitasking functional units. Sampling, measuring, processing, and communication may all be performed in parallel using FPGA-based designs utilising dedicated pipelines. The effective sample rate of the system will increase as a result.

Implementation Details

Signals from one relay may be sent to another via relay communication. We are using a Xilinx Virtex-IV FPGA Board to implement the main relay and a Xilinx Virtex-II FPGA Board to implement the secondary relay in this study. The relay-to-relay communication paradigm is shown in Fig. 6.1.

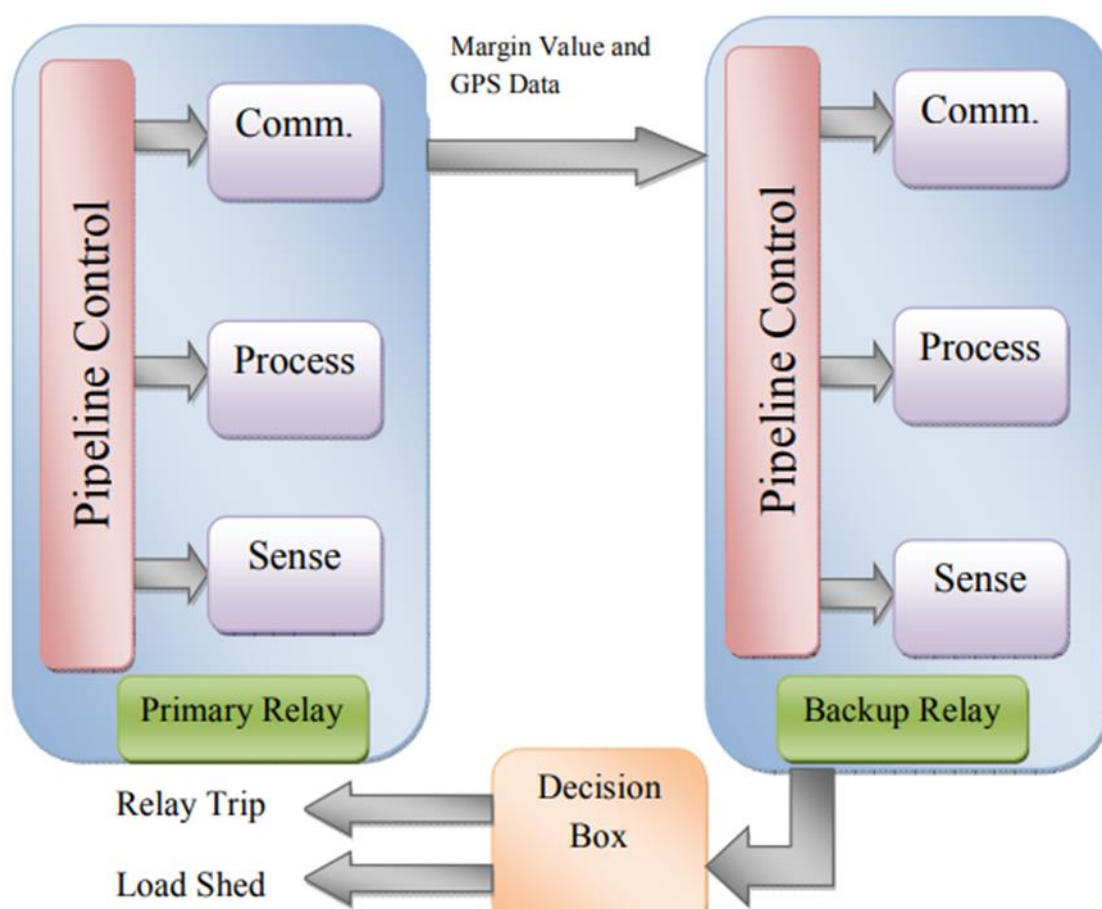


Figure. 2: Relay to Relay Communication Module

Initiating Switch The samples from the ADC are gathered by the primary relay, which then calculates the margin value of the relay and relays that information to the secondary relay. It also receives information from the GPS module and transmits it to the backup relay.

Module Sensation The 7476A is a 12-bit Analogue to Digital Converter in this module. From the point of zero crossing, ADC takes 128 samples. As can be seen in Fig. 2, ADC starts at SOC and ends at EOC to complete the sampling process. The zero crossing is sampled 128 times, and then sent to the FFT IP core. In a single half-power cycle, an ADC may gather 128 samples. The following 128 samples are collected after the first 128 have been sent to the FFT IP.

Methodical Unit From the zero crossing, 128 samples are gathered by the FFT IP core from the sensing module. The FFT IP core uses a burst design, which requires the collection of 128 samples before any loading or unloading can take place. IP cores for FFTs that can process 2's-complement samples. Once the samples have been unloaded, we use the FFT to determine the fundamental frequency component. The difference between the measured value and the peak value is then used in the margin value calculation.

Modula R Communicate The RS232 interface [RHY 14] is used to gather GPS data using a Rhydolabz GPS-2102 serial/USB receiver. The NMEA 0183 format is used for the serial data. Media Tek MT3329 chipset is used in GPS receiver. The main relay receives GPS data on the UART Rx line of the Virtex4 FPGA. The GPS receiver delivers data on the Tx pin at 9600 baud rate. Figure 3 depicts the RS232 serial interface used for bidirectional communication between the primary and secondary relay.

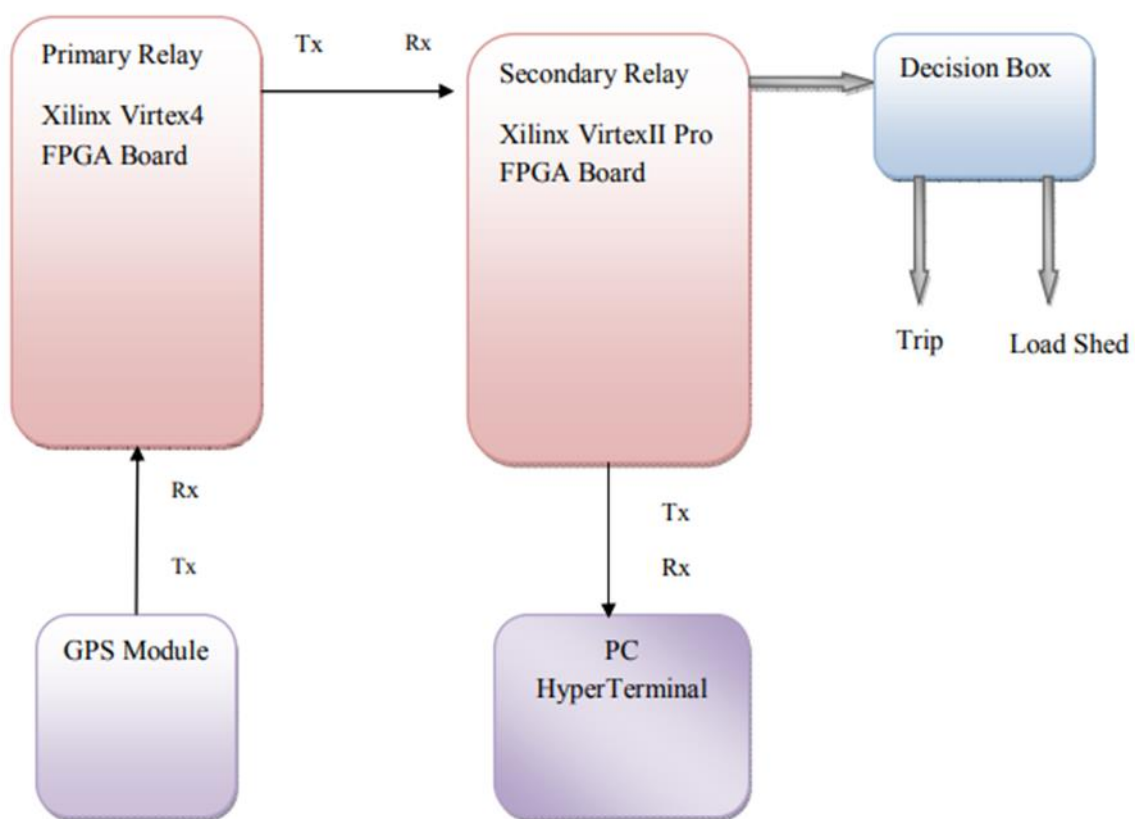


Figure 3.: Communication Interface between Primary and Secondary Relay

The GPRMC header is parsed to get the time zone offset in UTC and convey that information to the secondary relay. In Fig. 4, where the letter 'V' means receiving incorrect data, it can be shown that the GPS-2102 did, in fact, receive faulty serial data. Data serially received by GPS-2102 was valid.

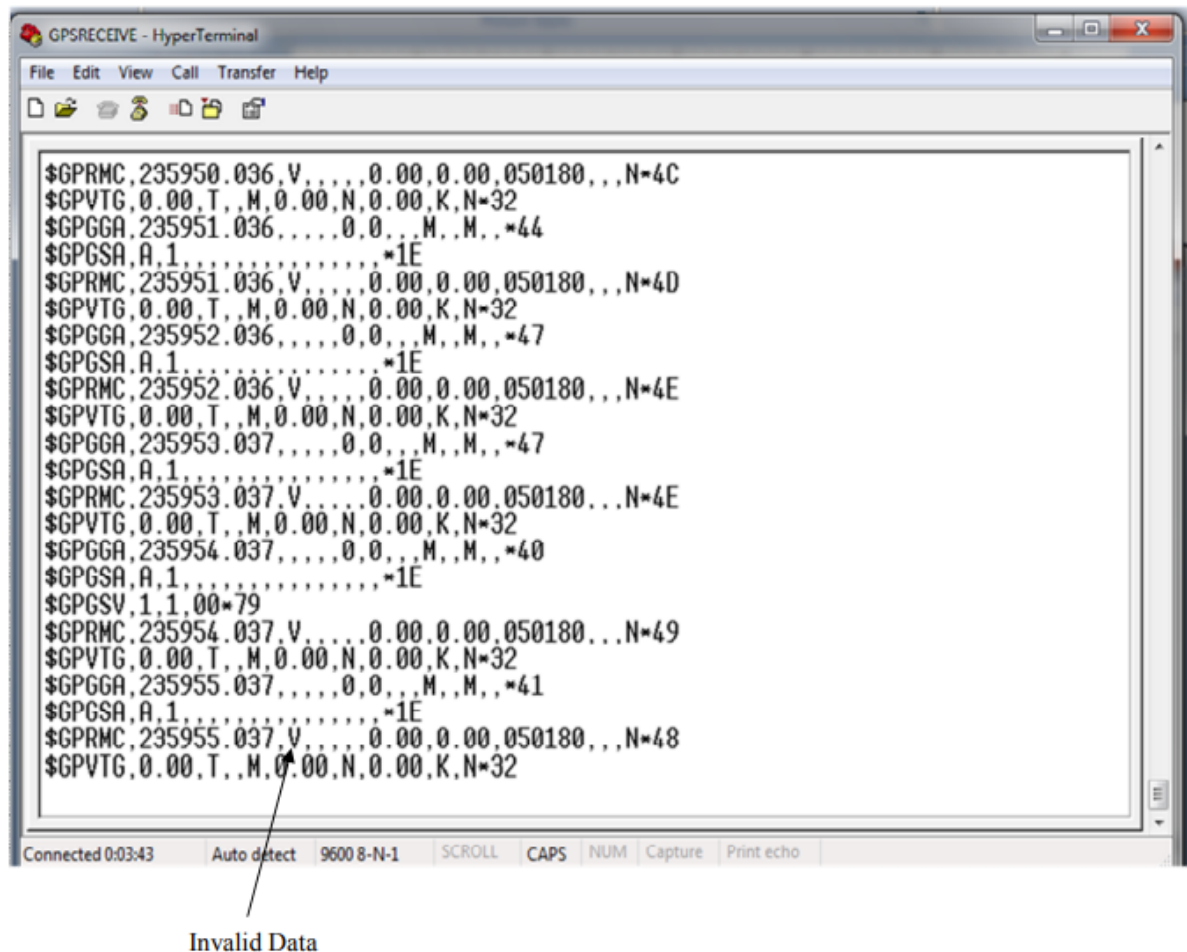


Figure. 4: Communicated Invalid Data Received from GPS 2102 to Hyper Terminal

Conclusion

Protection measures for today's power systems rely primarily on clear and consistent lines of communication. In order to avoid slowing down the electrical grid, relays have to be able to recognise data, evaluate it, and send the results. In this paper, we demonstrate how to design and implement a relay that communicates over Serial/IP and makes use of an FPGA. We propose a pipeline-based, simultaneous layout for the Sense, The procedure, and Communicate cycles. There are several different types of relays that may be included on an FPGA board, including overcurrent, resistance, reactance, and mho relays. The design is implemented on a Xilinx Virtex-II FPGA board using the VHDL programming language. The use of GPS coordinates for relay-to-relay communication is also covered in the thesis. Two different Xilinx FPGA boards, the Xilinx Virtex-II or the Xilinx Virtex-IV, are utilised to implement the main or secondary relay, respectively.

References

1. M. G. Adamiak, A. P. Apostolov, M. M. Begovic, C. F. Henville, K. E. Martin, G. L. Michel, A. G. Phadke and J. S. Thorp. Wide Area Protection Technology and Infrastructures. IEEE Transactions on Power Delivery April 2006; 21(2):601-609.
2. M. E. Agudo, B. Kasperek, S.I. Thomson. End to end relay testing using GPS synchronized secondary injection. IEE Conference on Developments in Power System Protection 2001; 42-45.

3. S. Ahuja, L. Kothari, D. N. Vishwakarma and S. K. Balasubramanian. Field Programmable Gate Arrays Based Overcurrent Relays. *Electric Power Component and Systems* 2004; 247-255.
4. T. Amraee, A.M. Ranjbar, R. Feuillet and B. Mozafari. System protection scheme for mitigation of cascaded voltage collapses. *IET Generation Transmission Distribution* Mar 2009; 3(3):242–256. ANA, “Web services description language”, retrieved Dec 18,2012 from http://www.analog.com/static/importedfiles/data_sheets/AD7476A_7477A_7478A.pdf
5. M. M. Begovic, A. R. Messina. Wide area monitoring, protection and control. *IET Generation Transmission Distribution* 2010; 4(10):1083-1085.
6. V. Betz, J. Rose and A. Marquardt. *Architecture and CAD for Deep-Submicron FPGAs*. Kluwer Academic Publishers; 1999. [
7. J. Bhasker. *VHDL Primer*. Third Edition. Addison Wesley Longman; 1992. [BLU 12] S. Blumsack and A. Fernandez. Ready or not, here comes the smart grid. *Energy* 2012; 37(1):61-68.
8. S. M. Brahma, P. L. De Leon and R. G. Kavasseri. Investigating the Option of Removing the Antialiasing Filter from Digital Relays. *IEEE Transactions on Power Delivery* 2009;24(4):1864-1868.
9. M. Breuer. A Class of Min-cut Placement Algorithms. *IEEE/ACM Conference on Design Automation* 1977; 284-290
10. Stephen Brown and Zvonko Vranesic. *Digital Logic Design with VHDL*. Second Edition. Tata McGraw-Hill; 2011.
11. V. Centeno, J. De La Ree, A. G. Phadke, G. Michel, R. J. Murphy and R.O. Burnett. Adaptive Out-of-Step Relaying Using Phasor Measurement Techniques. *IEEE Computer Application in Power* August 2002;6(4):12- 17.
12. R. M. Chabanloo, H. A. Abyaneh, S. S. H. Kamangar and F. Razavi. Optimal Combined Overcurrent and Distance Relays Coordination Incorporating Intelligent Overcurrent Relays Characteristics Selection. *IEEE Transactions on Power Delivery* July 2011;26(3):1381-1391.
13. C. S. Chen, C. W. Liu and J.A. Jiang. Application of Combined Adaptive Fourier Filtering Technique and Fault Detector to Fast Distance Protection. *IEEE Transactions on Power Delivery* April 2006;21(2):619-626.
14. C. R. Chen, C. H. Lee and C. J. Chang. Optimal Overcurrent Relay Coordination in Power Distribution System Using a New Approach. *International Journal of Electric Power and Energy Systems* February 2013;
15. Y. S. Cho, C. K. Lee, G. Jang and H. J. Lee. An Innovative Decaying DC Component Estimation Algorithm for Digital Relaying. *IEEE Transactions on Power Delivery* 2009; 24(1):73-78
16. A. Conde and E. Vazquez. Operation Logic Proposed for Time Overcurrent Relays. *IEEE Transactions on Power Delivery* 2007; 22(4):2034-2039
17. A. Conde. Design of an Interactive Application for Educational Support and Performance Analysis of Overcurrent Relay. *International Journal of Electrical Power and Energy Systems* 2014; 59:123-129.
18. J. Cong and Y. Ding. Flow Map, An Optimal Technology Mapping for Delay Optimization in Lookup-Table Based FPGA Designs. *IEEE Transactions on Computer-Aided Design* January 1994; 13(1)
19. M. T. Craig, C. Jorge, L. Alberto and B. Alan. Improvements in Power System Integrity Protection Schemes. *IET Conference on Developments in Power System Protection, Managing the Change* March 2010
20. J. Faiz, S. Lotfifard and S. H. Shahri. Prony-Based Optimal Bayes Fault Classification of Overcurrent Protection. *IEEE Transactions on Power Delivery* 2007; 22(3):1326-1334.