Design of high speed and low cost Novel Hybrid Adder for VLSI applications

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Abstract: Design of high speed and low cost Novel Hybrid Adder for VLSI applications is implemented in this paper. In VLSI chips adder is used as critical element for implementation. Adder's plays major role in circuits of ALUs, Floating point arithmetic units, memory addressing and program counting. Trade off occurred between the circuits is reduced because of Novel adders. Size of the parallel circuit is determined based on the nodes. VLSI synthesis tool is utilized to simulate Novel adder. Effective results are obtained compared with RCA.

KEY WORDS: Carry Look Ahead Adder (CLA), Ripple Carry Adder, Adder, CMOS, VLSI, Propagator and Generator (P & G).

I. INTRODUCTION

Basically, in VLSI chip design signal processing is implemented for effective integration in the system. In present generation, integration plays major role to get effective output. Here energy is consumed and capacity of signal is computed in signal processing applications [1]. In VLSI design mainly energy and area plays important role in the entire system. Two main forces are required to reduce the energy consumption. The operating frequency and chip capacity is operated in the system for the purpose of growth. By using cooling techniques the energy consumption is determined. In electronic devices the battery life plays important role in the system. There will be a limitation for battery life and the operation time is also prolonged in the entire system.

In signal processing algorithms, multiplication operation plays important role in entire system. By using adders, energy and latency is considerable. In VLSI design, adder gives low energy consumption. Logic levels and circuit in multipliers is extended and area is consumed. To perform high speed operations, multipliers are arranged in parallel form. Adders are classified based on two multipliers. They are fully parallel adders and fully serial adders [2]. Various bits are operated using single digit serial multiplier. Here by using this, both area and speed is operated at highly.

In digital computers and digital signal processor, the addition operation is performed effectively. Arithmetic operations are performed in basic building blocks which plays major role in entire system. In hardware architecture, arithmetic unit plays major role and process of addition operation is easily performed. Different characteristics and different architectures are existed to perform the arithmetic operations. Binary adder structure is implemented and compared with various analyze [3-4].

The configuration of adders are classified into various types they are Ripple carry adder, carry skip adder, carry look ahead adder and carry select adder. Carry skip optimization algorithm is introduced to map the problems occurred in the system. Multi level tree structures are implemented in the carry skip optimization technique. This will fix the length of modules in the system. This will optimize the number of levels, number of sizes and number of blocks. Carry signals are carried to increase the speed of the buffers. CMOS will implement the logical configurations in the narrow fields. Static and dynamic gates are implemented to limit the operations of binary adders [5].

II. LITERATURE SURVEY

Ashish Yadav, Bhawna P. Shrivastava and Ajay Kumar Dadoria.et.al [6]

Low power designs has become one of the primary focus in Deep Sub-Micron (DSM) Technology. Optimization of speed, power and area can be achieved by using Gated Diffusion Input (GDI) technique. In this paper an 11T Adder using GDI technique is proposed and it is compared with

various existing adder circuits for Average Power dissipation, delay & PDP. Proposed circuit is designed using Cadence Virtuoso Tool for 180nm CMOS technology. Area has been evaluated by Microwind using TSMC BSIM 180nm technology. A comprehensive study and analysis of various Adder circuits has been done in this paper and comparison of proposed 11T adder (input 1 bit) with these circuits shows reduction in Average Power by 93.25%, 59.16%, 64.09%, and 85.28 % with respect to 28T, GDI, SERF & 8T circuits respectively. Proposed adder with 8 & 16 bit inputs are also implemented.

S.Nagaraj, Dr. G.M.Sreerama Reddy, Dr. S.Aruna Mastani.et.al [7]
In this paper we design and analyse different types of adders using CMOS, Complementary Pass Transistor Logic(CPL), Double Pass Transistor Logic(DPL) logics. Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Incremental Adder, Carry Skip Adder, Carry Select Adder, Conditional Sum Adder are designed using CMOS, Complementary Pass Transistor Logic(CPL), Double pass transistor logic(DPL) logics for 16-bit, 32-bit and their speed, area and power are compared.

Kartheek Boddireddy, Boya Pradeep Kumar , Chandra Sekhar Paidimarry.et.al [8]
Adders play an important role in digital circuits. Logarithmic adders are efficient in delay reduction of carry generation/propagation in contrary to linear adders. It is found from simulations that even logarithmic adders suffer from delay, chip area over head and additional latches in the presence of ripple carry adders at the time of FPGA realization. The main motive of this work is to design and develop optimized delay free adders by introducing the proposed leaf adder module. In this work, we propose optimized Kogge-Stone and Spanning tree adders based on carry-tree architecture. Our designs are simulated using Verilog HDL and implemented on Xilinx Virtex-5 FPGA for real time verification. Performance metrics such as delay and chip area are evaluated using our numerical simulations. It is shown from results that our optimized Kogge-Stone and Spanning tree adders achieve 13.9% and 1.5 % reduction in delay: 24% and26.5% in LUT reduction; and 25.9% and 23.8% in slice reduction respectively, compared to existing tree adders.

Pavan Kumar.M.O.V, Kiran.M.et.al [9]
The complexity in digital circuits has increased with rapid growth in technology permeating into all areas including ALU, Memory addressing, PC updates etc. All of them depend on logical elements and Adders are logic elements that play a critical role in design and performance of different operations. Thus there exists a considerable interest in digital electronics for designing high speed and low complex adder architectures. Different adders came into existence such as Carry save Adder, Carry Look-a-head Adder, and Ripple Carry Adder, Carry Select Adder etc. Carry Select adder uses multiple pairs of Ripple Carry Adder. Using Carry Select Adder (CSLA) the carry propagation delay can be reduced to a certain extent. The carry is selected in this case and the architecture is modified. CSLA is a way to improve the speed by duplicating Ripple Carry Adder (RCA), due to the fact that the carry can only be either 0 or 1. This method is based on the Conditional Sum Adder and extended to a Carry-Select Adder. CSLA uses multiple pairs of RCA with each computing the case of the one polarity of the carry-in, and the sum is obtained with a 2-1 multiplexer with the carry-in as the select signal. Parallel Prefix Adders (PPA) is used to reduce the delay caused due to carry propagation. They use carry trees wherein the delay will be in the order of log2N for an N-bit width adder. This study opted for the Ling algorithm among the many phenomenons developed on Kogge-Stone structure. The logic is to utilize and employ the property of carry propagation and generation. Using a PPA the delay will be reduced by a percentage of up to 20% of the original delay. This study is an attempt of comparing various fast adders in 45nm CMOS technology with the support of CADENCE tools. The result analysis revealed that the proposed adder is optimal when compared with various fast adders of 16 bit.

Poornima N, V S Kanchana Bhaaskaran.et.al [10]
Addition is a vital operation in all data paths. The power dissipation and speed performance remain the primary factors that identify the choice of adders. To achieve the desired energy efficiency or lower power dissipation, the selection of the particular adder topology plays a major role. The operating speed of adder or the circuit latency of adder can be minimized by the use of architectures such as Parallel Prefix Adders (PPAs). This paper presents a radix-4, 32-bit Parallel Prefix Adder with a sparseness of 4. The work involves the structural realization and implementation of a 32-bit adder using radix-4 and comparison with a radix-2 32-bit adder for the power, delay, power-delay-product (PDP) and the number of computational nodes. Simulation results reveal that the radix-4 32-bit Parallel Prefix Adder realizes minimum PDP. The effects of introducing the radix-4 and sparseness on power and delay parameters of the adder structure are analyzed. Cadence EDA tool is used for the schematic implementation of the adders and simulations have been performed using 180nm bulk CMOS technology.

III. OVERVIEW OF HYBRID ADDER

One or more logics are used to implement adder, it is known as Hybrid adder. The inputs for module 1, module 2 and module 3 are A and B. In this, different type or same type of adders can be used. The outputs are sum and carry are produced. Multiple logic values can be formed by using same type adders or different type's adders. The below figure (1) shows the block diagram of hybrid adder.

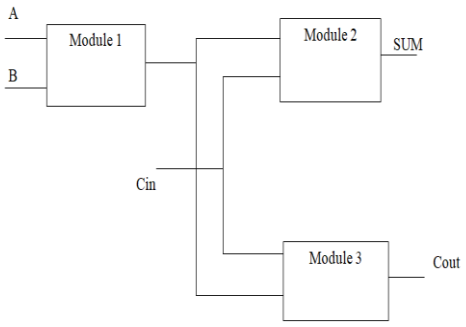

Fig. 1: Hybrid adder block diagram

The formation of Hybrid adder contains two types of architectures.
1 Homogeneous: Homogeneous architecture is formed by merger of same type of two or more adders.
2 Heterogeneous: Heterogeneous architecture is formed by merger of different type of two or more adders.

Low cost products and high performance produced by Hybrid structure due to combining designs. By considering advantages and limitations of individual adder, Hybrid adder can be performed by design engineers. 4-bit hybrid adder circuit is represented in below figure (2) which combines advantages of both adders. The full adder contains three inputs those are A and B and carry in. Carry out and sum outputs are produced by full adder. Carry-in port is used in carry save adder as another input of operand, so that three numbers can be operated. Sum and carry are obtained from first stage. Half adder is used for two inputs operation, in that propagation delay is reduced. Sum and carry are produced by half adder which is given to the carry skip adder along with skip logic.

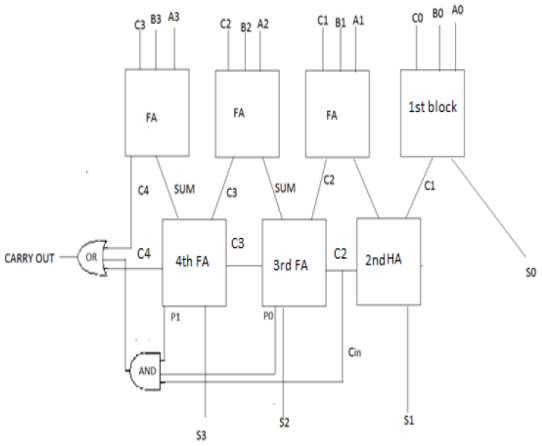

Fig. 2: Block diagram of 4- bit hybrid circuit

First carry save adder is considered. We know that in 1st block from A0, B0, C0 to C1, 4 gates delay is occurred. 4 gates delay is occurred in the 2nd FA block from C1 to C2 and C1 acts as operand.2 gates delay is occurred from C2 to C3. Similarly 2 gates delay is occurred from 3rd FA to 5th FA. 2 gates delay is occurred from last 5th FA. So that total delay is calculated as 4+4+2+2+2 is equal to14 gates delay for 4-bit CSA.

Now Hybrid circuit is considered. 4 gates delay occurred in the 1st block from A0, B0, C0 to C1. C1 acts as operand in the 2nd HA block so that it provides 1 gate delay. 2 gates delay occurred when C2 given to skip logic circuit. So that total delay is calculated as 4+1+2 is equal to7 gates delay for 4-bit circuit.
Advantages of the hybrid circuit:

- Advantages of two adders mixed in the Hybrid adder. It can be operate on three inputs and to speed up the calculation carry is skipped.
- For the calculation, simple RCA is used in CSA after first stage. But in Hybrid adder, carry skip adder is used than RCA, carry skip adder is more efficient.
- 2 carry skip logic circuits are used in 4-bit carry skip adder; more complexity of circuit is caused. But hybrid adder required 1skip block, so that circuit complexity is reduced.
- Extra XOR block is needed to obtain Pi block but XOR circuit is used from adder block in the Hybrid adder, so that number of gates and delay is reduced.

IV. NOVEL HYBRID ADDER

The below figure (3) shows the block diagram of Novel hybrid adder. In this mainly we use carry look ahead adder generator, propagator and generator and carry generation cells. The n-bits of an operand are divided into groups with a CLA in each group and each group is connected by using a RCA. The n-bits are divided in equal size for easy design and modularity.

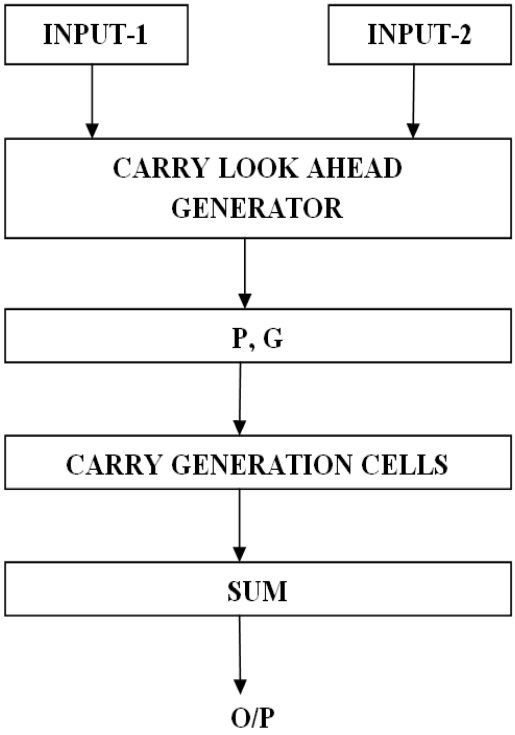

Fig. 3: Block Diagram of Novel Hybrid Adder

In group CLA the group carry generation and propagation are represented by G*, P*.
The G*= 1 if carry out from the group is produced.
The p* = 1 If all propagation P_0, P_1, P_2, P_3 bits inside the group are 1.
Group-generated carry G*= 1 if a carry-out (of group) is produced with in the group.
Group-propagated carry P*=1 if a carry-in (to group) is propagated internally to produce a carry-out (of group).
For each group the carry generate and carry propagate equations are given below
$G^* = G_3+G_2P_3+G_1P_2P_3+G_0P_1P_2P_3$
$P^* = P_0P_1P_2P_3$
The CLA works on the principle of determining, whether carry will generate or not based on input signals even before the actual addition performed. Here, it is illustrated an example addition two binary operands, which shows the difficulty arising due to the delay in carry propagation [3-5].

As a solution to this problem CLA is implemented. This leads to less delay in propagation of the carry. To make the concept of CLA much clear to control the logical expressions corresponding to the full adder. The equations of full adder regarding carry propagate and generate are given as

$$\text{Carry propagate } P_i = A_i \oplus B_i$$

$$\text{Carry generate } G_i = A_i \times B_i$$

The above equations clearly shows that both signals G and P can be produced by using input bits with in time of one gate delay. The rewritten expressions for sum S_i and carry C_{i+1} in the form of P and G are given by:

$$S_i = P_i \oplus C_{i-1}$$

$$C_{i+1} = G_i + P_iC_i$$

There are only two chances in getting carry while doing addition. One chance is when two input bits A_i and B_i are 1. Second chance is when at least one of input bits is one and carry input C_i is 1.

The common equation for carry in CLA is

$$C_{i+1} = Gi + PiG_{i-1} + PiP_{i-1}G_{i-2} + \ldots\ldots PP_{i\,i-1}\ldots.PP_{2\,1\,0}G + PiP_{i-1}\ldots.P_{1\,0\,0}C_0$$

The above expression can be realized using two stage circuit. But, in CMOS logic the delay of the circuit varies nonlinearly with the fan-in. The implementation of high fan-in circuits is not possible. Hence the CLA circuit is spitted into three stages. The levels are

- Carry propagate/ generate P_i and G_i
- Performing actual addition operation Sum bit S_i
- Carry generation C_{i+1}.

Stage 1: In this stage carry propagate and generate signals are produced. For 4-bit CLA it has 4 carry propagate and generation logics each having XOR and OR gates. Only one gate for each signal therefore, the delay is 1τ.

Stage 2: In this stage all carry signals are generated according to the equations defined above. It requires a two-level realization of gates. So, carry bits generated after delay of 3τ.

Stage 3: The final result sum signal (Si = Pi ⊕ Ci) is produced after the delay of 4τ. This is because it needs 4 XOR gates to generate it. This delay 4τ is less rather than $(2_{n+1})\Delta\tau$ in carry propagate adder.

The CLA has benefit of speed but it has a disadvantage of composite carry expressions makes it not reliable for large number of bits. The drawback of the CLA adders is that the realization of circuit turns to be hard for the number of bits.

V. RESULTS

The below figure (4) shows the RTL schematic of Novel Hybrid adder. Here a, b are the inputs and sum and carry are the outputs and c0 is the additional carry that is obtained while addition process.

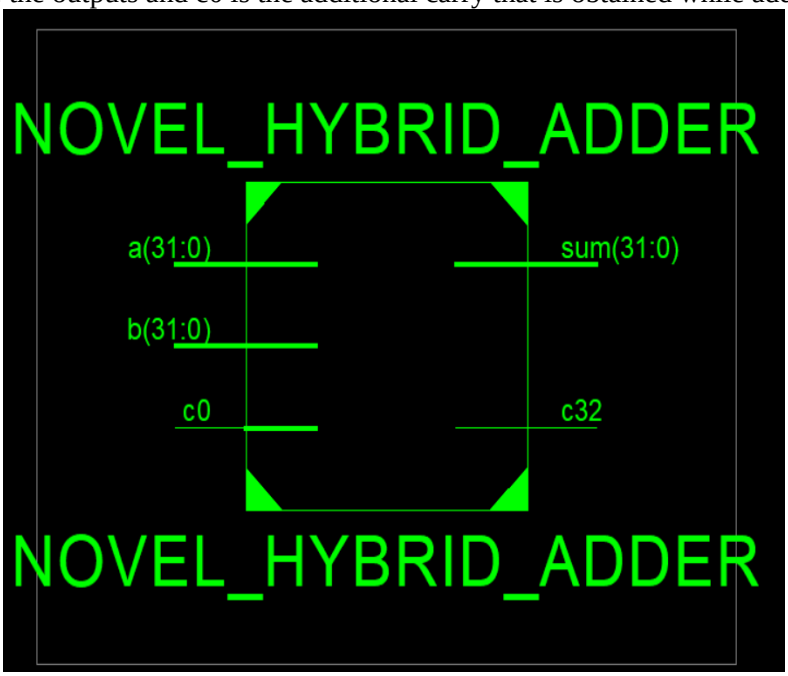

Fig. 4: RTL Schematic of Novel Hybrid Adder

The below figure (5) shows the Technology schematic of Novel Hybrid adder. Basically, the technology schematic is the combination of look up tables, equations, K-map and truth tables.

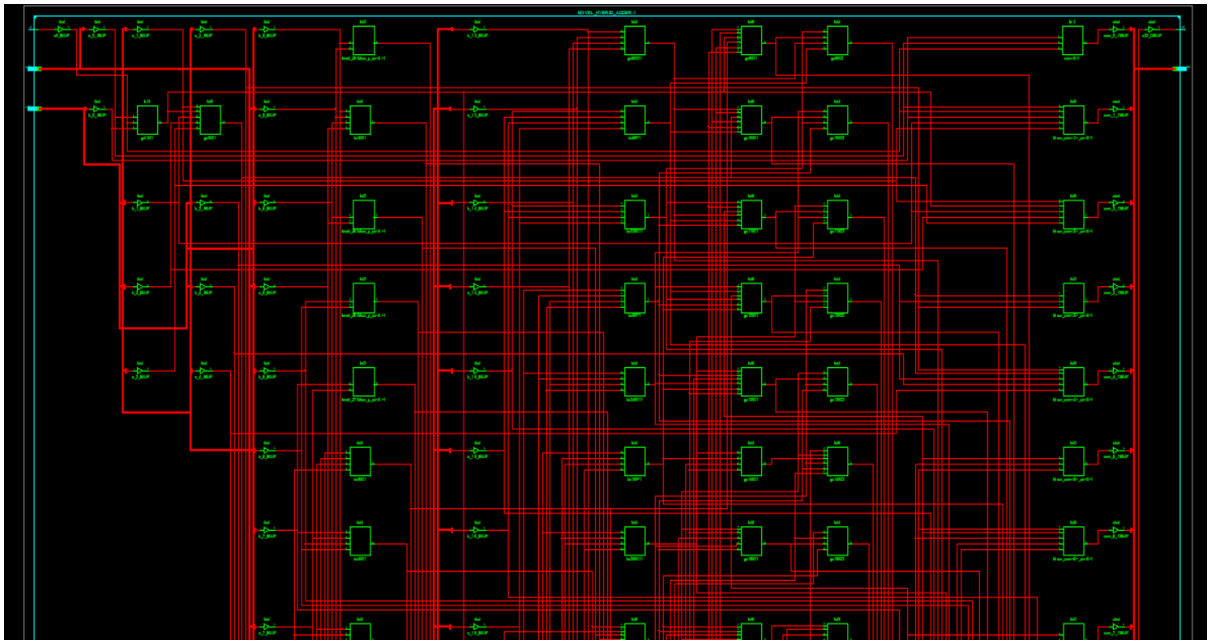

Fig. 5: Technology Schematic of *Novel Hybrid Adder*

The below figure (6) shows the output waveform of Novel Hybrid Adder. Here for gives inputs corresponding output is obtained which is shown from the below figure. Compared to the other system, the novel hybrid adder gives effective results.

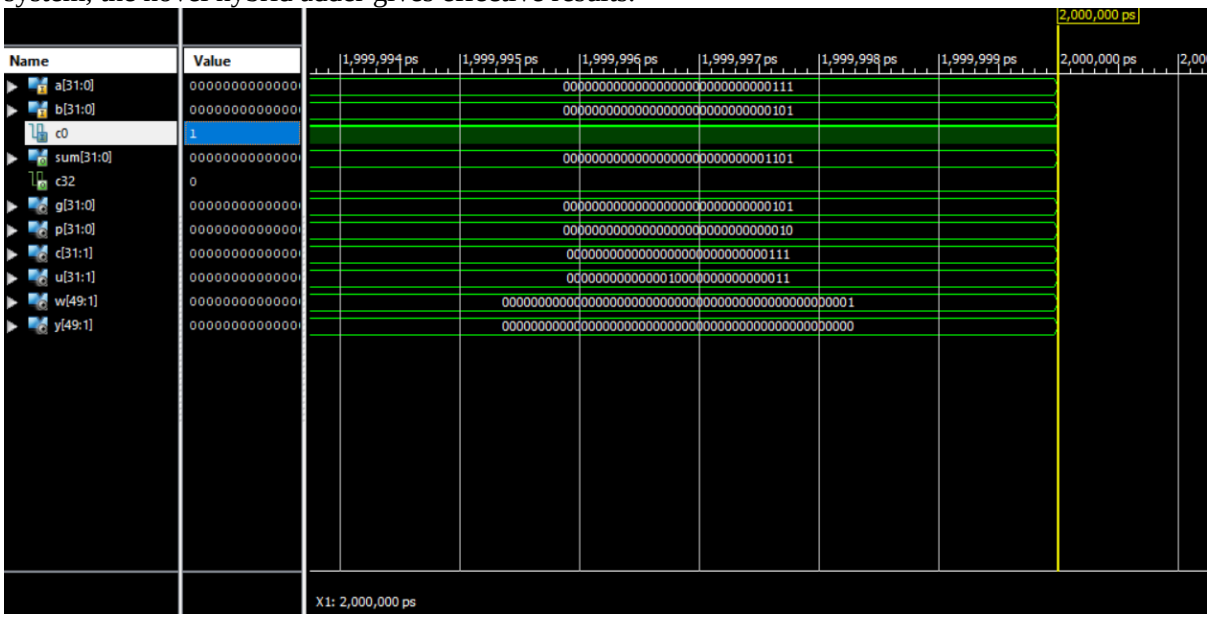

Fig. 6: Output Waveform of Novel Hybrid Adder

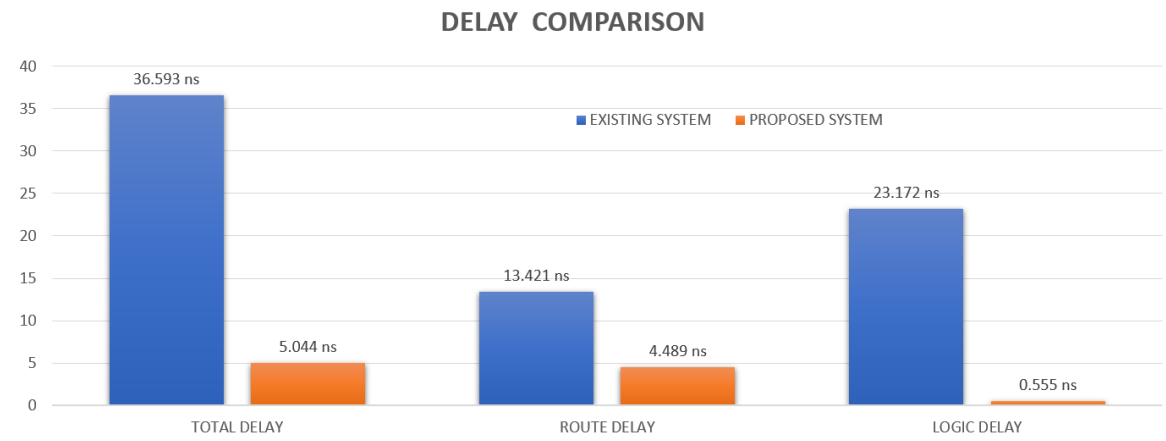

Fig. 7: Delay Comparison

The above figure (7) shows the delay comparison graph of Novel Hybrid Adder. In this total delay, route delay and logic delay are shown. Compared to existing system the Novel Hybrid Adder gives effective results.

Table. 1: Delay Comparison

S.NO	PARAMETER	EXISTED VALUE	PROPOSED VALUE
1	Total Delay	36.593ns	5.044 ns
2	Route Delay	14.295 ns	4.489 ns
3	Logic Delay	23.172 ns	0.555 s

VI. CONCLUSION

Design of high speed and low cost Novel Hybrid Adder for VLSI applications research work is done in this paper. Both multiplication and addition plays major role in DSP. Novel adder is implemented initially to occupy less area and to increase the speed of the system. Xilinx software is utilized to simulate the design. At last it can conclude that Novel adder gives effective output from simulation results.

VII. REFERENCES

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