DESIGN OF A 2-BIT MAGNITUDE COMPARTOR USING MULTIPLEXER USING PTL

Sk.Yasmeen[1], B.Vamsi [2], K.Gopinadh[2], D.Madhu krishna[2], K.Vishnu[2]

1 Assistance Professor, Dept. of ECE, Geethanjali Institute of Science and Technology, Andhra Pradesh.

2 UG Students, Dept. of ECE, Geethanjali Institute of Science and Technology, Andhra Pradesh.

Abstract

Design of a 2-bit binary Magnitude Comparator (MC) is presented in this research. The proposed MC has been designed using Conventional CMOS (CCMOS) logic, Pass Transistor Logic (PTL). The design is simulated along with 5 other existing MC designs to carry out evaluation and comparison. The proposed 2-bit MC displayed satisfactory level of improvement in speed and power. For this reason, significant enhancement in Power Delay Product (PDP) could have been attained. Due to the significant enhancement in performance, the proposed MC can be considered as a highly effective alternative to the existing MC designs. The rapid changes in circuit design have bring about various design methodologies for VLSI circuit implementation such as CCMOS, PTL, Transmission Gate Logic (TGL) etc. For this reason, various MC designs have been invented. PTL 2-bit MC is implemented using 40 transistors. PTL based design has a major disadvantage: voltage degradation. This voltage degradation problem becomes quite severe in lower CMOS technology nodes. For this reason, designs solely implemented using PTL without swing restoring transistors have become quite limited nowadays. This voltage degradation leads to another major problem: weak drive power. Due to various issues related to PTL, new designs have emerged.

Keyword: Multiplexer, Magnitude Comparator, CMOS, PTL, Tanner Eda

1. Introduction

An increase in the level of integration in modern Very Large-Scale Integration (VLSI) technology has rendered possible integration of many complex components in a single chip. Moreover, an analog circuit technique in the front-end wireless communication demand for a digital domain to save power. In most of these applications, multipliers have been an obligatory component and determine overall circuit performance with respect to speed, power consumption and size. Hence, the goal of this research work is formulated to design a comparator with less delay, low power consumption and compact area. In general, the performance of comparator in terms of delay, power consumption and area can be improved by two methods. First one is based on efficient implementation of comparator function, whereas another relies on proper selection of logic style for its implementation. There have been various multiplication methods for realizing the low power and high-speed comparator introduced in the last few decades. However, in these multiplication techniques, the intermediate computation involved in the comparator operation reduces the speed exponentially in accordance with the width of the comparator input bit. This becomes a critical issue for a higher number of input bits. But this issue can be mitigated by the addition of partial products in parallel, which is adopted from mathematics-based multiplication. Hence, these 2 works explore possible techniques on an existing comparator for the better performance. As stated earlier, the logic styles used for realizing the multipliers have significant influence on the speed, size, and power consumption and wiring complexity. Numerous logic styles in the classes of static Complementary Metal Oxide Semiconductor (CMOS), dynamic, transmission gate, Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) logic are discussed in the literature. Among them, GDI is considered in this research

work due to its merits of low power consumption and implementation of any functions with low transistor count. However, the gates based on this logic are suffered from a low output voltage due to the threshold voltage drop. This has motivated us to propose an improved set of gates that operate with merits of full swing without increasing the fabrication complexity with the possibility of implementing with less transistor count. Based on these gates and adders in mind, new compressors and parallel adders shall be designed. Further, the comparator shall also be realized with the help of these designs.

To propose the gates namely, AND, OR XOR and XNOR with full swing GDI logic and to extend the designed gates for implementing the full comparator designs. To improve the performance of parallel adders by implementing those using full swing GDI gates and comparator. To propose comparator architecture with less delay, low power consumption and small area using the concepts with full swing GDI logic.

2. Literature Survey

Lubaba, Samiha, et,al,(2020)[1], proposed design showed best performance in case of delay and Power Delay Product (PDP) which proved the effectiveness of the design, Moreover, power consumption of the design was also low which makes it highly usable for portable devices that requires low-power consumption.Gao, Mingming, et,al,(2021)[2], proposed a 1-bit comparator architecture in an optimized and efficient manner was suggested to bring a new phase of comparator circuit based on QCA, and then a novel 2-bit comparator structure was offered. The simulation and functionality of proposed comparators have been examined by the QCA designer tool, and comparison with formerly designs shows a high degree of compactness and consistent performance of proposed designs. Proposed 1-bit and 2-bit QCA comparators exhibit a delay of 0.75 and 2.75 clock cycle, occupy an active area of 0.04 and 0.19 μm2, and use 31 and 125 QCA cells, respectively.Paramasivam, K., N. Nithya, and A. Nepolean , et,al,((2021)[3] proposed 2-bit magnitude comparator was verified by theoretical analysis and SPICE simulations. The area on-chip and power analysis were performed, and the results were compared with conventional CMOS logic and threshold logic-based magnitude comparator. Sorwar, Afran,(2020) [4] proposed 2-bit MC displayed satisfactory level of improvement in speed and power. For this reason, significant enhancement in Power Delay Product (PDP) could have been attained. Due to the significant enhancement in performance, the proposed MC can be considered as a highly effective alternative to the existing MC designs.Machupalli, Madhusudhan Reddy,(2022) [5] proposed 2-bit comparator circuit occupies less amount of area on the silicon chip and consumes low power when compared to the existing magnitude comparators.Bhattacharjee, Soumik,(2021) [6] proposed comparator has been designed using DSCH 3.5 and simulations are done on Microwind 3.5 via 0.12 μ technologies. This comparator shows a power consumption of 31.746μW using 36 transistors. The proposed design exhibits a full adder logic-based comparator with less power consumption and transistor count as compared to those in recent literature.Otynshy, Dinmukhamedali,(2022) [7] proposed 1-bit digital comparator was CMOS-compatible meaning that it can be fabricated using the existing technologies. Also, to reduce the fabrication complexity of the proposed device, thermo-optic modulation was employed as the primary light modulating technique. The 1-bit digital comparator is tested at 0.5 Mbps. The study concludes with suggestions on design improvements and potential application in photonic computing. Bhuyan, Muhibul Haque,(2021) [8] this paper have reported the design process of a 4-bit comparator circuit, and have provided the simulation results at 3 CMOS technology nodes, like 90 nm, 65 nm, and 45 nm. They9 obtained improved performances in terms of surface area requirement, power dissipation, and propagation delay of the circuit at these three nodes. This article

gives an overview of the comparator circuit design.Bosu, Surajit, and Baibaswata Bhattacharjee,(2022) [9] In this paper, a design of a frequency encoded di bit-based 2-bit comparator is devised using reflective semiconductor optical amplifier (RSOA) and add/drop multiplexer (ADM). Encoding of a signal is necessary for long-range transmission. So we have adopted frequency encoding because it has been proven to be efficacious in long-range transmission.Gupta, Mangal Deep, and Rajeev Kumar Chauhan,(2021) [10] proposed to estimate the worst-case performance in terms of delay and power for binary comparator circuits. It combines the advantages of the simulation-based method for power estimation and dynamic timing analysis (DTA) techniques for timing analysis. This work also extends to 20, 16, 14, 10, and 7-nm FinFET technology. The comparator circuits are simulated on the Pyxis Schematic tool using Mentor GraphicsGudivada, Gudivada, A. Arunkumar, and Gnanou Florence Sudha,(2021) . [11] proposed a 2n-bit comparator architecture, to achieve the objective, 1-bit stack-type and 4-bit tree-based stack-type (TB-ST) comparators are proposed using QCA. Then, two tree-based architectures of 4-bit comparators are arranged in two layers to optimize the number of quantum cells and area of an 8-bit comparator. Thus, this design can be extended to any 2n-bit comparator. Simulation results of 4-bit and 8-bit comparators using QCA Designer 2.0.3 show that there is a significant improvement in the number of quantum cells and area occupancy.Chakrabarty, R,(2021) [12] This paper has focused on creating an area efficient QCA comparator circuit and a comparative study of area consumption with the previously made designs. The designed comparator circuit is the most area-efficient design as it is made up of minimum possible number of cells. A comparator is used in equality testers and many other digital communications The circuit proposed in this paper was a three layered circuit which can alternatively be used to realize the basic logic gates. The circuit can also be used as an alternative to the majority and universal gates in QCA.Askarian, Asghar, and Fariborz Parandin et,al,,(2022) [13] proposed the finite difference time domain (FDTD) procedure based on Yee's Algorithm is used to compute the propagation of optical waves in this structure. The FDTD simulation results of suggested 1-bit AOCMP indicate that the minimum and maximum values of the normalized power at ON and OFF states for output ports..Munratiwar, Shubham, Y. Saikrishna, and V. Jyothi,(2022) [14] proposed a design of 8-bit comparator which compares 8 bits of two binary data. This 2bit comparator is slightly different from conventional comparators, which can be built with 2 bit comparators using XNOR gates or by neglecting the logic for greater or lower output; that result in reduction of gates and area. The simulations of the comparator can be done using Verilog code in Xilinx tool and analyzing its performance for various inputs in the same way a security password circuit and the cascading circuit are design as a application using proposed 8-Bit comparator.Haron, Adib,(2020) [15] proposed 2-bit comparator is used in image processing for difference detection, and its efficiency is proved by image quality parameters. The post-layout simulations are performed for the 1-bit to 16-bit structures under TSMC 90 nm technology. The extracted results express a PDP with an average difference of 9.59% between the regular and post-layout modes. Also, the proposed 16-bit comparator is embedded in a pad with a total area of 4331.25 μm2. The designed magnitude comparators are key components in digital signal processors (DSPs).

3. Proposed Methodology

Pass transistor logic is a crucial logic style to design the integrated circuits because it uses less transistors, runs faster, and requires less power. By eliminating redundant transistors, it reduces the count of transistors used to make different logic gates. PTL uses N number of transistors instead of 2N, and, it has no static power consumption which makes it more powerful and successive logic style among all available logic styles. PTL is bidirectional in nature. By using this technique, the combinational logic gates like AND, OR, and EX-OR are designed using four transistors, whereas six

transistors are used for OR and AND logic gates and for EX-OR gate the transistor count is 8, using CMOS design [9]. Hence, the PTL is an effective technique to reduce the transistor count and to achieve less power consumption with high-speed performance as shown in Figure 1.

In other logic family's input is applied to gate terminal of transistor, but in PTL it is also applied to source/drain terminal. PTL circuits behave as switches use either NMOS transistors or parallel pair of NMOS and PMOS transistor called transmission gate. In this design the width of PMOS is taken equal to NMOS so that both the transistors can pass the signal simultaneously in parallel.

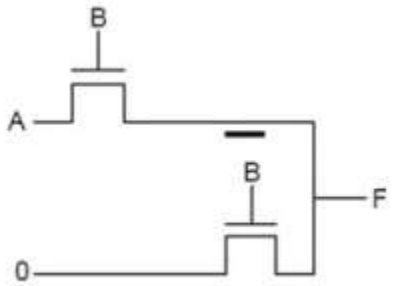

Figure 1. The basic PTL cell

The Pass transistor logic is required to reduce the transistors for implementing logic by using the primary inputs to drive gate terminals, source and drain terminals. In complementary CMOS logic primary inputs are allowed to drive only gate terminals. Figure below shows implementation of AND function using only NMOS passes transistors. In this gate if the B input is high the left NMOS is turned ON and copies the input A to the output F. When B is low the right NMOS pass transistor is turned ON and passes a '0' to the output F. This satisfies the truth table of AND gate reproduced in Figure 2. The major advantage of pass transistor logic is that fewer transistors are required to implement a given function. To illustrate this, consider the implementation of AND gate using complementary CMOS logic. If we compare this with the same AND gate implementation using pass transistor logic the number of transistors required are four including the two-transistor required to invert the input B. Another advantage of pass transistor logic is the lower capacitance because of reduced number of transistors. As discussed NMOS devices are effective in passing strong '0' but it is poor at pulling a node to VDD. Hence when the pass transistor pulls a node to high logic the output only changes upto VDD–VTh. This is the major disadvantage of pass transistors.

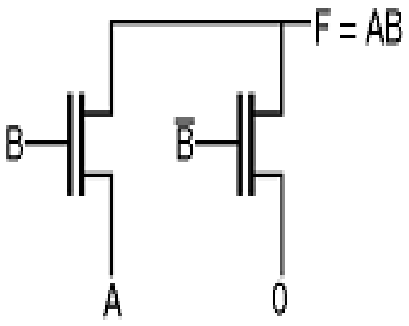

Figure 2. ANG gate using PTL.

Figure 3 shows the implementation of XOR function using NMOS transistors only. In this gate if the B input is high the right NMOS is turned ON and copies logic 1 to F and this operation does not affect by 'A' input. When B is low the left NMOS is turned ON the logic of 'A' is copied to the output F.

Figure 4 shows the implementation of XNOR function using NMOS transistors only. In this gate if the B input is low then right NMOS transistor is ON, and the inverted logic value of A is copied to the output F. When B input is high left NMOS transistor is ON and the logic value of A is copied to the output F, which satisfies the truth table of the XNOR gate.

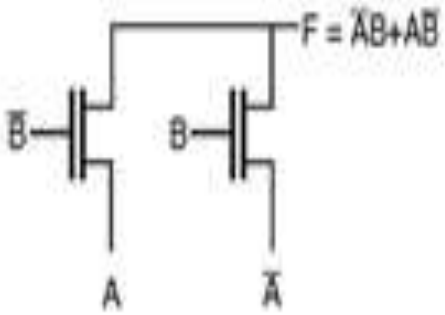

Figure 3. XOR using PTL.

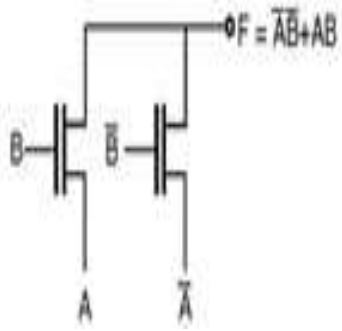

Figure 4. XNOR using PTL.

A magnitude comparator as shown in Figure 5 is an electronic circuit or a device that compares two binary numbers to determine their relative magnitudes (which one is greater than the other, or if they are equal). In other words, it is a digital circuit that compares the size of two binary numbers and produces an output indicating the result of the comparison. The magnitude comparator can be built using logic gates such as AND, OR, and NOT gates. The circuit compares the two binary numbers bit-by-bit, starting from the most significant bit (MSB) and working its way down to the least significant bit (LSB). The comparator produces a "greater than" or "less than" output based on the results of the bit-by-bit comparison. If the two numbers are equal, the output of the comparator is "equal."

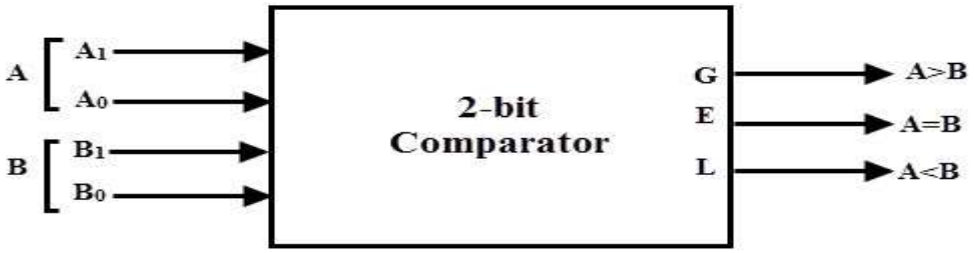

Figure 5. Magnitude Comparator

Figure 6 shows the comparator using 2to1 multiplexer diagram. Here, 2to1 multiplexer is developed using PTL logic. The operation of a magnitude comparator can be explained using a simple example of comparing two 2-bit binary numbers (A1 A0 and B1 B0). The comparison starts by comparing the most significant bits (MSBs) of the two numbers (A1 and B1) and working its way down to the least significant bits (LSBs) (A0 and B0). The comparison is done by subtracting one number from the other (A - B) and checking the result. If the result is positive, it means A is greater than B. If the result is negative, it means B is greater than A. If the result is zero, it means A and B are equal. The block diagram of a 2-bit magnitude comparator can be divided into three parts: the XOR gate, the AND gate, and the NOT gate. The XOR gate compares the MSBs of the two numbers (A1 and B1). If they are equal, the output of the XOR gate is 0, which means the two numbers are either equal or have the same magnitude. If they are not equal, the output of the XOR gate is 1, which means one number is greater than the other. The AND gate compares the outputs of the XOR gate and the A0 > B0 signal (which is produced by subtracting B0 from A0 and checking the result). If both inputs are 1 (i.e., the MSBs are not equal and A0 is greater than B0), the output of the AND gate is 1, which means A is greater than B. The NOT gate produces the A0 < B0 signal by negating the A0 > B0 signal. If A0 is less than B0, the output of the NOT gate is 1, which means B is greater than A.Finally, the two output signals (A > B and B > A) are combined with the equality output signal to produce the final output of the comparator. Magnitude comparators are widely used in digital circuits, such as microprocessors, to perform operations such as sorting, searching, and sequencing.

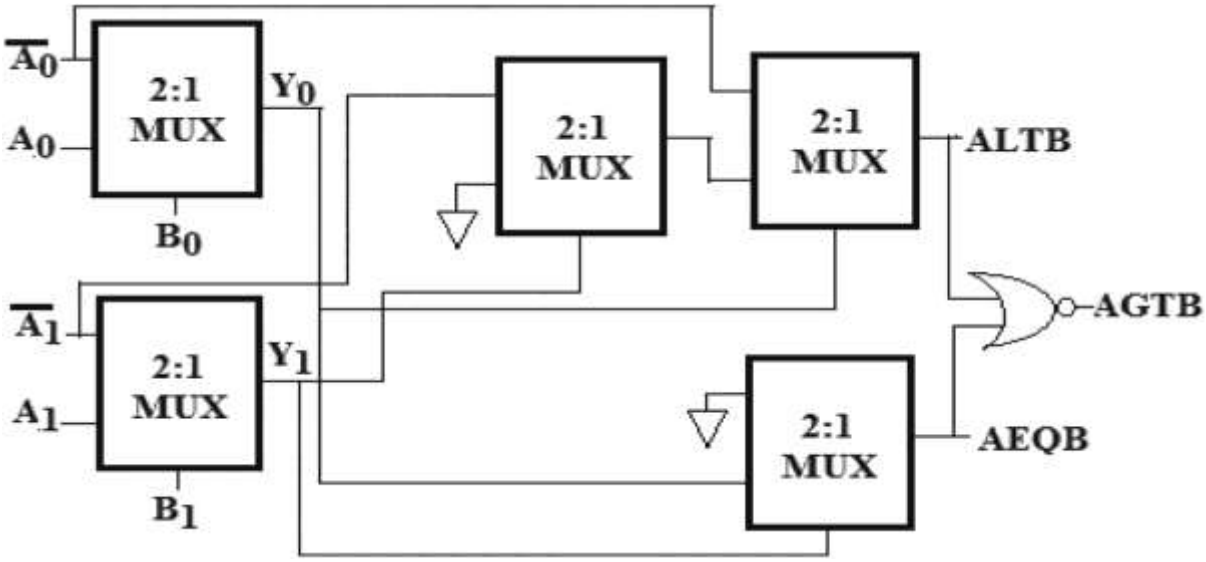

Figure 6. Comparator Design using mux.

4. Results and Discussion

The simulation will do in the Tanner EDA tool. Different PTL logic gates schematics and power and Area Results displayed in below.

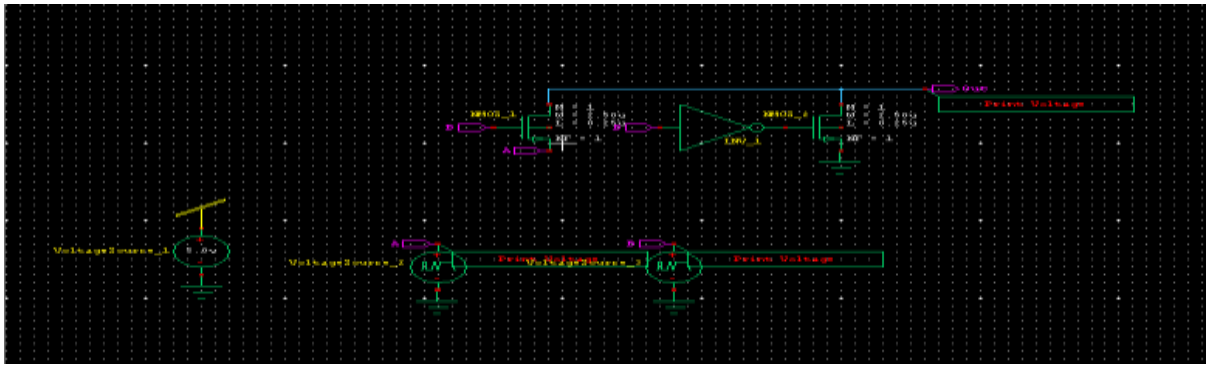

Figure 7. AND gate schematic.

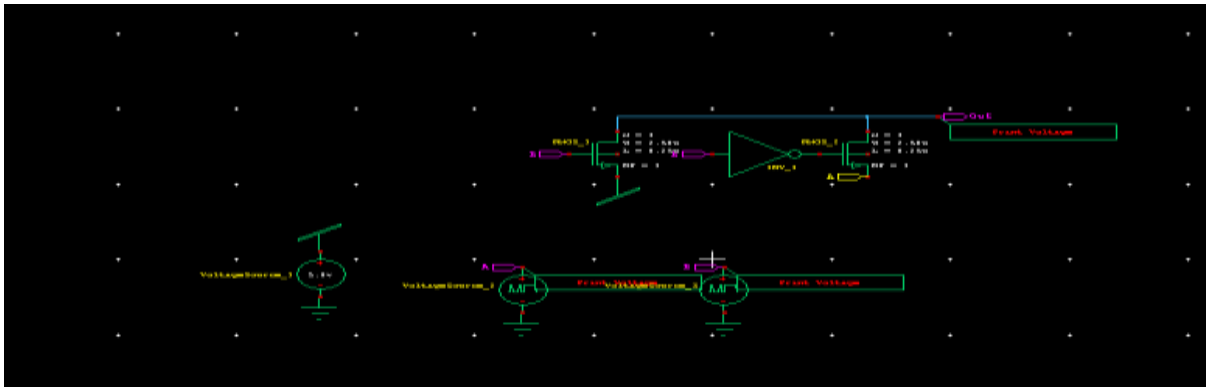

Figure 8. OR gate schematic.

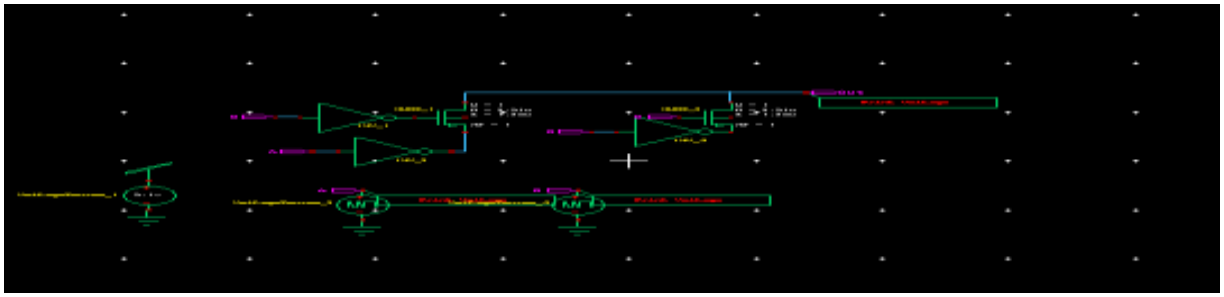

Figure 9. NOR gate schematic.

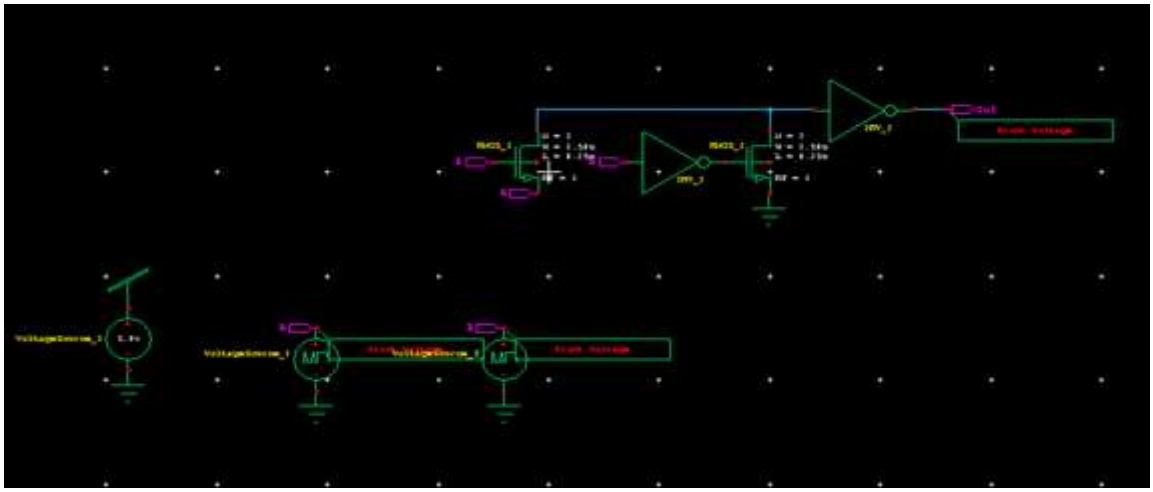

Figure 10. NAND gate schematic.

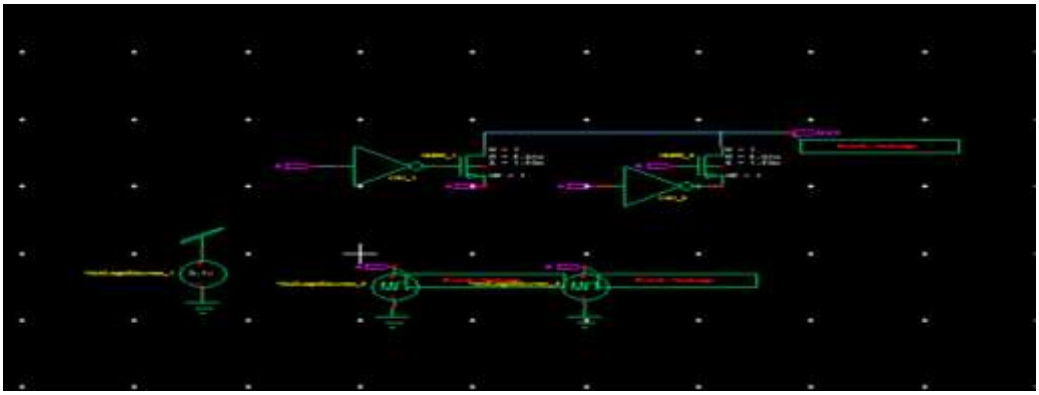

Figure 11. NAND gate schematic.

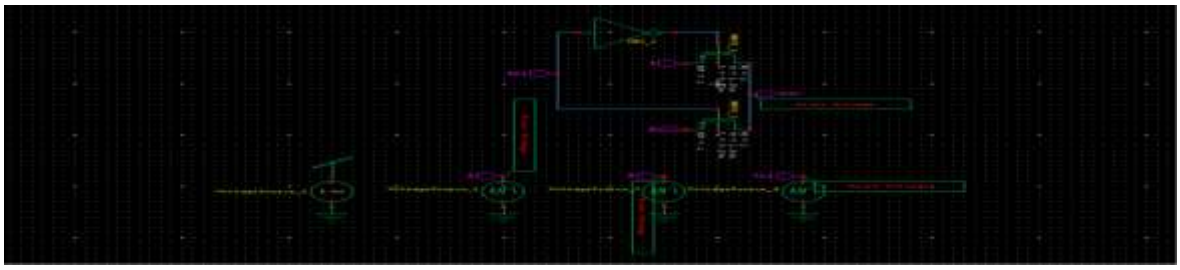

Figure 12. Mux 2to1 schematic.

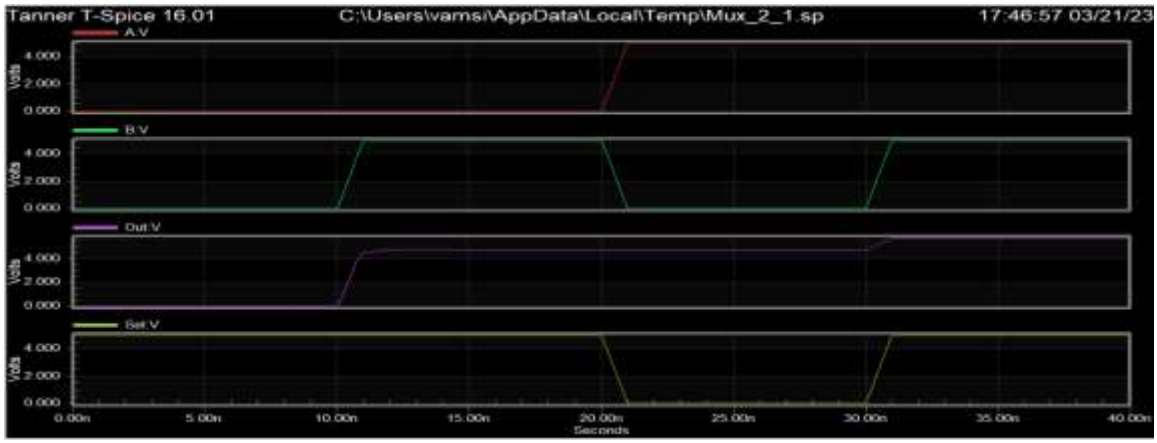

Figure 13. Mux 2to1 output waveform.

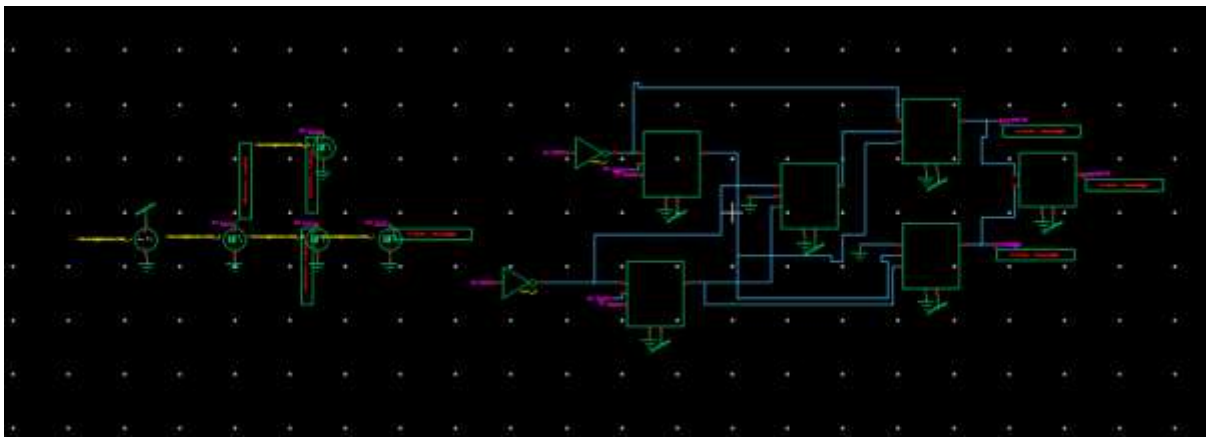

Figure 14. Comparator schematic.

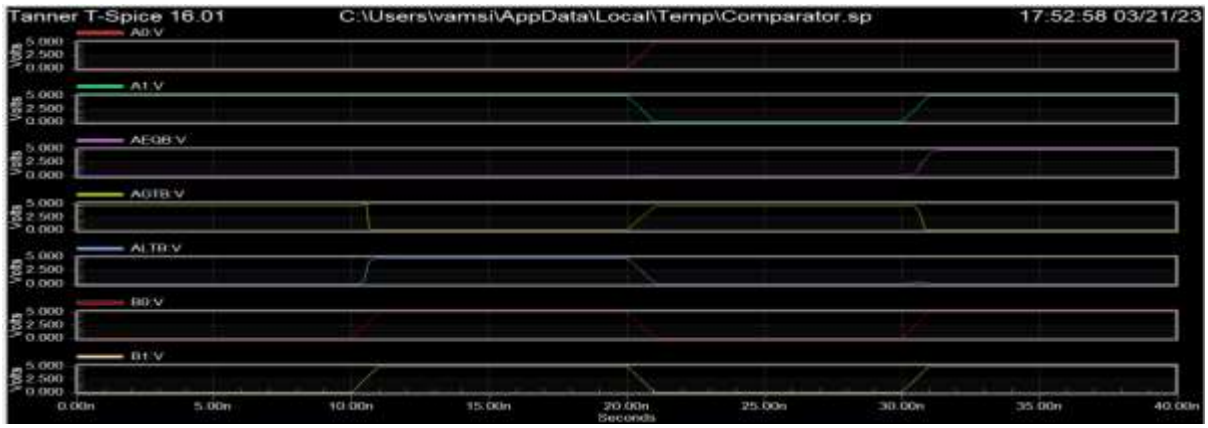

Figure 15. Comparator output waveform.

Table 1. Comparison Table

Technology	Area	Power (micro watts)
CMOS (existing)	108	22.4
PTL (Proposed)	30	0.5

5. Conclusion

A 2-bit MC design using PTL and CCMOS technique is presented in this research. The design comprised of PTL technique-based VLSI circuits for input terminals whereas CCMOS logic based complex VLSI circuit have been placed for output signals. The design in implemented and compared with various other MC design to show the performance evaluation of the design. The design displayed significant enhancement in PDP and delay while maintaining quite satisfactory power. As a result, the proposed MC design is quite suitable for present day microprocessor design.

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