A LOW POWER BINARY SQUARE ROOTER USING REVERSIBLE LOGIC

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Abstract

Square root is a vital mathematical operation which has a lot of applications. Square rooters are used in computer graphics, global positioning system (GPS), digital signal processing (DSP) computations, mathematical calculations, and data processing. In the present world of developments in various fields, the main novelty in the field of VLSI is Low Power. To attain low power Reversible logic is used in this design. In Irreversible logics, the amount of output port and input ports are not uniform and therefore they will be a loss of information bits. In restoring method more hardware resources are required whereas in non-restoring method it consumes less hardware compared to restoring method. Hence non-restoring algorithm is preferred. Many hardware architectures for digit-by-digit square root calculation using irreversible logic have been proposed. There are many reversible logic circuits that are used for the computation. Power reduction can also be done using array based arithmetic computation. Reversible logic is used to design hardware realization of non-restoring algorithm for computation of square root. Power obtained was high.The binary square rooter is designed and implemented using RCSM (Reversible Controlled Subtract Multiplexer). For further development such as number of quantum cost, garbage outputs and the constant inputs, binary square rooter is implemented using SRG (Samiur Rahman Gate). Binary square rooter using non-restoring algorithm is designed using both SRG and conventional approach.

Keywords: Binary square root, Reversable logic gates, Reversible Controlled Subtract Multiplexer.

1.Introduction

Reversible logic has presented itself as a prominent technology which plays an imperative role in Quantum Computing. Quantum computing devices theoretically operate at ultrahigh speed and consume infinitesimally less power. Research done in this paper aims to utilize the idea of reversible logic to break the conventional speed-power trade-off, thereby getting a step closer to realize Quantum computing devices. To authenticate this research, various combinational and sequential circuits are implemented such as a 4-bit Ripple-carry Adder, (8- bit X 8-bit) Wallace Tree Multiplier, and the Control Unit of an 8-bit GCD processor using Reversible gates. The power and speed parameters for the circuits have been indicated, and compared with their conventional non-reversible counterparts. The comparative statistical study proves that circuits employing Reversible logic thus are faster and power efficient. The designs presented in this paper were simulated using Xilinx 9.2 software.Reversible logic is widely used in low power VLSI. Reversible circuits are capable of back- computation and reduction in dissipated power, as there is no loss of information. Basic reversible gates are employed to achieve the required functionality of a reversible circuit. The uniqueness of reversible logic is that, there is no loss of information since there is one-to-one correspondence between inputs and outputs. This enables the system to run backwards and while doing so, any intermediate design stage can be thoroughly examined. The fan-out of each block in the circuit has to be one. This project focuses on implementation of reversible logic circuits in which

main aim is to optimize speed of the design. A Reversible adder is designed using basic reversible gates. Using this adder, an 8-bit reversible ripple-carry adder is devised and then compared with the conventional 8-bit adder in terms of speed, critical paths, hardware used. Then using the same reversible adder, a Wallace tree multiplier has been implemented, and compared with the conventional Wallace tree multiplier. With the known fact that sequential circuits are the heart of digital designing, the design for the control unit of a reversible GCD processor has been proposed using Reversible logic gates. Reversible Logic is becoming more and more prominent technology having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and Optical Computing. Reversible logic has emerged as one of the most important approaches for the power optimization with its application in low power VLSI design .In contrast to conventional gates, reversible logic gates have the same number of inputs and outputs, each of their output function is equal to 1 and their fan-out is always equal to 1. It is interesting to compare both reversible and conventional gates. LITERATURE

2. Literature Survey

Calculating square root is an important mathematical operation which has wide applications. The design of square rooter in hardware needs to achieve low power, low area and high speed. Often there can be a trade-off among the three metrics. As the current technology aims for low power, designs require major architectural modification. This paper presents a low power binary square rooter using reversible logic. It uses reversible logic to achieve low power. The binary square rooter is designed and implemented using RCSM (Reversible Controlled Subtract Multiplexer). For further development such as number of quantum cost, garbage outputs and the constant inputs, binary square rooter is implemented using SRG (Samour Rahman Gate). Binary square rooter using non-restoring algorithm is designed using both SRG and conventional approach. Simulations are carried out using Model Sim software and the power is obtained using Synopsys Design Compiler The power obtained for SRG and conventional technique are compared. The gate count has been reduced to 35 from 75. Power improvement of 20% obtainedN. Krishna, V. Murugappan, R. Harish, M. Midhun and E. Prabhu (2017)[3],Reversibility is among the rapidly evolving areas of system design, where the design has ideally zero power dissipation. Considerable research and designs have been developed in this field and the recent designs of MACs (Multiplier and Accumulators) and memory elements in reversible logic are still a budding field of research. Reversible logic is a very promising choice for quantum computational systems, DNA computation and other Low Power digital system designs. Here, we propose three novel reversible Non-Linear Shift Register (NLFSR) designs. L.Yamin,C.Waning,(1997)[4],The square root operation is hard to implement on FPGAs because of the complexity of the algorithms. In this paper, we present a non-restoring square root algorithm and two very simple single precision floating point square root implementations based on the algorithm on FPGAs. One is low-cost iterative implementation that uses a traditional adder/subtracter. The operation latency is 25 clock cycles and the issue rate is 24 clock cycles. The other is high-throughput pipelined implementation that uses multiple adder/subtracters. The operation latency is 15 clock cycles and the issue rate is one clock cycle. It means that the pipelined implementation is capable of accepting a square root instruction on every clock cycle.T. Sutiono (2011) [5] 793–8201.This paper proposes an efficient strategy to implement modified non restoring algorithm based on FPGA in gate level abstraction of VHDL, which adopt fully pipelined architecture. A new basic building block is called controlled subtract-multiplex (CSM) is introduced. The main principle of the proposed method is similar with conventional non-restoring algorithm, but it only uses subtract operation and append 01, while add operation and append 11 is not used. The proposed strategy has conducted to implement FPGA successfully, and it is offer an efficient in hardware resource. Haritha

and S. R. Ramesh, 2017 Roorkee, (2017) [6], Exact circuits produce accurate results but consume more power and area. Approximation is done to reduce the high consumption of area and power at the cost of accuracy. An array-based approximate arithmetic computing model (AAAC) is used for the reduction of error occurring in approximate binary arithmetic circuits. Although the model provides a trade-off between power, area and accuracy, these parameters can be improved further. The proposed model in this paper uses reduced number of truncated bits and a different compressor architecture for this improvement. L. Yamin, C. Warming,(2018) [7] We present a new non-restoring square root algorithm that is very efficient to implement. The new algorithm presented here has the following features unlike other square root algorithms. First, the focus of the "non-restoring" is on the "partial remainder", not on "each bit of the square root", with each iteration. Second, it only requires one traditional adder/subtracter in each iteration, i.e., it does not require other hardware components, such as seed generators, multipliers, or even multiplexors. Third, it generates the correct resulting value even in the last bit position. Next, based on the resulting value of the last bit, a precise remainder can be obtained immediately without any correction or addition operation. And finally, it can be implemented at very fast clock rate because of the very simple operations at each iteration. We illustrate two VLSI implementations of the new algorithm. One is a fully pipelined high- performance implementation that can accept a new square-root instruction each clock cycle with each pipeline stage requiring a minimum number of gate counts. The other is a low-cost implementation that uses only a single adder/subtractor for iterative operation.L. Yamin, C. Warming, (1997)[8], pp. 690–695.In this paper we present a parallel-array implementation of a new non-restoring square root algorithm (PASQRT). The carry-save adder (CSA) is used in the parallel array. The PASQRT has several features unlike other implementations. First, it does not use redundant representation for square root result. Second, each iteration generates an exact resulting value. Next it does not require any conversion on the inputs of the CSA. And last, a precise remainder can be obtained immediately. Furthermore, we present an improved version-a root-select parallel-array implementation (RS-PASQRT) for fast result value generation. The RSPASQRT is capable of achieving up to about 150% speedup ratio over the PASQRT. The simplicity of the implementations indicates that the proposed approach is an alternative to consider when designing a fully pipelined square root unit.R. Bala Kumaran and E. Prabhu, , (2016) [9], In this paper novel method for multiplier and accumulator is proposed by combining reversible logic functions and hybrid carry look-ahead adder. Modified booth algorithm produces less delay in comparison with a normal multiplication process and it also moderates the number of partial products. The Carry look-ahead adder is used for controlling the overall MAC delay. The main purpose of designing a reversible logic is to reduce the circuit complexity, power consumption and loss of information.T. Sutiono, (2011),[10] ,This paper proposes an efficient strategy to implement modified non restoring algorithm based on FPGA in gate level abstraction of VHDL, which adopt fully pipelined architecture. A new basic building block is called controlled subtract-multiplex (CSM) is introduced. The main principle of the proposed method is similar with conventional non-restoring algorithm, but it only uses subtract operation and append 01, while add operation and append 11 is not used. The proposed strategy has conducted to implement FPGA successfully, and it is offer an efficient in hardware resource.Lihui Ni, Zijin Guan and Wenying Zhu, " (2010) [11],The reversible gates, attracting people's attention increasingly, have been widely used in low- power CMOS design, optical computing and quantum computing. In many existing literatures, only the methods of constructing certain specific reversible full-adders were presented, while we proposed a general approach to construct the reversible full-adder. According to the approach, we can realize a variety of reversible full-adders flexibly with only two reversible gates and two garbage outputs, which have improvements in the gate count and garbage count and can reduce the cost of network.

Nagapavani.T and P. Rajendran, "Optimized shift register design using reversible logic" 978-1-4244-8679-3/11, IEEE(2011) [12],Now a days, reversible logic is seeking lot of attraction due to its low power consumption. Though lot of research has been done in reversible combinational circuit design, the less work has been done in sequential logic, especially shift registers. In this work we proposed a new D- flip-flop whose efficiency is shown in terms of garbage output, constant input and number of gates. Using this proposed D flip-flop, we also proposed efficient shift registers.Zhijin Guan, Wenjuan Li and Weiping Ding, Yueqin Hang, (2011)[13], In this paper, a design constructing the Arithmetic Logic Unit (ALU) based on reversible logic gates as logic components is proposed. By using reversible logic gates instead of using traditional logic gates such as AND gates and OR gates, a reversible ALU whose function is the same as the traditional ALU is constructed. The presented reversible ALU reduces the information bits' use and loss by reusing the logic information bits logically and realizes the goal of lowering power consumption. Xiyu Cheng, Zijin Guan and Wei Wang Jingling Zoe,(2012) [14].To further simplify the reversible circuit cascaded by positive/negative control (PNC) gates, new merging, moving and splitting rules of PNC gates were proposed in the paper, and these rules have been proved correct by way of logic algebra. We gave a novel simplification algorithm for reversible logic network of PNC gates by utilizing these rules. Experimental results on all 3-bit reversible functions show that our simplification algorithm is effective, it can decrease the gate count as well as the number of control bits compared to some known results, which were yielded by two excellent heuristic methods. Because the proposed rules have the generality, our simplification algorithm can be easily extended to reversible functions with a greater number of input bits. Rakshith Shaligram and Rakshith T.R,(2013) [15],A Gray Code is an encoding of integers as sequences of bits with the property that the representations of adjacent integers differ in exactly one binary position. Gray Codes have many practical applications that go beyond research interests. There are different types of gray codes: Binary reflected, Maximum Gap, Balanced, Antipodal and Non-Composite to name a few. On the other hand, Reversible logic has received great attention due to their ability to reduce the power dissipation--an important aspect of low power circuit design. Other applications include Optical information processing, DNA computing, bio informatics, quantum computation and nanotechnology. Counters have a primary function of producing a specified output sequence and are thus sometimes referred to as pattern generators. This paper proposes design of different gray code counters using reversible logic gates, to draw comparative conclusions upon their performance.

3. Proposed Methodology

The non-restoring algorithm used for the computation requires a reversible full subtractor. The square rooter is designed using Saimur Rahman gate and Feynman Gate. The functionality of the Saimur Rahman gate is a full subtractor. It is shown in Fig 1. Here the output W7 represents the borrow (BO) and W8 represents the difference (DI). The SRG gate acts as a full subtractor only if W4=0, if W4 is ≠ 0 then the gate won't act as a full subtractor. W5 and W6 acts as a garbage output. The truth table of the SR gate is given in Table.1 Let the radicand be N7N6N5N4.N3N2N1N0 with a total length of 8 bits. Since it is an 8-bit square rooter the nod of bits for the quotient is 8/2= 4(U3U2.U1U0). The implementation of 8-bit square rooter using SR and FG gates is shown in Figure 2. According to the non-restoring computation if the remainder is positive then quotient (U=1) and the difference should be carried over for the next process. If the remainder is negative, then quotient is (U=0) and the previous inputs should be carried over for the next process. So, a control unit is designed using RT reversible gate to switch between the difference (W8) and the inputs (W1). A reversible multiplex is used for all the gates to switch between the difference and the inputs. The input (W1), the difference (W8) and the quotient are given as input to the gates. The

configuration is shown in Figure 2. So, depending upon the quotient (U) the input and the difference will get switched automatically.

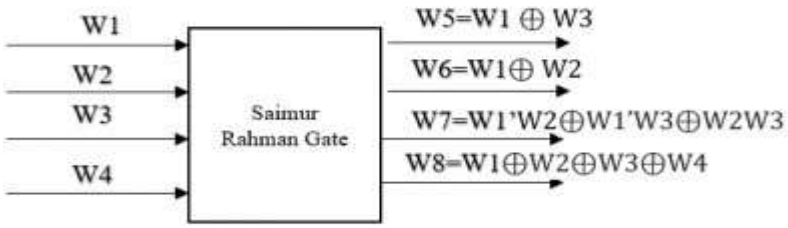

Figure 1. Saimur Rahman Gate

Table 1. Truth Table for Samiur Rahman Gate

W1	W2	W3	W4	W7	W8
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	0	0	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	1	1

3.1 Block diagram description

Thus, with these reversible gates the design is proposed for the non-restoring algorithm. The conventional design is carried upon using the irreversible gates. The basic xor, and, or, not gates are used for conventional approach. The power results of reversible and conventional design are obtained. To find the square root of a binary number is performed by digit-by-digit procedure. The algorithm is further classified into non-restoring and restoring algorithms. The restoring algorithm involves a greater number of hardware resources which in turn increases the total power of the system. Hence the non-restoring algorithm is used for the computation. The non- restoring algorithm simply uses subtraction and appending 01. In the non-restoring algorithm, the total number of bits N is divided into groups of two digits. In general, the length of the quotient is N/2. The algorithm is as follows:

Step 1: Split the number of bits N into groups of two digits.

Step 2: Subtract 1 from the left most significant group of digits. Quotient is 1 if the difference is positive and quotient is 0 of the difference is negative.

Step 3: Bring the next group of two digits. Append 01 and the previous quotient and then subtract.

Step 4: Proceed to step 2 until the end of groups of two digits.

The radicand may be a whole number (13) or may be a decimal number (2.2). If the radicand is a whole number (13) it can be represented as 1101 and if it is a decimal number 2.2 it can be represented as0010.0011… Here 0010 corresponds to 6 and 0011...corresponds to 0.4 in binary. The number of bits after the decimal can be extended to N number of bits depending upon the application

and accuracy that is required. For example, consider a binary square rooter (N7N6N5N4.N3N2N1N0). The quotient for the square rooter is U3U2.U1U0.The count of bits before and after the decimal point can be decided upon the user. For example, the square root of 13(1101) and 2.2(0010.0011) is given in figure 3. From Figure 3, the square root of 13 and 2.2 are found. The square root of 13 is approximately equal to 3.6.From the quotient 11.10(U3U2.U1U0) ,11(U3U2) corresponds to 3 and 10 (U1U0) corresponds to .6.The binary representation of .6 is 1001..The square root of 2.2(0010.0011) is approximately equal to 1.4..From the quotient 01.01, 01(U3U2) corresponds to 1 and 01 (U1U0) corresponds to .4.The binary representation of .4 is 0110..As earlier mentioned the number of bits before and after the decimal point can be decided upon the user and application. If a greater number of bits in the quotient is necessary, the bit size after the decimal point shall be increased.

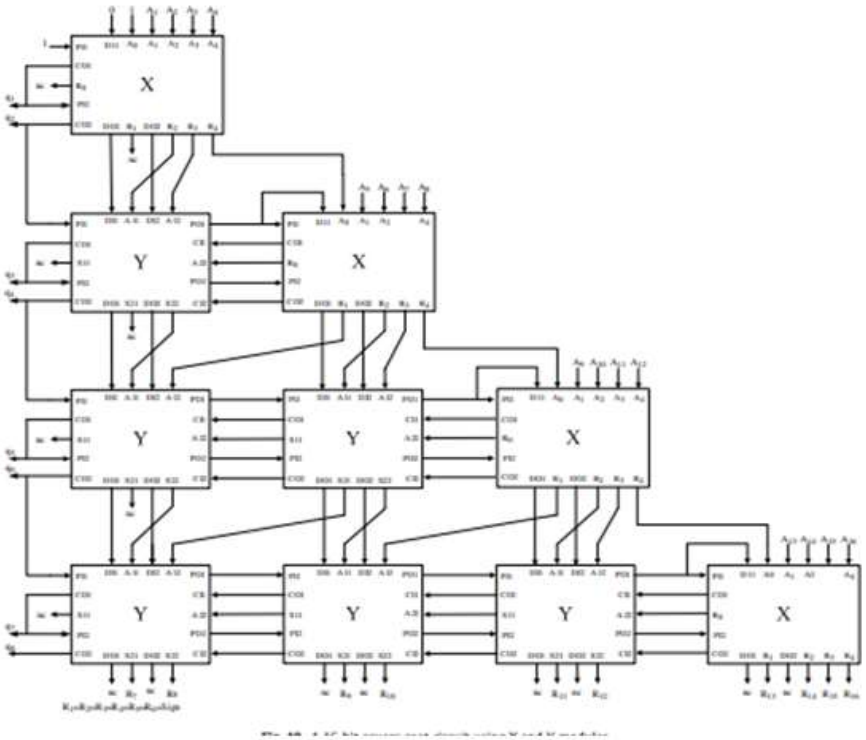

Figure 2. Design of an 8 Bit Binary square rooter

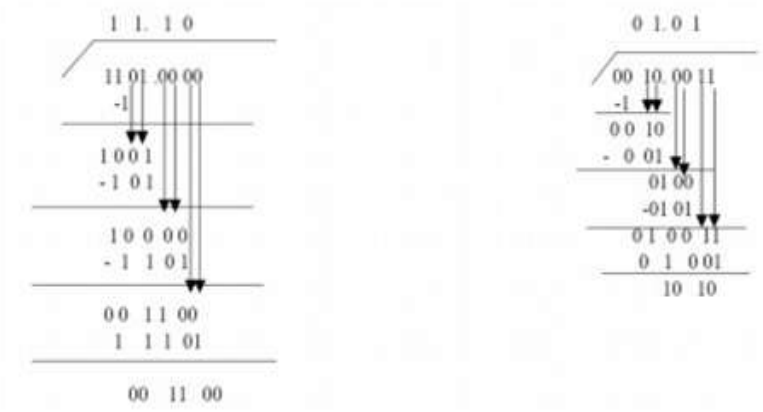

Figure 3. Non-restoring algorithm example

4. Results and Discussion

The simulation results will do by using in Vivado ISE. The timing, power and synthesis reports listed below.

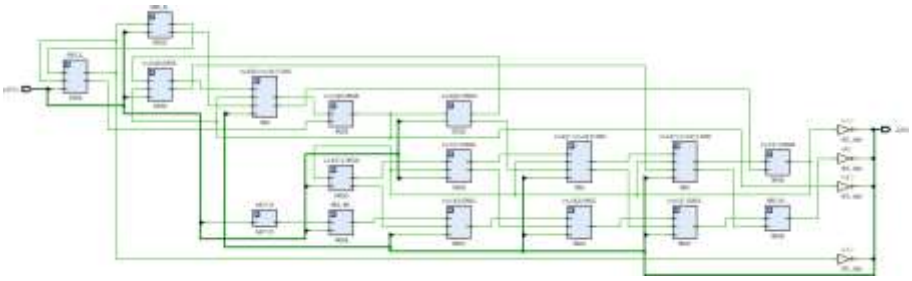

Figure 4. RTL schematic

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization...
LUT	6	47200	0.01
IO	12	170	7.06

Figure 5. Design summary

Name	Slack	Levels	Routes	High F... ^1	From	To	Total Delay	Logic Delay	Net Delay
Path 4	∞	3	2	4	p[6]	u[3]	3.101	1.841	1.261
Path 1	∞	3	2	6	p[5]	u[1]	2.930	1.859	1.071
Path 2	∞	3	2	6	p[4]	u[2]	3.034	1.957	1.076
Path 3	∞	5	2	6	p[5]	u[0]	3.088	2.051	1.037

Figure 6. Timing summary

Figure 7. Power utilization summary

Figure 8. Simulation output

Table 2. Comparison table

SI No	Area (Luts)	Power (W)	Delay (ns)
Proposed method	6	1.644	4.02
Existing Method	30	5.02	6.521

5. Conclusion

In this work, the performance of square rooter circuits can be enhanced using reversible gates and in terms of speed and power; thereby concluding that reversible designs are faster and power efficient. A low power reversible binary square rooter has been designed. The square rooter can be used in ALUs especially in DSP processors for reversible computing. Conventional approach consumes more power than the reversible computing. Also, a decrease in gate count is observed. Reversible logic design finds applications in various fields including Quantum computing, Nano-computing, optical computing, Quantum Computing Automata (QCA: study of mathematical objects called Abstract machines and the computational problems that can be solved using them), ultra- low power VLSI designing, Quantum dot cellular etc. The future of computer chips is limited by Moore's law; hence an alternative is to build quantum chips. Our future research topic is designing a new reversible gate and to implement reversible logic into a complete Quantum processor capable of ultra-high speed and infinitesimally low power computing.

References

[1]. Lindauer, Irreversibility and heat generation in thecomputing bprocess, IBM J. Res. Dev. 5 (1967) 183–191.
[2]. C.H. Bennett, Logical reversibility of computation, IBM J.Res. Dev. 17 (1973), 525–532.
[3]. N. Krishna, V. Murugappan, R. Harish, M. Midhun and E. Prabhu,"Design of a novel reversible nlfsr," 2017 International Conference on Advances in Computing, Communications and Informatics (ICACCI), Udupi, 2017, pp. 2279-2283.
[4]. L. Yamin, C. Wanming, Implementation of single precision floating point square root on FPGAs, in: Proceedings of the IEEE Symposium on FPGA for Custom Computing Machines,1997, pp 226–232.
[5]. T. Sutikno, An efficient implementation of the non- restoring square root algorithm in gate level, Int. J.Comput. Theory Eng.3 (1) (Feb. 2011) 1793–8201.
[6]. Penchalaiah, Usthulamuri, and VG Siva Kumar. "Design and Implementation of Low Power and Area Efficient Architecture for High Performance ALU." Parallel Processing Letters 32.01n02

(2022): 2150017.

[7]. S. V. G. Kumar, M. Vadivel, U. Penchalaiah, P. Ganesan and T. Somassoundaram, "Real Time Embedded System for Automobile Automation," 2019 IEEE International Conference on System, Computation, Automation and Networking (ICSCAN), Pondicherry, India, 2019, pp. 1-6, doi: 10.1109/ICSCAN.2019.8878820.

[8]. H. Haritha and S. R. Ramesh, "Design of an Enhanced Array Based Approximate Arithmetic Computing Model for Multipliers and Squarers," 2017 14th IEEE India Council International Conference (INDICON), Roorkee,2017, pp. 1-5.

[9]. L. Yamin, C. Wanming, A new non-restoring square root algorithm and its VLSI Implementation.

[10]. L. Yamin, C. Wanming, Parallel-array implementations of a non-restoring square root algorithm, in: Proceedings of the IEEE International Conference on Computer Design: VLSI in Computers and Processors, 1997, pp. 690–695.

[11]. R. Bala Kumaran and E. Prabhu, "Design of high-speed multiplier using modified booth algorithm with hybrid carry look-ahead adder," 2016 International Conferenceon Circuit, Power and Computing Technologies (ICCPCT), Nagercoil, 2016, pp. 1-7.

[12]. T. Sutikno, An efficient implementation of the non- restoring square root algorithm in gate level, Int. J.Comput. Theory Eng. 3 (1) (Feb. 2011) 1793–8201.

[13]. A.V. AnanthaLakshmi, Gnanou Florence Sudha, "Design of a reversible floating-point square root using modified non-restoring algorithm", in Microprocessors and Microsystem, Vol.50, pp.39-53, May 2017.

[14]. Md. Samiur Rahman, Sajjad Waheed, Ali Newaz Bahar, "Optimized Design of Full-Subtractor Using New SRG Reversible Logic Gates and VHDL Simulation", in International Conference on Electrical & ElectronicEngineering, Rajshahi,2015,pp.69-72

[15]. L. Gopal, N Raj, A. A. Gopalai and A. K. Singh, "Designof reversible multiplexer/de-multiplexer," 2014 IEEE International Conference on Control System, Computing and Engineering (ICCSCE 2014), Batu Ferringhi, 2014, pp. 416-420.

[16]. R. Landauer, ―Irreversibility and Heat Generation in the Computational Process‖, IBM Journal of Research and Development, 5, pp. 183-191, 1961

[17]. C.H. Bennett, ―Logical Reversibility of Computation‖, IBM J. Research and Development, pp. 525-532, November 1973.