

A Study on Semiconductor Memory Cells Using CMOS- Technologies in Digital Electronics

Rohit Kumar

Assistant Computer Operator & Networking Instructor,
Information Technology,
Central Industrial Training Institute, Siwan Bihar

Abstract

The CMOS technology is known for low threshold voltage high density and high performance. The electronic circuit or components density has increased daily in a single chip by employing VLSI design. The power consumption going to low and operating frequency achieved higher through VLSI technology. In this article, we included a brief review on digital electronic memory cell and future technology. We have mainly focused flash memory devices such as Static Random-access memory (SRAM), dynamic Random-access memory (DRAM) and Flip-flop. RAM is a very powerful components for personal computer, mobile and any electronic gadgets. The development of RAM and flip-flop in the form of memory is very important because its impacts on the performance of the programs in personal computer (PC). Now a days, all the research and development as well as normal work have been dependent on the PC performance. The speed of the PC depends on RAM and flash memory used in PC configurations. This is the main reason to study and analyzed the digital memory cell, especially RAM and flip-flop. These are various applications in VLSI digital clock system, baths, registers, microprocessors, etc., and very low power consumptions.

1. INTRODUCTION

The output of the digital circuit is in binary format. The binary means the representation of only two states. The higher value represents the one and the lower value by 0. Because of these two upper and lower values, the digital circuit has several advantages over the analog circuit. But in case of analog circuit analogue signal having the continuous signal over time [1]. So, the chance of the error in the analogue signal is higher than the digital signal. In recent time, the digital electronic circuit are used. In electronic circuit digital Memory play an important role. Digital memory means that data recorded and save in it. The format of store date is in zero and 1 form. Digital memory made of the logic gates such as AND gate, OR gate, Not gate, NAND gate, EXOR gate etc[2]. The combination of these gates makes digital electronic circuit from these logic gates.

Customize integrated circuits, especially for a specific task cleverly built circuits, known as application-specific integrated circuits (ASICs). Integrated circuits with digital logic circuitry layouts that can be changed and deal with fixed gate arrays (FPGAs) and are frequently used for prototyping and development[1,3]. Different types of memory cells, such as contextual memory and bubble memory, have been employed throughout computing technology. Metal-oxide-

semiconductor (MOS) memory cells are today's most typical type of memory cell construction. Flip-flops made of MOSFETs (MOSFETs), and MOS capacitors are both used in contemporary random-access memory (RAM). Present-day RAM uses as flip-flops and MOS capacitors. The SRAM (static RAM) memory is made from flip-flop circuits, usually used with MOSFETs. The second kind of RAM is DRAM (dynamic access memory). The DRAM works based on the charging and discharging capacitors of MOS capacitors. It can store '1 'or' 0 'in charging and discharging, respectively[4,5].

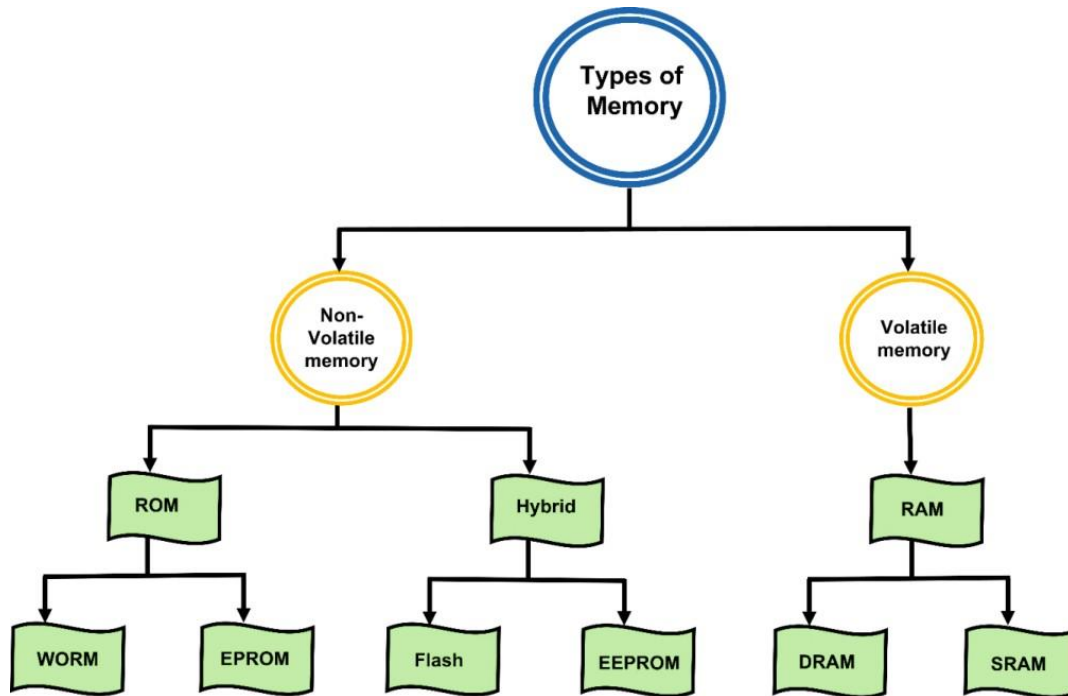


Fig.1. Semiconductor Memory Classification

However, nonvolatile memory (NVM) relies on the development of floating memory cells. The floating gate memory cells are used in read-only memory, such as erasable programmable read-only memory and electrically erasable programmable read-only memory [6,7]. The foundation of creating digital memory is a memory cell, which is made of flip-flops. Many different technologies used in producing high-density memory cells in an integrated chip, such as BJT, FET, and MOSFET, can be employed with it [8,9]. These digital memories can store the data to enable the computer. These memory cells are also utilized to store information in integrated circuits that will be utilized by users later on in the future. Repeated circuits are intelligent devices that make use of memory cells. The output is influenced by both the previous state circuits, as defined by prices, and the input's current value. These circuits need a clock or a time generator to function. The majority of modern computer programs use DRAM cells as their primary form of memory because of their reduced size and ability to deliver at the lower price

with higher storage capacity [10]. The Dynamic RAM memory able to refresh the stored information and cell's value needs to be rewritten frequently because it holds its value as a charging and discharging of MOS capacitor. It has an issue as leakage current in these capacitors. This is one factor contributing to DRAM cells' decreased speed compared to

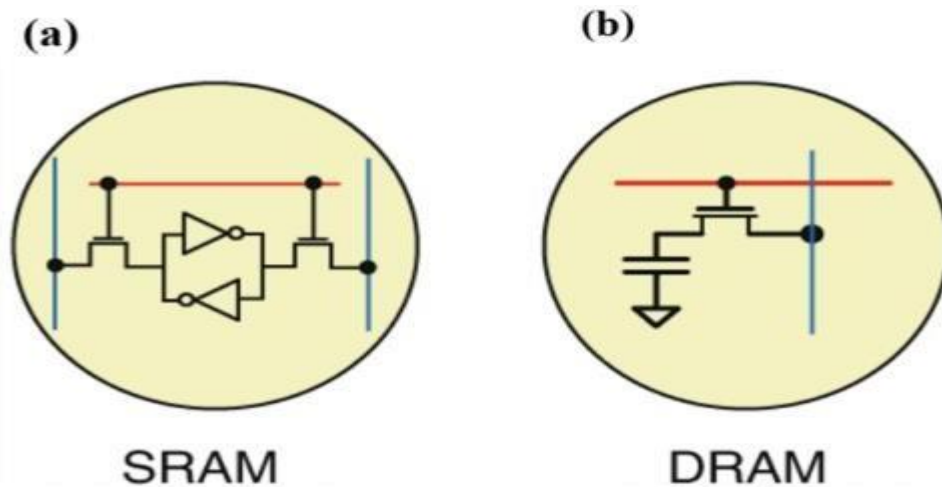


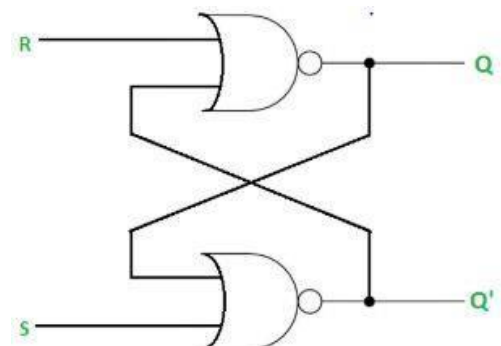
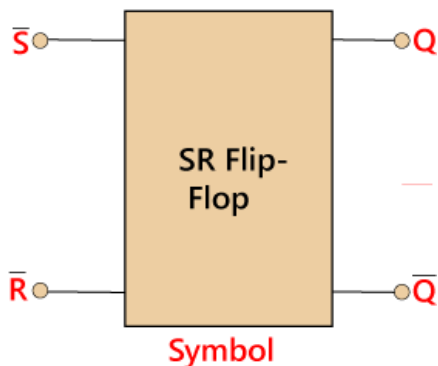
Fig.2. Schematic configuration of (a) SRAM (b) DRAM

huge SRAM cells (standing RAM). Because of this, on-chip storage found on contemporary microprocessor chips uses SRAM memory [5,11].

2. Discussion

2.1. 1 Bit Memory cell (SR flip flop):

The flip flops are a basic unit of digital memory. One flip flop store one bit of data. The basic flip-flop is known as the SR flip-flop. The SR Flip Flop store one bit of data in the form of Zero and one. It stores data in bistable of 0 and 1. It has 2 inputs SET and RESET. SET is denoted by S and RESET is denoted by R and its 1 and 0, respectively[12].



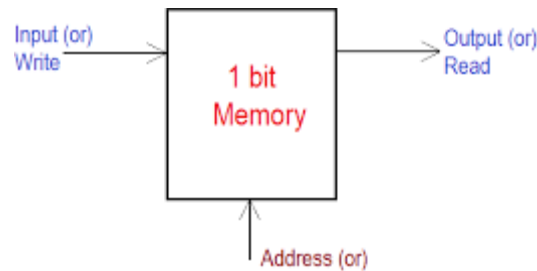


Fig.3. 1bit memory cell

- (A) $S = 1, R = 0$: set
- (B) $S = 0, R = 0$: hold
- (C) $S = 0, R = 1$: reset
- (D) $S = 1, R = 1$: not allowed

Switching from a limited combination (D) to (A) leads to an unstable state operations.

2.2.DRAM MEMORY CELL

DRAM stands for dynamic random-access memory. The DRAM Memory was first marketed in the late 1960s, about 50 years ago, and it was very likely the first memory-integrated circuit ever sold. This memory cell made of one transistor and one capacitor, make up one that repeats that is only 2 elements per cell by comparison. Through continued improvements over these 50 years, DRAM has remained the second most compact memory technology in production. DRAM is very fast and has symmetrical read and write speeds[6,7,14]. The room is in fact the lowest price per bit. Symmetrical speed, which means fast rate equals fast ride speed memory and is widely used to hold large working files. This capacitor effectively holds the value of the bit, can be charged up to high voltage, and it can be discharged to low voltage which will call a logic zero. To make it work again we will use VSS or ground and there is a small leakage path from this gate drain into the substrate. When the game is off through this reverse diode junction, here the capacitor will this charge after some finite time and follow the midpoint 0.5 volts. Let's say that finite time is 200 milliseconds in our case or 1/5 of a second. So, these memory cell capacitors need refresh to retain their memory value[9]. The standard for refreshing every drop capacitor on an IC is every 64 milliseconds or less. That's why this is called dynamic RAM. Dynamically refreshed

16 times at least each second. The charge on this capacitor, which is higher one Volt in this case, adds enough positive voltage. The advantages of DRAM are low cost, high speed and infinite memory access. The disadvantage of DRAM is its content will be lost on any power loss.

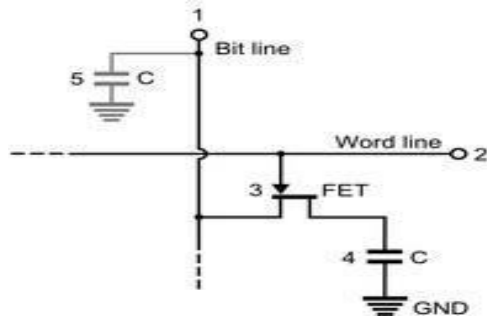


Fig.5: DRAM cell (1 transistor and one capacitor)

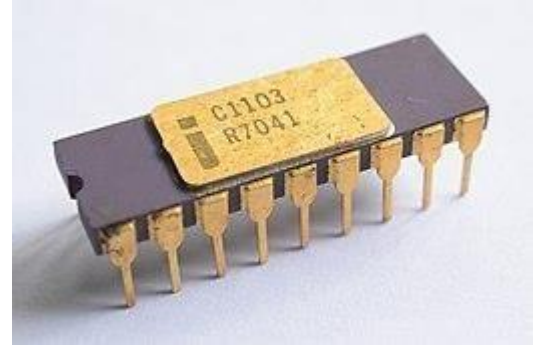


Fig 6: DRAM chip

In figure 5, you can see only one transistor and one capacitor. First, we discuss about read operation. The applied voltage $V_{dd}/2$ to charge the capacitor. If this is one, then this transistor will be on output is equal to one. If this is the voltage of the data line and if it is sent to sense amplifier. Then output will be one. In the case of write operation, the data line will be acted as the input [10]. The capacitor would have the value one. So, this capacitor would be charged. If you place a value zero here then capacitor would be discharged, so the value here would be zero. Data line would be acted as the input line. Should be one so that we can access this transaction because we can access this transistor. That is, if this is one, we can access this capacitor and output is one. This means that we have the access to this capacitor now and if word line is one then the voltage share would be if data line is one then the capacitor will have the voltage V_{dd} and if data line is zero then capacitor will have the voltage zero.

Types of DRAM

These are the types of DRAM memory:

- i. **SDRAM** (Synchronous Dynamic Random-Access Memory)
- ii. **DDR SDRAM** (Double Data Rate Synchronous Dynamic Random-Access Memory)
- iii. **ECC DRAM** (Error Correcting Code Dynamic Random-Access Memory)
- iv. **DDR2** (Double Data Rate 2 Synchronous Dynamic Random-Access Memory)

2.3. SRAM MEMORY CELL

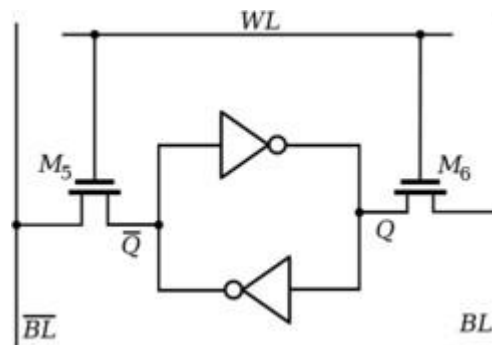


Fig.7: SRAM memory cell showing Inverter Loop as gate

SRAM stands for static random-access memory. The first SRAM in integrated circuit was sold around 1970, about 50 years ago. Means they were introduced to within a decade of the very first planner transistors integrated circuits. The bit memory uses 6 transistors, and these bits are packed together in a row and column array to make a byte word of memory as you need. The address used to access the memory are decoded so that the word line turns on these 2 transistors simultaneous[15]. Then these pair lines, true and complement are driven with your value. The drive strength is sad, so the weaker inverse inside the memory cell change to keep your new value. In SRAM, these bits can be read over and over or written over and over infinitely. The only time designers buy external SRAM integrated circuit if they need more SRAM than the microcontroller they select can hold, or it's a cheaper system cost to have it outside for some odd reason. if their application needs non-volatile as scrap, in that case the put SRAM outside. The number of chips in SRAM is more than the other RAM variants such as DRAM for the same amount of storage space which increases its manufacturing cost. Have it works in a fast manner and consumes less power. As it is, no refresh cycle is needed. Working of SRAM, we know that computer is working in binary language. So whatever input we are giving to a computer will be converted into form of zeros and ones. Similarly, the output generated by a computer will be in the binary language which is then converted into human understandable language. Now let's see how the read operation is performed in SRAM. The 2 pass transistors are turned on by applying the voltage at the address line. It can also sense the voltage difference between these bit lines. This whole operation could also be accomplished with the help of one bit line. But here we are using 2-bit lines to increase the speed of the read operation. There are mainly two types of SRAM: (i) asynchronous SRAM, it is called asynchronous SRAM because it works independently of the

system clock in CPU. (ii) Synchronous SRAM, it is synchronised with the system clock. This allows it to be more easily synchronised with any device that accesses it and reduces excess waiting time while the speed may be high[13].

3. CONCLUSION

In this paper, we investigated the operation of Dynamic Random Access Memory (DRAM) and static random-access memory. We have found that these two digital memories are essential components of electronic gadgets and computers. We have studied the detailed operation of digital memory such as SRAM and DRAM. The operation like storage of data, reading and writing from external commands to memory. We have found that the stored data in DRAM is lost when power fails. But in the case of SRAM data is safe. Let's say that finite time is 200 milliseconds in our case or 1/5 of a second. So, these memory cell capacitors need refresh to retain their memory value. The standard for refreshing every drop capacitor on an IC is every 64 milliseconds or less. Dynamically refreshed 16 times at least each second. The advantages of DRAM are low cost, high speed and infinite memory access. The disadvantage of DRAM is its content will be lost on any power loss.

4. FUTURE SCOPE

Reduce the size electronic components inside integrated chip and increase the density of transistors in it. We also go for RRAM (resistive random-access memory), because the size the RAM is in very low dimension compared to the SRAM and DRAM.

References:

1. Asai, S. (1986). Semiconductor memory trends. *Proceedings of the IEEE*, 74(12), 1623–1635.
2. Cha, S. Y. (2011). DRAM technology-history & challenges. In Proc. IEDM.
3. Spessot, A., & Oh, H. (2020). 1T-1C dynamic random access memory status, challenges, and prospects. *IEEE Transactions on Electron Devices*, 67(4), 1382–1393.
4. Rodriguez, N., Gamiz, F., & Cristoloveanu, S. (2010). A RAM memory cell: Concept and operation. *IEEE Electron Device Letters*, 31(9), 972–974.
5. Jacob, B., Wang, D., & Ng, S. (2010). *Memory systems: Cache, DRAM, disk*. Morgan Kaufmann.

6. Keeth, B., Baker, R. J., Johnson, B., & Lin, F. (2007). DRAM circuit design: Fundamental and high-speed topics (Vol. 13). John Wiley & Sons.
7. Garg, S., & Saurabh, S. (2018). Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis. *Superlattices and Microstructures*, 113, 261–270.
8. Kim, H. W., & Kwon, D. (2021). Steep switching characteristics of L-shaped tunnel FET with doping engineering. *IEEE Journal of the Electron Devices Society*, 9, 359–364.
9. Bohr, M., & Elmansy, Y. (1998). Technology for advanced high-performance microprocessors. *IEEE Transactions on Electron Devices*, 45, 620–625.
10. Spasova, M. L., Angelov, G. V., Hristov, M. H. (2012). Simulation of 1T DRAM memory cell with verilog-a model of CNTFET in cadence. *Annual Journal of Electronics*, 6(2), 1-4.
11. Bhati, I., Chang, M. T., Chishti, Z., Lu, S. L., & Jacob, B. (2015). DRAM refresh mechanisms, penalties, and trade-offs. *IEEE on Computers*, 65(1), 108–21.
12. Asthana P (2020) Analysis of dram cell designs for nanometer-scale memories
13. Asthana P. Mangesh S (2014) Design and implementation of 4T, 3T and 3T1D dram cell design on 32 nm technology. *Int J VLSI Des Commun Syst* 5(4):47
14. Gupta T, Naik P (2017) Comparative analysis of 2T, 3T and 4T dram CMOS cells. In: 2017 international conference on information, communication, instrumentation, and control (ICICIC). IEEE, pp 1–6.
15. T. Gupta and P. Naik, "Comparative analysis of 2T 3T and 4T DRAM CMOS cells", de 2017 International Conference on Information Communication Instrumentation and Control (ICICIC), 2017.
16. https://www.researchgate.net/publication/368654310_An_Industry-Institute_Collaboration_Project_Case_Study_Boosting_Software_Engineering_Education
17. https://www.researchgate.net/publication/353767742_Cyber_Growth_due_to_covid-19
18. https://www.researchgate.net/publication/368654207_Cybersecurity_Cyber_Physical_Systems_And_Smart_City_Using_Big_Data
19. https://www.researchgate.net/publication/368654289_An_Analysis_on_Cybercrime_againts_Women_in_the_state_of_Bihar_and_various_Preventing_Measures_Made_by_Indian_Government
20. https://www.researchgate.net/publication/352178529_Social_Impact_of_Cyber_Crime_A_Sociological_Analysis?_sg%5B0%5D=Jz3oHbn8qN0Im3j6X2I8rUm_ZxZmdKi7ipSyyVhq8DJfG15IbmGz94K5cFLaapVf131K2dR_kYzcuaE5kV1cJZuMfrA6cx9B-

oS6fb9Q.hzZiR9SIWGXmAe7jHQzOWTz5x3KxFz4uTgUrfHo2bbbMgHQMcHTBecBFaedLvY
j7yS5ayoTYXxs_zvtVe4Ku9g

21. https://www.researchgate.net/publication/352178441_A_Study_on_Preventive_Measures_of_Cyber_Crime?_sg%5B0%5D=PxYUuNIRpY40NQJvwihxhD2QExAJ-WjylLLwBXm7YVtRGqTZB4RkF430TG3GKIc1G2sslfbKLA1SYbu_Pg7nUw-Wn7gatA1LGdSOM9KC.V0TchKVT5-NPB3qTNX4NZvoFgDkxzQ8X7eIdDirvIg7Tj7FPh9PmPGbZabH4RhL82avAJCvmvxtfrzsySSFqg
22. https://www.researchgate.net/publication/352178543_A_Study_on_Importance_of_Data_Mining_in_Information_Technology?_sg%5B0%5D=VsA5qNVTuutbkS4_wOJiTRA1BClqv4MBbBAFFVVGd_iksF4bNtbkfMIUhE3Av8YNYdHrCP7VThrFp6uWHvNVfm-dpUHcl2zqiibl9dOH.SVCpJY5va-Q3hATOrFNSSLVQ9OByfxAV-R3q7QabJaY-__jyjLZZmdjDwj-zNtzNK0jxjfXy_y6z6M__OeLW1A
23. https://www.researchgate.net/publication/352178543_A_Study_on_Importance_of_Data_Mining_in_Information_Technology?_sg%5B0%5D=Q4eSD6oSveOKdLp0MNv2jcRK1a77iodxS86y3j2FmDBHT7V36mkosB2pBJXvsa7qeK037tl6Lnv8vs7y1io-HmhxBo7Akppm9vpxcaC.eci_M0Bg3vU0C2ErAefr6xBGstzqeGZ6Db2sMR-kU8E2WfV_oOTqW65Vlz7FyTq0Xadsgg5CxAWtP2nMnOmz8w
24. https://www.researchgate.net/publication/363859895_An_Analytical_Study_of_Software_Testing_Models
25. https://www.researchgate.net/publication/352178391_A_STUDY_ON_CLIENT_SERVER_SYSTEM_IN_ORGANIZATIONAL_EXPECTATIONS
26. https://www.researchgate.net/publication/352178400_A_COMPARATIVE_ANALYSIS_OF_TRADITIONAL_MARKETING_VS_DIGITAL_MARKETING
27. https://www.researchgate.net/publication/352178478_Analytical_Study_of_Data_Warehouse
28. https://www.researchgate.net/publication/352178553_A_Study_on_Structured_Analysis_and_Design_Tools
29. https://www.researchgate.net/publication/352178694_A_STUDY_ON_IMPACT_OF_HEALTH_AWARENESS_IN_EDUCATION

30. https://www.researchgate.net/publication/352178508_A_Study_on_quality_of_Hospital_facilities_patient_satisfaction_through_various_Health_Care_Departments
31. https://www.researchgate.net/publication/352178664_Analytical_Study_on_System_Implementation_and_Maintenance
32. https://www.researchgate.net/publication/352178674_A_Comparative_Analysis_on_different_aspects_of_Database_Management_System
33. https://www.researchgate.net/publication/352178728_Quality_of_Patients_Care_in_Hospital_Setting_A_Critical_Analysis
34. https://www.researchgate.net/publication/353210680_CYBER_CRIME_TRENDS_IN_COVID-19_ERA
35. https://www.researchgate.net/publication/353210752_STUDY_OF_MALWARE_DETECTION_USING_MACHINE_LEARNING
36. https://www.researchgate.net/publication/353767742_Cyber_Growth_due_to_covid-19
37. https://www.researchgate.net/publication/363859378_Need_of_Popularization_of_Cyber_Security
38. https://www.researchgate.net/publication/363859713_REVIEW_OF_TEACHING_METHODOLOGIES_WITH_CYBER_WORLD
39. https://www.researchgate.net/publication/363859935_CYBER_CRIME_A_HIDDEN_EVIL