Research Article

Design of 16-Bit SAR ADC Using DTMOS Technique

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Article History: Received: 10 November 2020; Revised: 12 January 2021; Accepted: 27 January 2021; Published online: 05 April 2021

Abstract: This paper presents a 16-bit 100MS/s SAR ADC with 1V power supply for biomedical implant systems developed with low power technique i.e., DTMOS logic. It consists of a R-2R DAC, low-power comparator, a digital SAR logic with low-leakage. The designed comparator is a differential architecture that has used to have an excellent, common-mode noise rejection. Comparator was created for proper operation to remain in saturation and could be used with differential amplifier. The comparator is the chief block of power consumption, so we focused mainly much of ability we make to design this module. The ADC is designed using Cadence virtuoso with CMOS 45nm technology. For SFDR, SNR, ENOB and power consumption, the converter utilizes 63.97dB, 51.06 dB, 15.15 and 528.8uw.

Keywords: Comparator, Control logic, DAC, Low Power, SAR ADC

1. Introduction

The role of ADC is vital in the bi-signal processing; for noiseless signal processing, data conversion is essential. In the proposed physiological transmission system, the captured signals from the human body after amplification and feature extraction are then converted into digital form by ADC and processed to the receiver [58]. Data converters are essential in the signal acquisition board; they are the bridge between analog and digital form. For physiological signals, data converters speed is not much concern. These devices are implanted on the human body since they should be operated with ultra-low power and powered by harvested energy [59-60]. So by combining these two features with the required accuracy and resolution completes the design of ADC. In this thesis, it is highly concentrated on low power consumption with minimized supply voltages with low power optimized techniques. If the main criteria are higher resolution, then the ADC Sigma Delta (or ADC form implementation) is introduced. It's the most sluggish ADC and it's complex settingtoo. Several improved and hybrid systems includingsuch as Flash pipeline, SAR pipeline, SARflash is developed and discussed [1].to enhance processing speed and power consumption optimization. These ADCs have reduced the group of components, and that is not better to adjust power consumption beyond a certain limit.SAR ADC has becoming a bigger subject to study for its excellent power efficiency. It will be used for applications of medium resolution, high speed and low power and small section. This is in the making of an appropriate option such as biomedical purposes.Software too. It consumes less power to its simple structure and therefore innovation scalable as all with its elements or parts are digital other than a comparator. There were some other tasks connected to improve SAR ADC results and this document focus mostly for the extraction of loads. The differential amplifier was used even with fewer disturbances and higher standard noise reduction mode and common source amplifier phase have been used as a second amplification phase and level to keep the transistor in the area of saturation Section II defines the mainSAR ADC architecture. Section III describes various structures of the architecture as well as its diagrams and operation of the control logic. The observations and analysis of the simulation are given in the Section IV and Section V accordingly.

2. SAR ADC Structure

SAR ADC structured of a sample and hold circuit(S / H) that samplesthe analog input signal; comparator cont rasts the performance of DACto the on being sampled (reference) signal; a DAC that gets the value analog of control logic result (SAR); and checkingSAR logic which decides every bit [2]. The SAR ADC design can be seen in the figure 1.

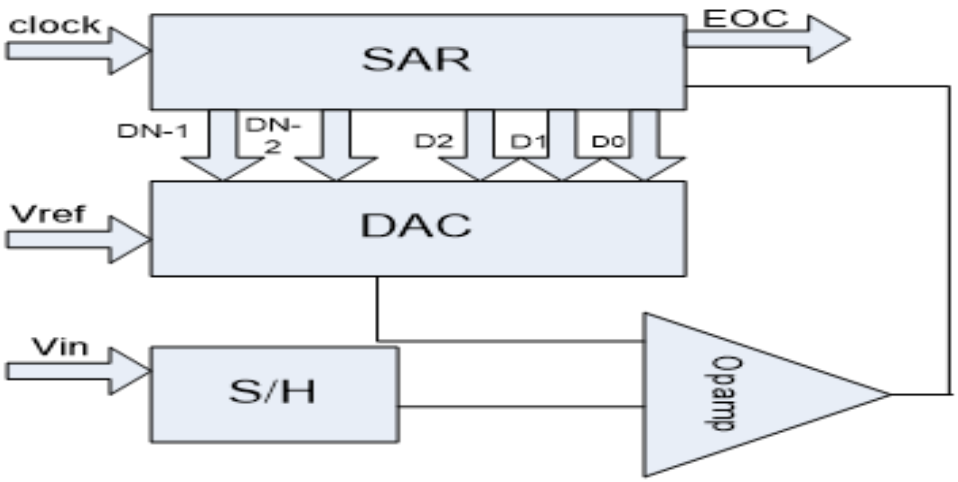

Figure1. SAR ADC Architecture

3. Design of SAR ADC

A. Track and Hold Circuit

An equivalent Sample and hold circuit is a device in which specified span is used to obtain voltage constantly variable analog signals and locks at a stable value. These are fundamental analog memory instruments that are applied in ADC to get out of some input signal gap which will occur harm mechanism of change**.** Using a condenser, this sample and hold circuit keeps electrical charge to it and then maintains. At only one switching system such as transistor in the field effect and one active amplifier sample and hold samples the input data and gives to comparator.

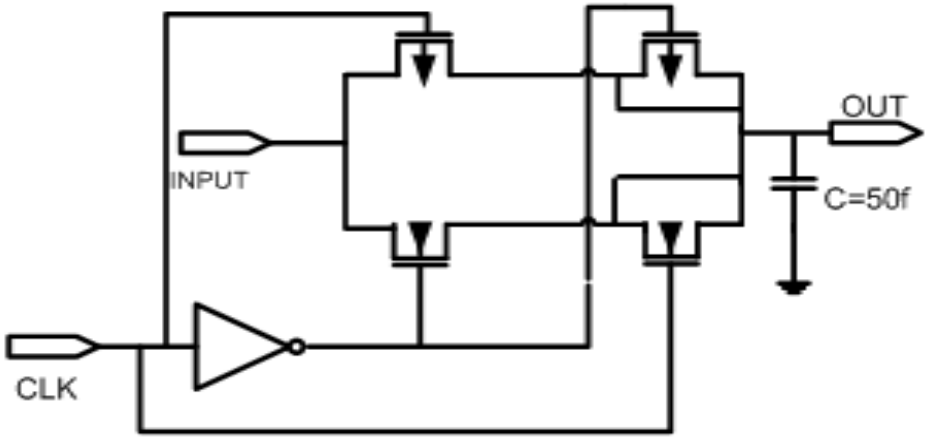

Figure 2. Track and hold circuit

The op amp will switch off and high impedance will be maintained for its output. Unit gain buffer linked take the sample and keep the output phase will be always functional during both sample and hold mode and gives the voltage on hold condenser using the sampling and retaining circuit. Using anoperational amplifier, it displays the track and hold circuit. It being connected by the transition to two op-amps. The sampling method will be on when the switch is in lock state. If the switch is unlocked, the holding will be activated. Connecting the condenser to the second op-amp implies keeping the condenser. We obtain samples of analog signals with the help of the condenser by using the sample and hold circuit. For a certainperiod of time, it maintains samples. When a stable signal is generated, the analog to digital converter can be used to alter it into a digital signal.

B. Comparator

A comparator is an electronic device that contrasts with two input values are added to it, generating. The comparator's performance value specifies which input is higher otherwise lower. Realize this comparator falls within the range of applications of non-linear IC that comparator is the primary power consumptionblock in the

structure that's the thing much of the progress has been put over this section. The comparator produces a high or low logic output factor depends between analog input and band gap voltage. For this function the comparator becomes an improved operational speed andstrong resolution.

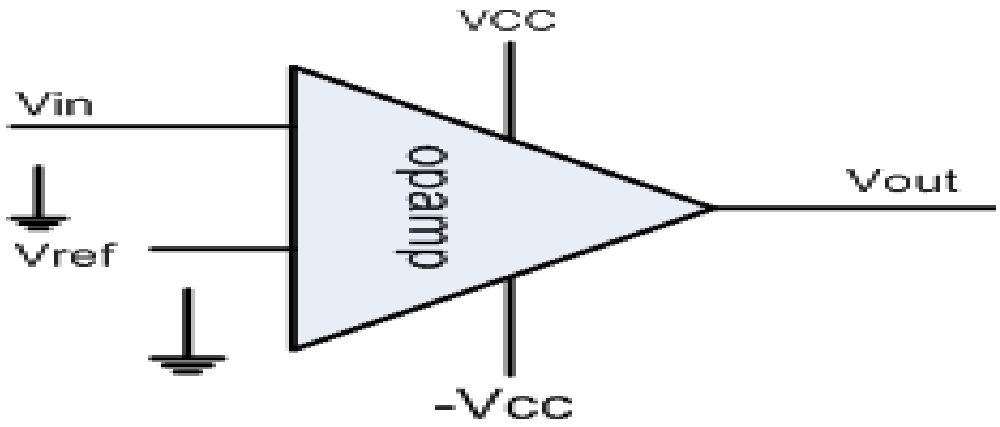

Figure 3. Op amp as comparator

C. Digital to Analog Converter

The R-2R DAC is a modification to the DAC model of the binary weighted resistor ladder where only two resistor values are used. The resistor ladder in R-2R DAC is designed to connect resistors in series with resistor value R, then 2R resistor rungs can be represented as in current mode or voltage mode depending on the reference voltage. Switches operated in voltage mode between Vref and ground and the switches operate in current mode between output and ground where the reference voltage is attached to the ladder resistor. The advantage of R-2R DAC is that it needs only resistors with only two values of resistance and 2N is the number of resistors. The output impedance for this model is always constant due to the 2R resistance of the ladder rung on each side. Current source transistors are used to increase the linearity of this system in combination with the resistor ladder network. To change the reference voltage between ground and digital level, a physical amplifier must be used. This limits the bandwidth and linearity errors can occur with the use of the op amp output buffer.

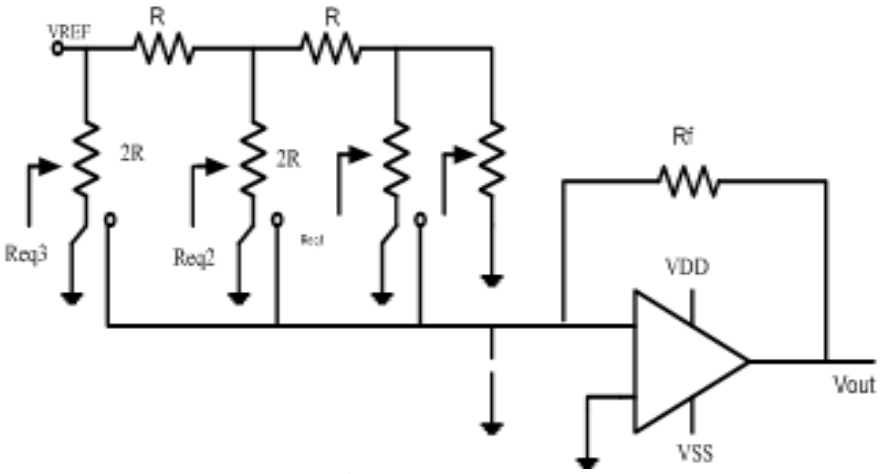

Figure 4. R-2R DAC

Switches operate between ground and Vref in voltage mode, which is difficult to design. Since the switches are directly connected to the output node, there will be glitches in the current mode.

D. Successive Approximation Register Logic

Successive Approximation Register (SAR) control logic determines each bit successively. Basically the Successive Approximation (SA) register contains N flip flops for an N-bit ADC and some combinational logic. It implements its operation with the binary search algorithm. SAR ADC performs all possible bits of binary

search.Each bit has three options: it can be set to '1,' it can be set to '0 or maintains its value. The operation is briefly explained as:

The SAR is reset at the start of the conversion cycle by holding a high start signal. MSB bit is set to ' 1 ' on th e positive edge of the first clock pulse and reset other bits (' 0 ').This digital word is then created by the DAC ana log equivalent. The comparator compares the DAC output to the analog input signal being sampled. The compar ator gives LOW output if the DAC output is lower than the sampled input. and the SAR MSB will be reset (‘0’). If the DAC output is lower than the sampled input, the comparator gives HIGH output and the SAR MSB will be held and on the positive edge of the next clock pulse the next MSB will be set (’).For the other bits, the same pro cess is repeated until each SAR bit is determined. Once LSB is tried, the SAR forces the full HIGH conversion si gnal to enable the latch to digitally deliver the valid data. In this case, for "N" bit ADC, "N+1" clock cycles are r equired.

The SAR conversion uses a binary search algorithm as its name implies. The inner circuit is therefore much easier to run than the full ADC sampling frequency. In general, the inner circuit runs at least as quickly like resolution for the Analog-to-Digital Convertersample rate. Thus a 10 bit, 1 MS/S SAR ADC [4].internally does not operate any slower than 10 MHz, allowing for the resolution of all 10 bits in one sample time. An SAR ADC's fundamental structure is very basic and can be seen in Figure even though it developed over the years with further variations and development.

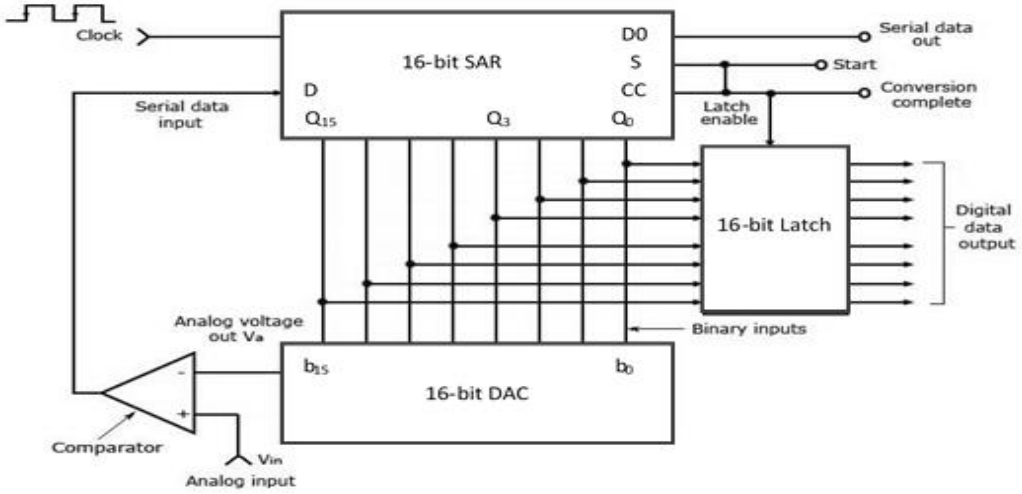

Figure 5. Schematic View of SAR ADC

4. DTMOS Logic

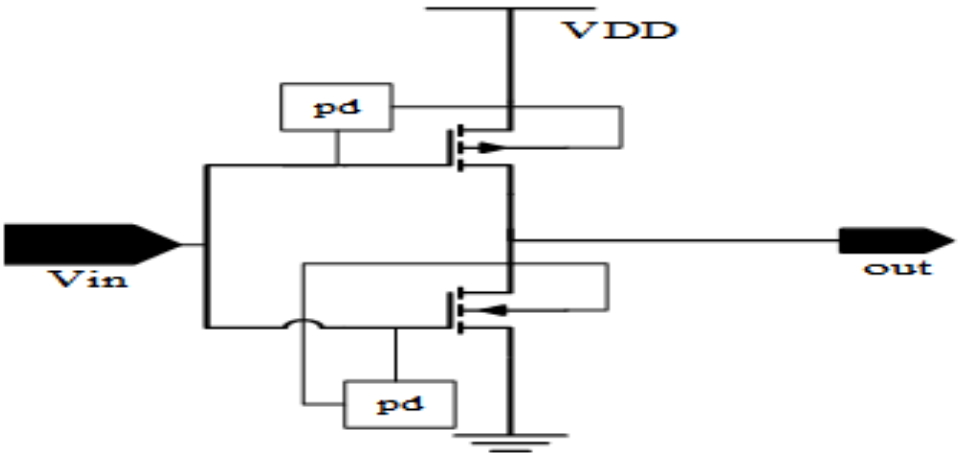

Figure 6. DTMOS inverter

For adaptivethreshold CMOS, their pinch off voltage was changed progressively match its operational status upon the device here the NMOS and PMOS transistor body is biased dynamically. Sufficient body biasing voltage to both PMOS and NMOS transistors are provided by the potential dividers which are connected to the input for that inverter. The maximum input impedance in ideal mode provides lower conduction losses whereas a small voltage level makes to large output switches in aggressive state. It could attain adaptive CMOS threshold while binding the gate with body attached. DTMOS input power is constrained mostly by constructed-in diode ability in mass silicon machineries. A p-n diode must be negative voltage among source and body.

5. Results and Exploration

Figure 7 shows the calculated *SNR of* 51.02 dB for 16bit. The blue color line denoted with 'F' is indicates fundamental power, orange lines indicate the noise. The figure 8 shows square boxes with numbers are indicates the harmonics presented.

Figure 9 shows the calculated the Spurious Free Dynamic Range (*SFDR)* of 63.97 dB for 12bit. The portion shade with blue color is SFDR and 'F' is indicates fundamental power, S is the spurs.

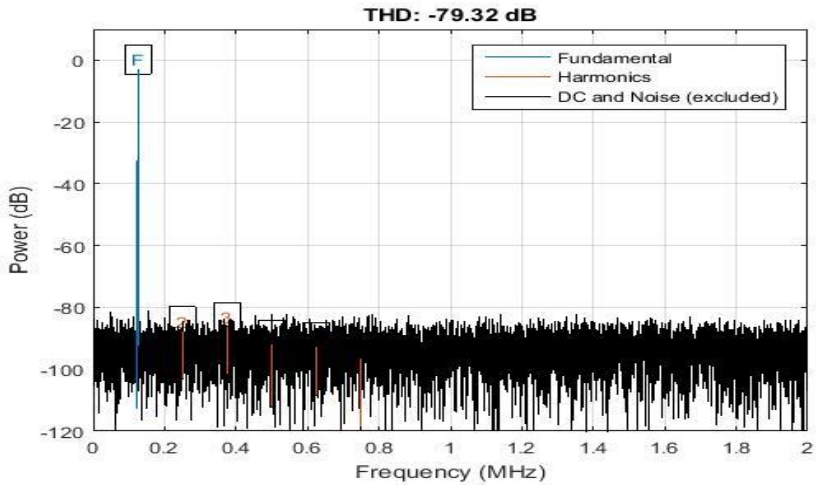

Figure 7. Total harmonic distortion

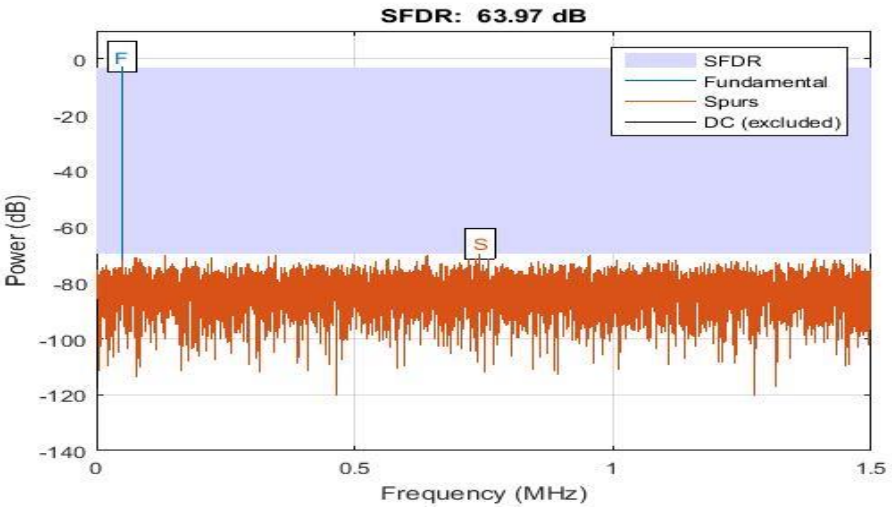

Figure 8. SFDR

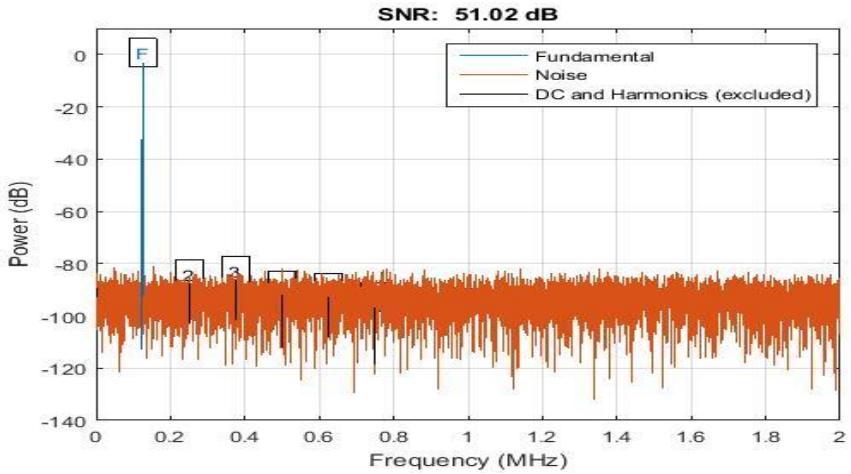

Figure 9. SNR

Hence results obtained during this aspect can be found in this chapter, where their implications are addressed as well as the use of CMOS 45 nm technology for circuit implementation.

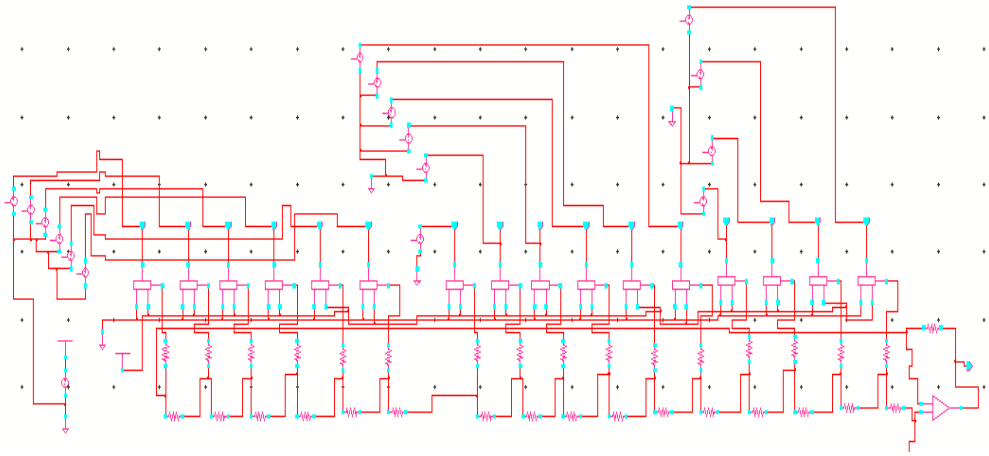

Figure 10. Schematic of R-2R DAC

Table 1. Comparison with existing one

	This work	**[7]**	**[8]**	**[6]**	**[9]**
Architecture	SAR	SAR	SAR	SAR	SAR
VDD[V]	1	1	1	1	1.2
Power	528.8 µW	127.8µW	820µW	0.98mW	0.826mW
Technology(nm)	45	180	65	90	130
Resolution (bits)	16	10	10	10	10
F_{sample}	100Msps	-	-	30Msps	50Msps
DNL(LSB)	+0.66/-0.52	-	-	-	+0.91/-0.63
INL(LSB)	+0.4/-0.33	-	-	-	+1.27/-1.36
SFDR (dB)	63.97	-	75.2	-	65.9
SNR (dB)	51.02	-	56.9	57	57
ENOB	15.15	-	9.16	9.16	9.18

6. Conclusion

This paper16-bitsuccessive ADC approximation is functionally concludedwith 1V supply voltage and which is simulated in cadence 45nm CMOS technology this paper mainly focusses on. Minimum power comparator and Digital-to-analog converter(DAC) as more power is used by SAR ADC.The SAR ADC is more appropriate to biomedical applications.

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