TACKLING THE VOLTAGE ISSUES AND HARMONIC DISTORTIONS WITH DISTRIBUTION STATIC COMPENSATOR (DSTATCOM) USING SRF CONTROLLER AND DEADBEAT CONTROLLER

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ABSTRACT This paper presents a comparison of two control algorithms used in controlling the DSTATCOM for reducing the harmonic distortions and tackling power quality issues. The paper focuses on Synchronous Reference Frame (SRF) controller and a deadbeat controller for DSTATCOM. The two controllers are simulated and tested for 1) nominal operations 2) voltage sag conditions and 3) THD analysis. The results are measured and compared between the conventional Synchronous Reference Frame based controller and deadbeat controller using MATLAB/SIMULINK. The THD analyses shows that there is a reduction of THD values from 37.13% (distribution system without DSTATCOM) to 2.06% (DSTATCOM with SRF controller) and 0.65% (DSTATCOM with deadbeat controller). The simulation results shows that the deadbeat controller is better than the SRF controller in tackling the power quality issues and in reducing the total harmonic distortion, thus improving the power quality.
Keywords: Flexible AC transmission system (FACTS), DSTATCOM, controllers, voltage sag, power quality improvement, Total Harmonic Distortion (THD)

1. Introduction

Quality of power is an important problem analysed by electricity consumers nowadays (Arrillaga, N.R. and Bollen 2000). Different agencies are performing extensive surveys to quantify the power quality issues (PADIYAR 2007). Many efficient solutions have been developed from time to time to eliminate the power quality issues like active filters, passive filters, hybrid filters and custom power devices. Custom power devices (CPD) are power semiconductor switches used in the transmission as well as distribution lines to eliminate power quality disturbances (Crow 2004).

There are Voltage Source Inverter (VSI) type bridge structure and Current Source Inverter (CSI) bridge structure for power quality improvement, in which the CSI type is less used. On the basis of alignment in the system, the CPD's can be classified as shunt connected (DSTATCOM), series connected (DVR) and hybrid connected (UPQC) (Comprehensive Review of Distributed FACTS 2020). using Among these, DSTATCOM is most widely used to eliminate both current and voltage related issues, harmonic elimination, flickering problems and load balancing (Phipps, Nelson and Sen 1994). Among these FACTS devices, the compensation DSTATCOM is much cost-

effective (Sundararaman Kumar and Menakadevi 2020). The control algorithms developed by the researchers have contributed much to reduce the power quality issues. Some of them are Synchronous Reference Frame (SRF), Instantaneous Symmetrical component theory, neural network-based algorithms, fuzzy logic-based algorithms and so on (Singh and Solanki 2003). The performance of the system is analysed and verified through simulation. (Ledwich and A 2002)

This paper deals with the comparison of SRF based control algorithm and deadbeat control algorithm for DSTATCOM. This paper is organized as follows. Section 2 explains the working of DSTATCOM. Section 3 deals with control algorithms of DSTATCOM, Synchronized Reference Frame Theory (SRFT) based control algorithm and deadbeat controller-based algorithm. Section 4 presents the simulation results using MATLAB/SIMULINK for the system without DSTATCOM, system with DSTATCOM using SRF controller and system with DSTATCOM using deadbeat controller for nominal operation and voltage sag. THD analysis of the two controllers are compared using MATLAB/SIMULINK.

2. Distribution Static Compensator (Dstatcom)

The Distribution Static Compensator (DSTATCOM) is a voltage source used for improving the power quality. The DSTATCOM continuously checks the line waveform with respect to a reference ac signal, and therefore the voltage variations are reduced by injecting leading or lagging reactive current (Singh *et al* , 2008). The major components of a DSTATCOM given in Fig 1.

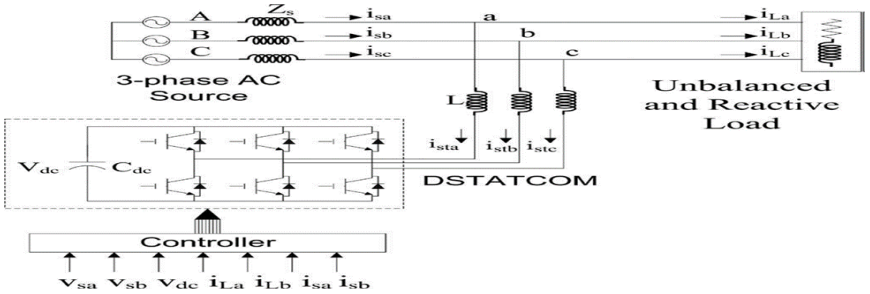


Figure 1. Distribution Static Compensator (DSTATCOM)

It consists of a Voltage Source Inverter (VSI) along with dc capacitor. The VSI provides the switching pulses for the working of the DSTATCOM which is controlled by the controller. The output of the VSI is filtered with an AC filter and compared with AC signal from the main distribution system (Yao.Z and Xiao.L, 2013).

2.1 Basic Operating Principle

DSTATCOM has the ability to generate and exchange reactive power when needed and it can also generate real power using the dc capacitor. (Mishra *et al* 2003)

1) Reactive power exchange: It provides lagging current to the system when the output voltage of VSI is less than the main line ac voltage at the PCC.

2) Real power exchange: it provides leading current to the system when the output voltage of VSI is greater than the main line ac voltage at PCC.

DSTATCOM is employed at the distribution level or at the load end for power factor

improvement and voltage regulation. The performance of a control algorithm is analysed by its flexibility and how fast it can be implemented. It also depends on how well the system responds to a sudden variation. The steps involved in the implementation of a control algorithm are as follows:

- Voltages and currents are measured
- Compared with the reference values
- Calculation of compensating signals
- Generation of firing angles of switching devices

The transient and steady state performance of the overall system depends upon the generation of appropriate PWM switching pulses.

3. Control Algorithms

The reactive power needed by the load during sudden load change is given by the DSTATCOM during reactive power compensation. The switching pulses of the DSTATCOM depends upon the reference source current and fundamental value of load current which is extracted by using different control algorithms (Gheewala et al. 2017). In this paper, two control algorithms are discussed and compared on account of harmonic distortion, mitigation of voltage sag, UPF operation and Total Harmonic Distortion (THD).

3.1 SRFT Control Algorithm

In SRF theory, the computations are carried out in a rotating d-q frame. (Geddada *et al* 2015). Fig. 2 shows the block diagram representation of this theory. The current and voltage inputs v_a, v_b, and v_c and i_{La}, i_{Lb}, and i_{Lc} are sensed and fed to the controller. On passing the signals through Phase-Locked Loop (PLL), unit vector templates are generated. The signals are then passed through a Low Pass Filter which then undergoes reverse Clark's and Park's transformation to extract back the abc signals (i_{sa}, i_{sb}, and i_{sc}). They are then fed to a hysteresis-based PWM signal pulse generator to generate final switching signals fed to the DSTATCOM; this acts a controller block for DSTATCOM. The main disadvantage regarding this method is that the operation of PLL makes the entire process slow.

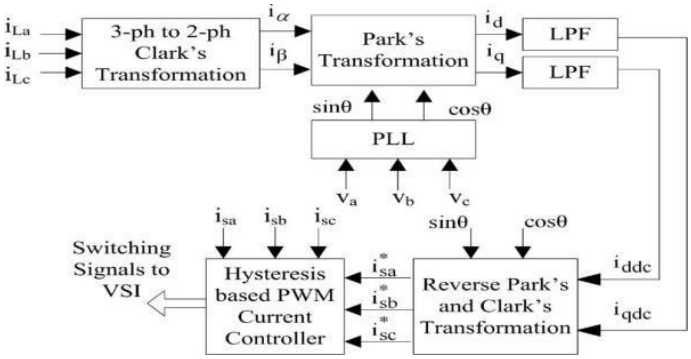


Figure 2. Block diagram of SRF theory

3.2 Deadbeat Control Algorithm

This is a predictive control algorithm which predicts the (n+1) th control signal and compares with the nth signal depending upon the present system conditions. Instantaneous symmetrical component theory is used to extract the switching signals for the DSTATCOM. Another important feature of the

controller is the Unit Vector Generation module which extracts the unit vector templates of the sensed inputs which makes the calculation simpler. The control algorithm also provides a fast voltage regulation as it used the state- space analysis for computing reference signals (Kumar and Mishra 2014). The deadbeat controller with IRP theory could be operated either in Current Controlled Mode (CCM) or Voltage-Controlled Mode (VCM) (Ramtharan *et al* 2006). At nominal operation the controller maintains UPF operation by working in CCM and during voltage disturbances the controller works in VCM. The overall control block diagram is given in fig.3.

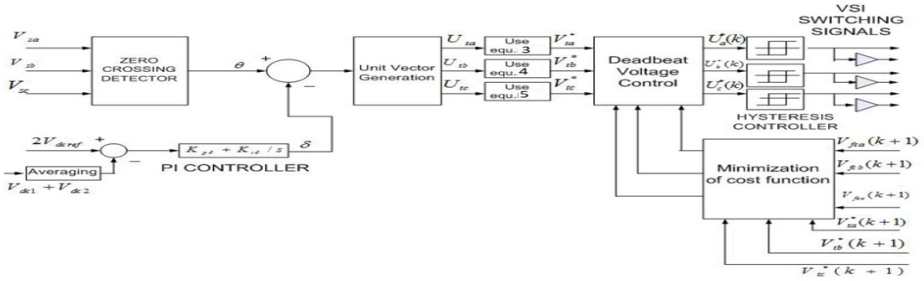


Figure 3. Overall block diagram of deadbeat control algorithm

DC capacitor voltage is controlled and maintained by PI controller (Maheswari, et al. 2015). The VSI parameters are designed and tabulated in Table 1. The change in dc capacitor voltage during load changes might affect the compensation process. Capacitor voltage should be maintained near the reference value for good compensation. PI controller supports the dc-link to maintain its voltage value by varying the gains. The average value of real power at PCC is given by:

$$P_{pcc} = P_{lavg} + P_{loss} \tag{1}$$

where P_{pcc}, P_{lavg}, and P_{loss} are the average PCC power, load power and losses in the VSI, respectively. The load angle δ is computed by the PI controller adjusting the gains. The average value of the dc-link voltages is compared with the reference voltage and the error computed is forwarded to the PI controller.

Table 1. Design parameters of VSI

V_{L-L} = 400V	V_{dc}= 650V
C_{dc}= 2600μF	$C_{dc} = \frac{2pST}{V_{dcref}^2 - V_{dc}^2}$
C_{fr} = 5μF	$C_{fr} = \frac{1}{\omega_0^2 L_s}$
L_f = 22mHz	$L_f = \frac{0.5V_m}{\omega_0^2 L_s}$

The PCC voltage depends on the load angle. Hence to make the PCC voltage stable δ should be maintained constant.
By changing the value of load angle, we can regulate the dc-link voltage. The load angle δ is computed as:

$$\delta = K_{p\delta}\, e_{vdc} + K_{i\delta} \int e_{vdc} dt \tag{2}$$

where $e_{vdc} = 2V_{dcref} - (V_{dc1} + V_{dc2})$ is the voltage error . $K_{p\delta}$ and $K_{i\delta}$ are proportional gain and integral gain, respectively. The controller gains must be chosen properly as the flow of power depends upon them. The main component of unit vector generation is the phase locked loop (PLL). The terminal voltages are multiplied by a gain equal to $1/V_m$ (V_m is the peak amplitude of fundamental terminal voltage) to extract the unit vector templates. The output of the PLL is expressed mathematically as

$$U_a = sin\omega t$$

$$U_b = \sin(\omega t - 120)$$

$$U_c = \sin(\omega t + 120)$$

The reference terminal voltages of the three phases are calculated as:

$$V_{ta}^*(t) = \sqrt{2}V_t^* \sin(\omega t - \delta) \quad (3)$$

$$V_{tb}^*(t) = \sqrt{2}V_t^* \sin\left(\omega t - \frac{2\Pi}{3} - \delta\right) \quad (4)$$

$$V_{tc}^*(t) = \sqrt{2}V_t^* \sin\left(\omega t + \frac{2\Pi}{3} - \delta\right) \quad (5)$$

where $V_t^* = \sqrt{V^2 - (|I_{la1}^+|X_s)^2} - |I_{la1}^+|R_s$ is the reference load voltage.

From this control algorithm, future reference voltage can be predicted by the equation

$$V_t^*(k+1) = 3V_t^*(k) - 3V_t^*(k-1) + V_t^*(k-2) \quad (6)$$

From this equation, one-step ahead voltage control lawcan be found from the equation,

$$U^*(k) = \frac{V_t^*(k+1) - G_{11}V_{fc}(k) - G_{12}i_{fi}(k) - H_{12}i_{ft}(k)}{H_{11}} \quad (7)$$

where the terms of this equation are developed on the basis of the circuit diagram shown in fig.4.

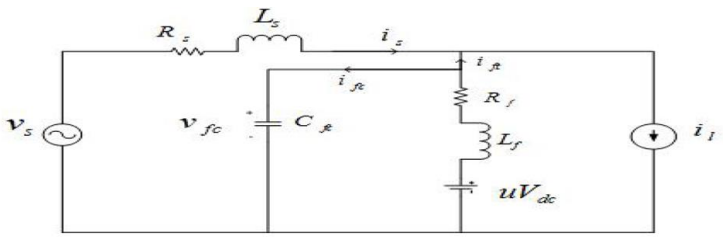


Fig 4 Single Equivalent circuit

L and R are filter inductance and resistance respectively. State space equations of the system is

$$\dot{x}=Ax+Bz \tag{8}$$

where

$$A=\begin{bmatrix} 0 & \frac{1}{C_{fc}} & 0 \\ \frac{-1}{L_f} & \frac{-R_f}{L_f} & 0 \\ \frac{-1}{L_S} & 0 & \frac{-R_s}{L_s} \end{bmatrix} \quad B=\begin{bmatrix} 0 & \frac{-1}{C_{fc}} & 0 \\ \frac{V_{dc}}{L_f} & 0 & 0 \\ 0 & 0 & \frac{1}{L_s} \end{bmatrix} \quad x=[v_{fc} \quad i_{fl} \quad i_s]^t \quad z=[u \quad i_{ft} \quad v_s]^t$$

The state vector x(t) is computed as follows:

$$x(t)=e^{A(t-t_0)}x(t_0)+\int_{t_0}^{t} e^{A(t-\tau)}Bz(\tau)\,d\tau \tag{9}$$

Replacing t0 = kT_d and t=(k+1) t_d, the equivalent discrete solution of equation (9) can be simplified as follows,

$$x(k+1)=e^{AT_d}x(k)+\int_{0}^{T_d} e^{A\lambda}Bd\lambda z(k) \tag{10}$$

Equation (10) is rewritten as follows:

$$x(k+1)=Gx(k)+Hz(k) \tag{11}$$

where G and H are sampled matrices, with a sampling time of T_d. For small sampling time, matrices G and H are calculated as follows:

$$G=\begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix}=e^{AT_d}\approx I+AT_d+\frac{A^2{T_d}^2}{2} \tag{12}$$

$$H=\begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix}=\int_{0}^{T_d} e^{A\lambda}Bd\lambda \tag{13}$$

From (12) and (13), $G_{11} = 1 - \frac{T_d^2}{2L_f C_f}$, $G_{12} = \frac{T_d}{C_{fc} - \frac{T_d^2 R_f}{2L_f C_f}}$, $H_{11} = \frac{T_d^2 v_{dc}}{2L_f C_{fc}}$, $H_{12} = \frac{-T_d}{C_{fc}}$. By substituting these values in (7), we obtain the voltage control law. Hence the capacitor voltage using (8) is given by

$$V_{fc}(k+1) = G_{11} v_{fc}(k) + G_{12} i_{fi}(k) + H_{11}(k) + H_{12} i_{ft}(k)$$

(14)

Equation (14) shows that terminal voltage depends upon the sampling time and VSI parameters. (B.Widrow 1975)

4. Results And Discussions

The control scheme is implemented using MATLAB/SIMULINK. Two conditions namely nominal operation and operation during sag are compared between a SRF based method and the deadbeat voltage controller algorithm. The two controllers are compared by measuring Total Harmonic Distortion (THD), settling time and voltage sag (Patjoshi and Mahapatra, 2013).

The Simulink model of DSTATCOM with SRF controller is given in fig 5. The model is designed with a 25kV rms voltage source and an 1kW inductive load. The DSTATCOM with SRF controller is connected to the Point of Common Coupling (PCC) through a coupling transformer. The DSTATCOM block consists of the bridge circuit and the controller.

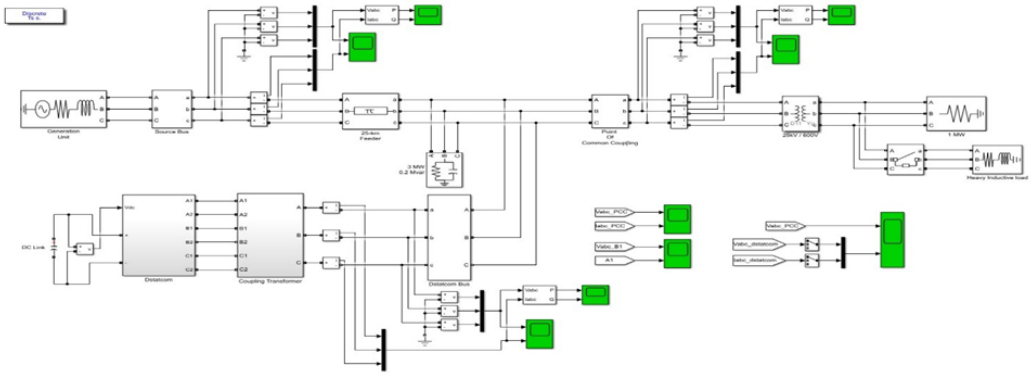


Fig 5 Simulation model of DSTATCOM with SRF controller

The Simulink model of SRF controller is given in fig.6. This converts the “abc” frame to “dq” frame for the measurement of voltage and current.

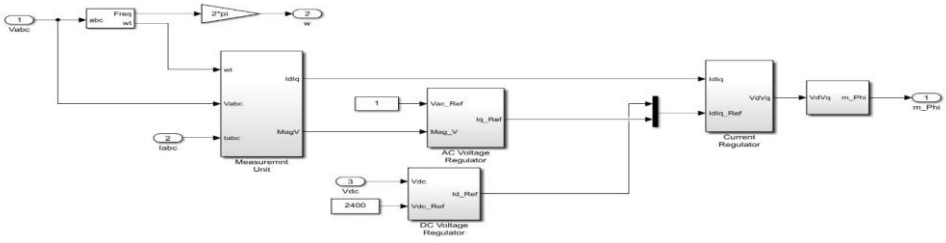


Fig.6. Simulation model of SRF controller

The simulation model of DSTATCOM with deadbeat controller is given in fig.7.

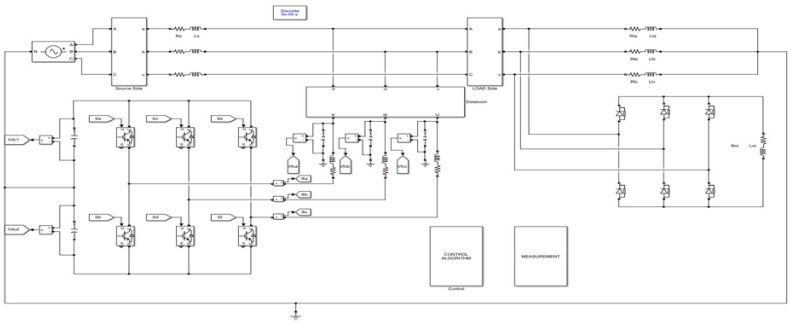


Fig 7. Simulation model of DSTATCOM with Deadbeat controller

The simulation model consists of 25kV rms voltage source and a non-linear load, 1 kW inductive load. The simulation model of the deadbeat controller is given in fig.8.

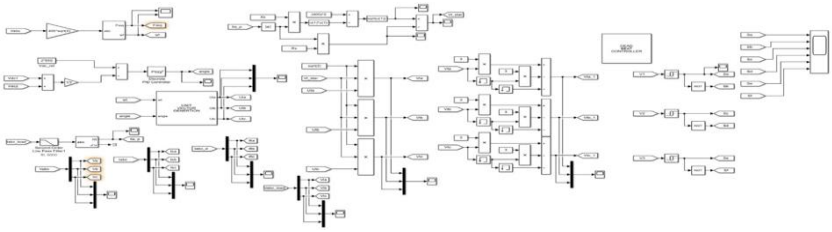


Fig.8. Simulation model of deadbeat controller and PI controller

4.1 Nominal Operation

During nominal operation, harmonics is injected in the system by the non-linear load, an inductive load. Both SRF controller and Deadbeat controller reacts differently to such harmonics.

4.1.1 SRF Controller

From the simulation model given in fig 5, the waveforms of source voltage and source current are given in fig 9.

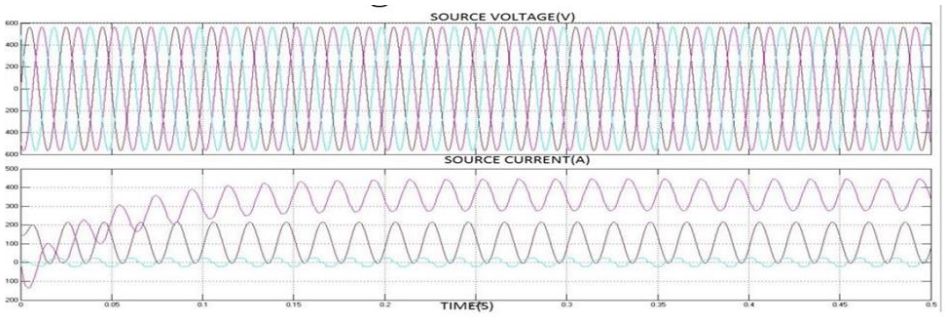


Fig 9. Source voltage and source current with SRF controller

From the figure it is clear that the harmonics present in the source current are compensated but they are not balanced. From fig.7, the waveform of source current and source voltage after compensation by a deadbeat controller is given in fig.10.

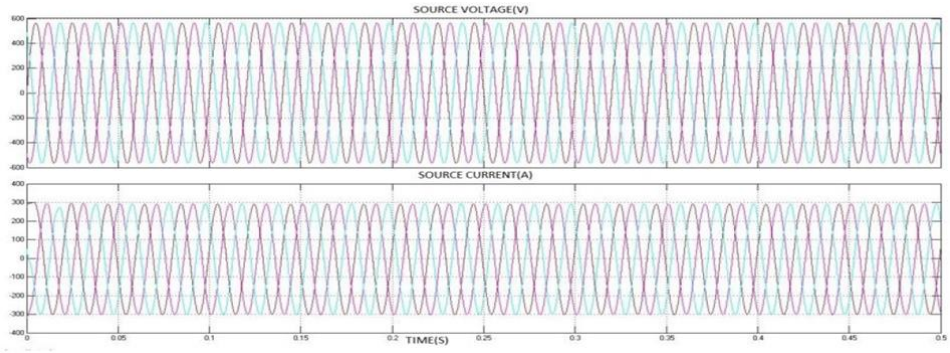


Fig 10. Source current and source voltage with deadbeat controller

From this waveform it is clear the current waveform is free from harmonics and is balanced. The deadbeat controller very well filters the harmonic elements from source current and makes the system stable. Similarly, the load current waveforms also show the same improvement. The load current waveform using a SRF control algorithm is shown in Figure 11.

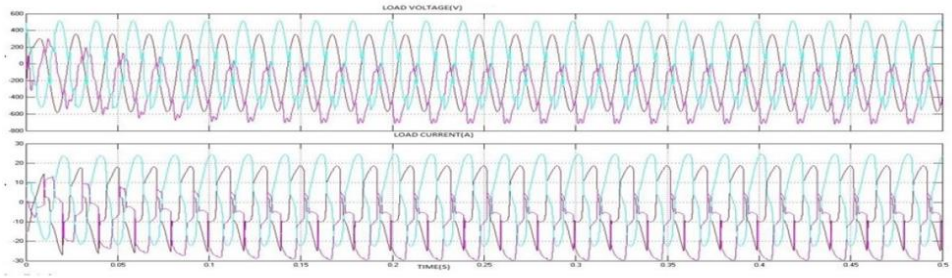


Fig 11. Load current and load voltage with SRF controller

In nominal operation SRF controller is not able to remove the harmonics completely from the load end. Fig.12 shows the waveform of load voltage and load current using a deadbeat controller.

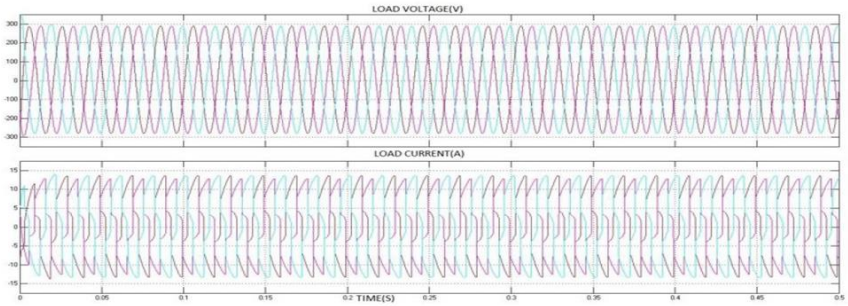


Fig. 12. Load voltage and load current using deadbeat controller

The deadbeat control removes the harmonics better than the SRF controller but not completely. Compared to fig.11, the harmonics is completely removed from the load voltage waveform.

Comparing the reactive powers of the two systems, in the system with SRF controller the reactive power takes time to settle down, i.e., after a disturbance, the system takes time to settle down. But in the system with deadbeat controller, the reactive power settles down in a fraction of time. This is shown in fig.13 and 14.

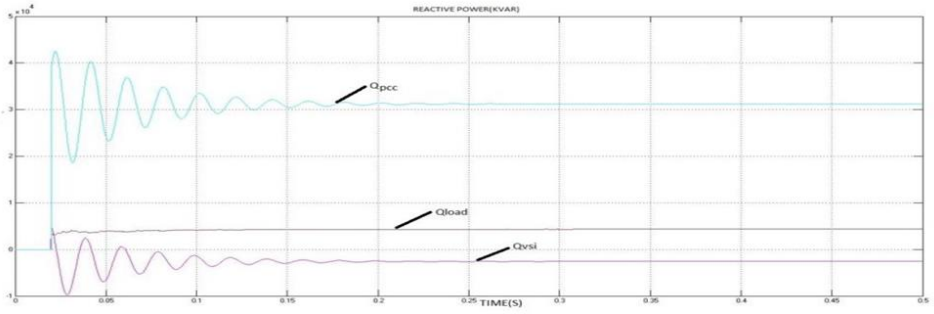


Fig.13 Reactive power using SRF controller

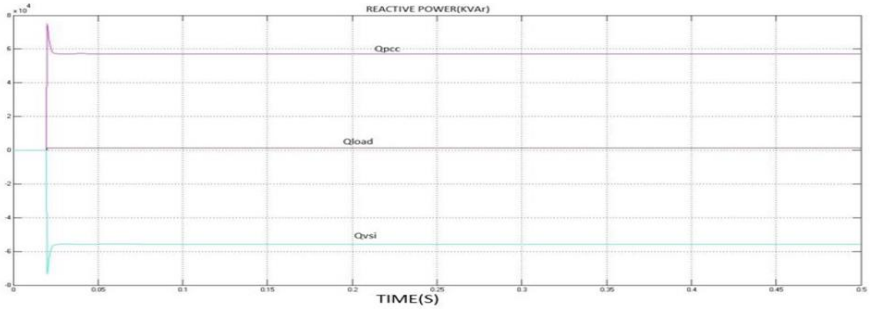


Fig 14. Reactive power using deadbeat controller

SRF controller do not provide a Unity Power Factor (UPF) operation but deadbeat controller provides a UPF operation, which is the unique quality of deadbeat control algorithm. The UPF operation of deadbeat controller is given in fig.15.

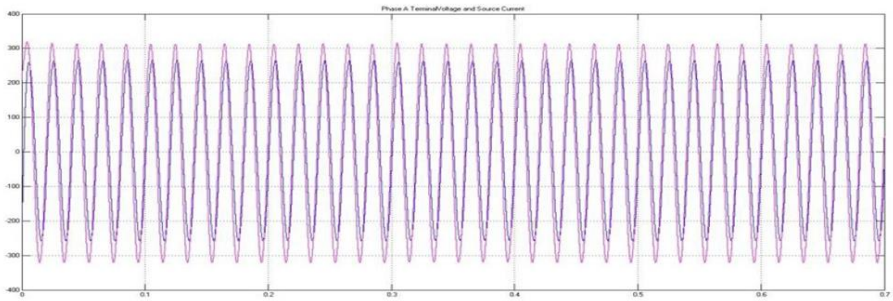


Fig.15 UPF operation

4.2 Operation During Sag

Voltage sag is introduced in the system by injecting a heavy inductive load at particular intervals using a breaker. The system without a DSTATCOM is given in fig 16.

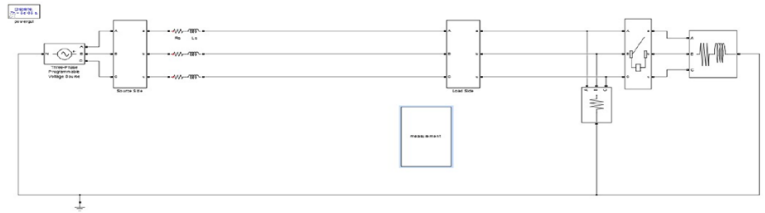


Fig.16 System without DSTATCOM

The load voltage waveform of the test system is given in fig.17. In the waveform, the voltage sag takes place between the time interval 0.3-0.4 s.

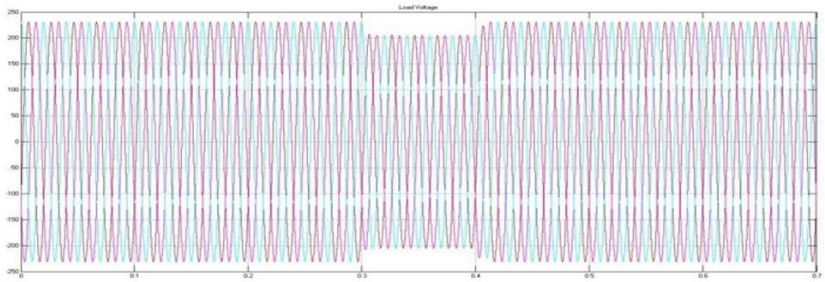


Fig 17. Load voltage of the system without DSTATCOM

The MATLAB/SIMULINK model given in fig.5 using SRF controller mitigates 90% of the voltage sag issue. The waveform of the load voltage after compensation is given in fig.18.

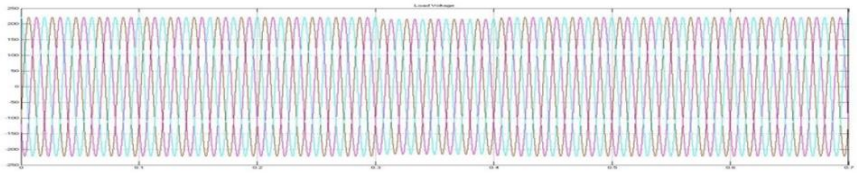


Fig.18. Load voltage of the system with DSTATCOM using SRF controller

For better mitigation of voltage sag DSTATCOM uses deadbeat controller which completely mitigates the voltage sag caused during the time interval 0.3-0.4s. The waveform is given in fig.19. Here the highly inductive load is switched between 0.3-0.4s. In the system without DSTATCOM the voltage is reduced between these time intervals to 200V, but in the system with DSTATCOM using SRF controller there is an improvement in this voltage to 222V and it has the nominal value to 250V in the system with DSTATCOM using deadbeat controller.

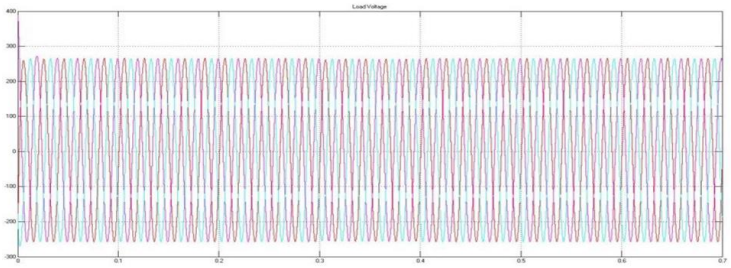
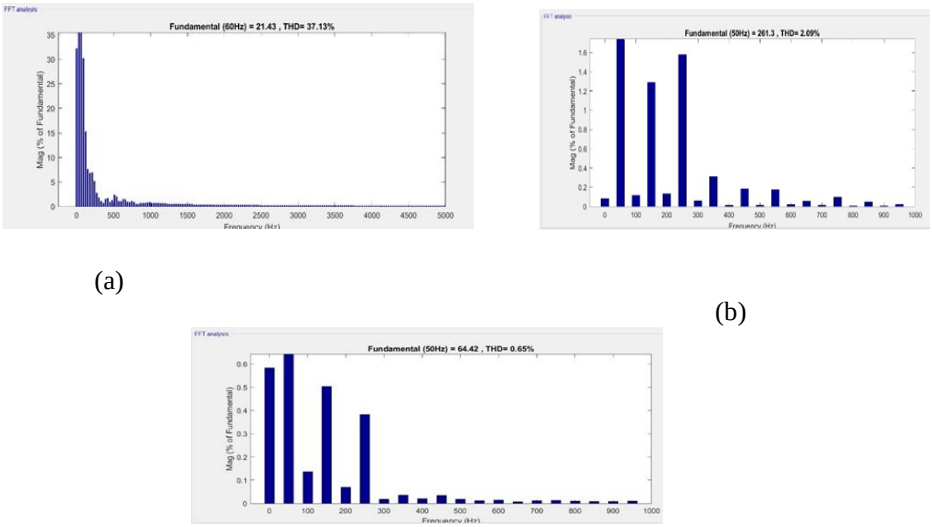


Fig. 19 Load voltage of the system with DSTATCOM using deadbeat controller

4.3 THD Analysis

The Total Harmonic Distortion (THD) is measured and compared for these two controllers. THD of a signal is the measurement of the total harmonics present in a signal and is defined as the ratio of the sum of the powers of all harmonic components to the fundamental frequency component. Here

the THD analysis is done using MATLAB/SIMULINK. Fig.20 (a),(b) and (c) shows the FFT analysis of the test system, SRF controller and deadbeat controller to compute the THD value.



(a)

(b)

(c)

Fig 20. FFT analysis of system without DSTATCOM, SRF controller and deadbeat controller

The lesser value of THD indicates that the system is more stable and has a faster response. Table 2 shows comparison of SRF controller and deadbeat controller. This shows that THD value has decreased from 2.09% in SRF controller to 0.65% in deadbeat controller. In the voltage sag case, the voltage has decreased to 200 V during the time interval 0.3s-0.4s. SRF controller has compensated this to 222V and deadbeat controller has compensated this to 250V. After a fault or injection of non-linear load the system settles down in a time of 0.2s in case of SRF controller and it only takes 0.025s in case of deadbeat controller. So, we can conclude that DSTATCOM with deadbeat controller shows a better performance than DSTATCOM with SRF controller.

Table 2 Comparison of SRF controller and Deadbeat controller

MEASURING FACTOR	SYSTEM WITHOUT DSTATCOM	SRF CONTROLLER	DEADBEAT CONTROLLER
THD (%)	37.13%	2.09%	0.65%
Voltage sag (V)	200V	222V	250V
Settling Time (s)	100s	0.2s	0.025s

Table 3 shows the comparison of different control algorithms of DSTATCOM on the basis of THD values. From the control algorithms compared deadbeat controller has the lowest THD value which makes it a good option for improving the power quality problems.

Table 3 Comparison of Proposed work with existing works

REFERNCES	DSTATCOM CONTROLLERS USED	THD (%)
Dinesh et al, (2012)	Hysteresis controller [19]	2.51%
Bhatia, R. S. and Nijhawan, P (2012)	PI controller [20]	3.39%
Sri Prakash et al. (2017)	P-Q theory-based controller [21]	3.63%
Proposed Work	**SRF controller**	**2.09%**
	Deadbeat controller	**0.65%**

Dinesh et al. has proposed hysteresis controller for DSTATCOM in their work which calculates the THD value as 2.51%. DSTATCOM using PI controller has been proposed by Bhatia, R. S and Nijhawan, P and this work calculates the THD value as 3.39%. Sri Prakash et al. uses PQ theory-based controller for DSTATCOM which measures the THD value 3.63%. From all these existing controllers, deadbeat controller reduces the THD value to an acceptable level.

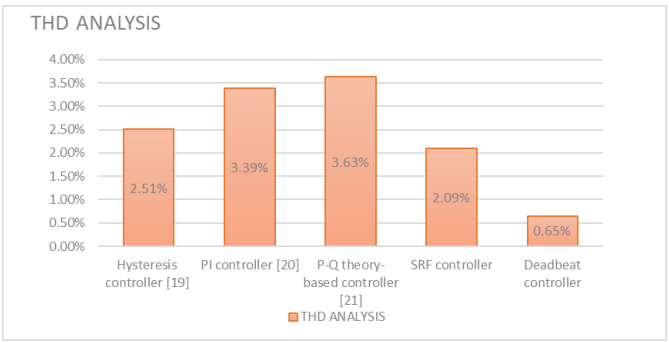


Fig 4.9 THD Analysis of Different Controllers of DSTATCOM

5. Conclusion

In this paper, two control algorithms of DSTATCOM have been compared considering three factors 1) Harmonic distortion 2) Voltage sag 3) THD analysis. The deadbeat controller gives better performance than the SRF controller. In the voltage sag condition, voltage sag is caused by injecting a non- linear load during a specific interval of time. In this case, deadbeat controller mitigates the voltage sag completely compared to the other controller. THD analysis shows that the amount of harmonic distortion is reduced considerably using deadbeat controller. The value has been reduced to 2.09% using SRF controller and reduced to 0.65% using deadbeat controller compared to the system without DSTATCOM. From the simulation results its concluded that deadbeat controller shows a better performance compared to SRF controller for compensating power quality disturbances.

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