Performance Analysis of a Low Power High Speed Hybrid Full Adder Circuit and Full Subtractor Circuit

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Abstract: In this paper, a hybrid 1-bit adder and 1-bit Subtractor designs are implemented. The hybrid adder circuit is constructed using CMOS (complementary metal oxide semiconductor) logic along with pass transistor logic. The design can be extended 16 and 32 bits lately. The proposed full adder circuit is compared with the existing conventional adders in terms of power, delay and area in order to obtain a better circuit that serves the present day needs of people. The existing 1-bit hybrid adder uses EXNOR logic combined with the transmission gate logic. For a supply voltage of 1.8V the average power consumption (4.1563 µW) which is extremely low with moderately low delay (224 ps) resulting because of the deliberate incorporation of very weak CMOS inverters coupled with strong transmission gates. At 1.2V supply the power and delay were recorded to be 1.17664 µW and 91.3 ps. The design was implemented using 1-bit which can also be extended into a 32-bit design later. The designed implementation offers a better performance in terms of power and speed compared to the existing full adder design styles. The circuits were implemented in DSCH2 and Microwind tools respectively. The parameters such as power, delay, layout area and speed of the proposed circuit design is compared with pass transistor logic, adiabatic logic, transmission gate adder and so on. The circuit is also designed with a decrease in transistors in order to get the better results. Full Subtractor, a combinational digital circuit which performs 1-bit subtraction with borrow in is designed as a part of this project. The main aim behind this part of the project is to design a 1-bit full Subtractor using CMOS technology with reduced number of transistors and hence the efficiency in terms of area, power and speed have been calculated is designed using 8,10,15and 16 transistors. The parameters were calculated in each case and the results have been tabulated.

Keywords: EX-OR, EX-NOR, PDP, Carry propagation adder, high speed, hybrid design, low power, 1-bit half Subtractor, 1-bit full Subtractor

1. Introduction

The adder is one of the most important components of a CPU, ALU, floating-point and address units like cache or memory access unit. Used exclusively in VLSI systems as the advanced circuits, including microprocessors, digital communication gadgets and DSP processors. In addition to the main task of an adder i.e., performing OR between two binary numbers, which is the most vital block in the electronic system that performs arithmetic operations such as multiplication, subtraction, division, calculating address. Also, the increased usage of portable devices that operate on batteries like cellular phones, personal digital assistants often demand VLSI and ULSI which improve consumption of power and delay characteristics of the design. Increased growth in technologies in mobile communication and computing, there has arrived the demand of constructing low power VLSI systems. Full adders are the fundamental building blocks in this regard which is focused over the years. The logic style that possesses both pros and cons are used to implement 1-bit adders. The implementations which every low power VLSI system utilizes are categorized as: (i) Static Design Flow and (ii) Dynamic Design Flow. Static Full Adders work as more advantageous in terms of power, reliability, and its simplicity but the area it occupies over a chip is usually too large compared to its dynamic counterpart [3], [4]. Full adders are divided into two groups. The group which has full swing output include CCMOS, CPL, TGA, TFA, Hybrid, 14T, and 16T. Second group full adders comprise of full adders without full swing outputs. This full adder has less number of transistors based upon XOR-XNOR, low power consumption, and less area. Different logic styles favour at least one of the performance aspects when compared with each other to design a low power circuit. So in order to achieve a low power circuit that overcomes the drawback of each design style we do require a logic style in a combination of one or more. Standard CMOS, Transmission Gate Adder (TGA), dynamic CMOS and CPL are considered as the important logic styles under conventional domain. The adders which use one or more logic styles are known as hybrid logic styles. S5 Batch 10 2 A conventional complementary MOS FA has 28 transistors which is advantageous in terms of its robustness over scaling voltages and sizing of transistors; while requirement of a buffer, input capacitance serve as a disadvantage. Mirror adder , another complementary cell do come up with the same results of power consumption and transistor sizing by using the same number of transistors as a conventional CMOS does whereas the maximum propagation path inside the cell is smaller than a conventional CMOS FA circuit. Whereas, a CPL results efficient voltage swing restoration which obtained by employment of 32 transistors. However, CPL cannot be used in this case of building low power applications/circuitry. As such CPL constitutes of high switching

activity, more number of transistors, static inverters, more number of inputs are the disadvantages of CPL approach. The main consequence of CPL is voltage degradation which the transmission gate adder successfully addressed without these drawbacks because a TGA uses only 20 transistors to implement a full adder. Also, disadvantages being slower and higher consumption of power is considered by every researcher in low-power applications field. Later the researchers focused on eliminating all the demerits in each logic style adders by coming up with the hybrid approach to get the better performance of the adder as a whole.

2. Design of the Proposed Full Adder

2.1 CMOS Logic

The CMOS logic uses p-type and n-type MOSFETs for various logic functions used to construct an integrated circuit (IC) chips that are used in microprocessors, microcontrollers, memory cells and various other digital circuits. CMOS is also used in analog circuits that include image sensors, RF, data converters for various types of communication. Full Adder using CMOS the CMOS logic style is used to implement full adder for 1-bit to get low power. Generally, they are divided into two: Complementary CMOS and PTL circuits. The complementary CMOS full adder in Fig 2.1 is based on CMOS structure. The advantages of C-CMOS are robustness upon scaling of voltage and sizing of the transistors.
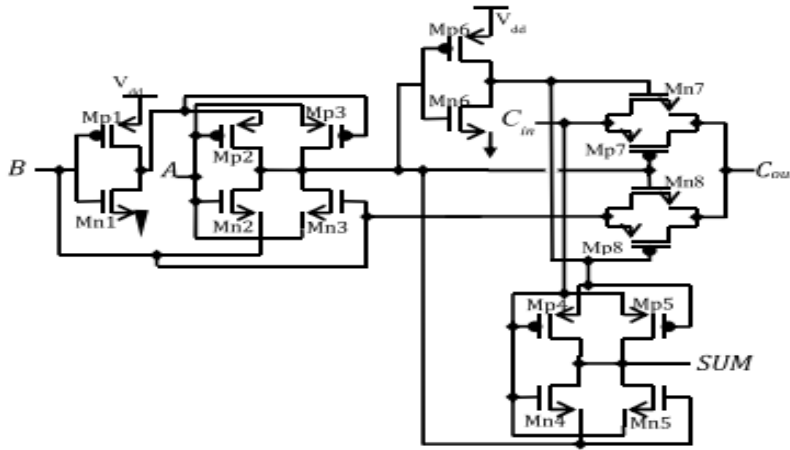

Figure 2.1. Proposed Circuits

2.2 Full Adder using PTL

A full adder can be designed by using PTL by connecting the NMOS PTL with a MUX. It varies with TGA as we do not utilize PMOS parallel to NMOS. A full adder can be designed using PTL in connection with MUX logic, XOR or XNOR logic which reduces the transistor count and also the delay in output as shown in Fig 2.2.
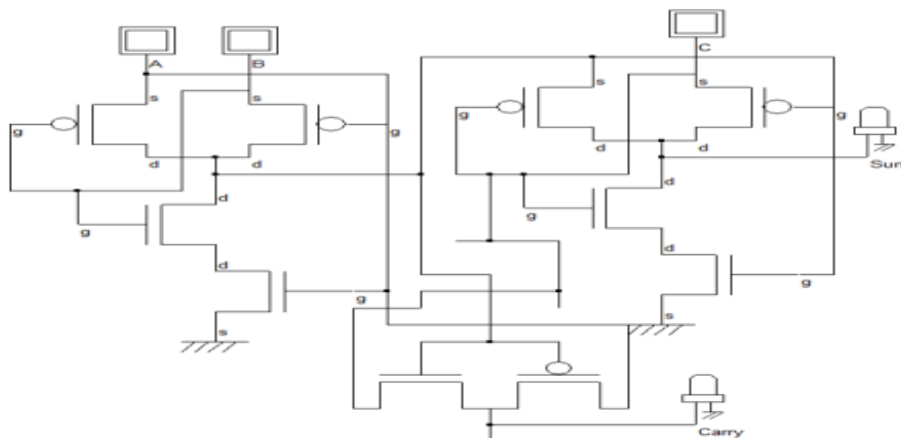

Figure2.2. Full adder using PTL

2.3 Transmission Gate Adder

The TGA has an n-channel and p-channel with connections for the source and the drain whereas a different gate connection. It has 20 transistors, which are transmission gates, p-type MOSFETs, n-type MOSFETs. The transmission gates enable circuit to work on higher speeds and lower power dissipation. Transmission gate operates like a switch with low resistance and capacitance where DC characteristic of gate is irrespective of the input as shown in Fig 2.3.. It connects both source to source and drain to drain terminals of NMOS and PMOS transistors respectively. When NMOS transistor is passing '0' signal, it discharges the output level as zero and P type MOS transistors pass '1' signals towards output it charges output towards logic high, enable signals used to turn on/off the two transistors at a time.
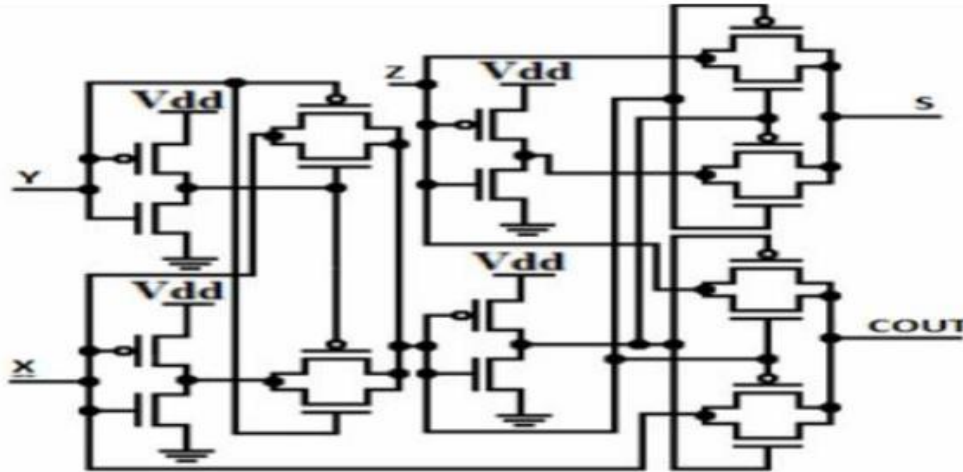

Figure2.3. Full Adder using Transmission Gate

2.4 Hybrid Logic Style

A hybrid circuit is designed by combining one or more modules where each module uses a different logic style. Every module has been designed separately to analyze parameters such as power and delay of circuits. The advantage of the hybrid logic style in a circuit is that it creates a short path for between the nodes of input and the output with a decrease in the delay of the circuit.There are three modules in which MOD1 and MOD3 are the EXNOR modules which implement the Sum output, whereas MOD2 is the carry generation module which is used to reduce delay and creates short paths. Out of the two EXNOR modules, one is implemented by using PTL (2T) which reduce the transistor count and consumption of power. Following EXNOR module is implemented using transmission gates (4T). Hence the total 6T circuitry built using the EXNOR modules reduce the power and gives the sum output with a decrease in the transistor count and high speed in comparison to the conventional EXNOR module as shown in Fig 2.4. The carry generation module is implemented using four transistors. The input signal flows through a single transmission gate which reduces the propagation path of a carry signal and reduces the delay of carry signal.
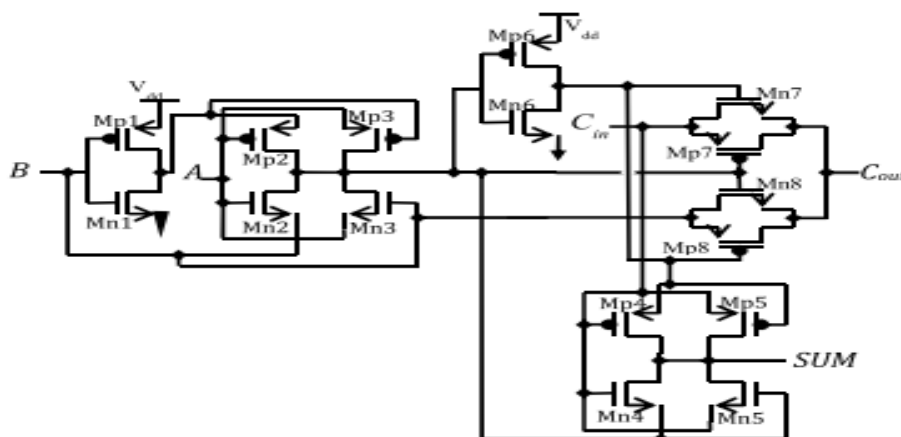

Figure2.4. Hybrid Full Adders

3. Simulation Results

3.1 Simulation Setup

The 1-bit full adder that has been implemented is designed using three different modules where MOD1 and MOD2 are used for SUM signal generation (Sum) and MOD3 alone for the output CARRY signal (Cout). Modules 1 and 2 use XNOR module whereas carry module is separately designed to optimize circuit in area of power, delay and chip area as a whole.The XNOR module in this circuit is mostly accountable for the power consumption for the entire adder circuit. Hence, the module is designed to lower the power to the possible extent. The below Fig 3.1, 3.2 and 3.3 depicts the circuit designed using XNOR module for sum generation. Power consumption of XNOR circuit is reduced using the inverter channel formed. Transistors Mp3 and Mn3 act as transistors that restore the level which guarantee full swing levels for the output signals. The XOR/XNOR topologies which use four transistors come up at the cost of low logic swing. On the contrary, the XOR/XNOR module in uses six transistors to obtain better logic swing to that of four transistor XOR/XNOR. The XNOR presented in the project offers low-power, high-speed compared to the six transistors XOR/XNOR.The carry signal obtained at the output for the proposed circuit is implemented as below. The transmission gate consisting of certain transistors propagate the carry signal (Cin) which reduces entire carry propagation path. Also, the purpose of transmission gates guarantee reduction in the propagation delay of output signal (Cout).
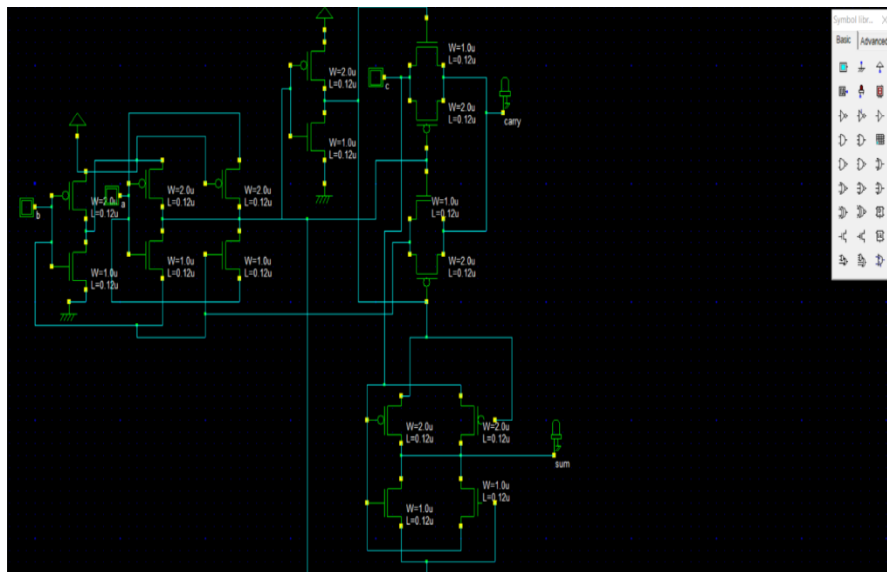

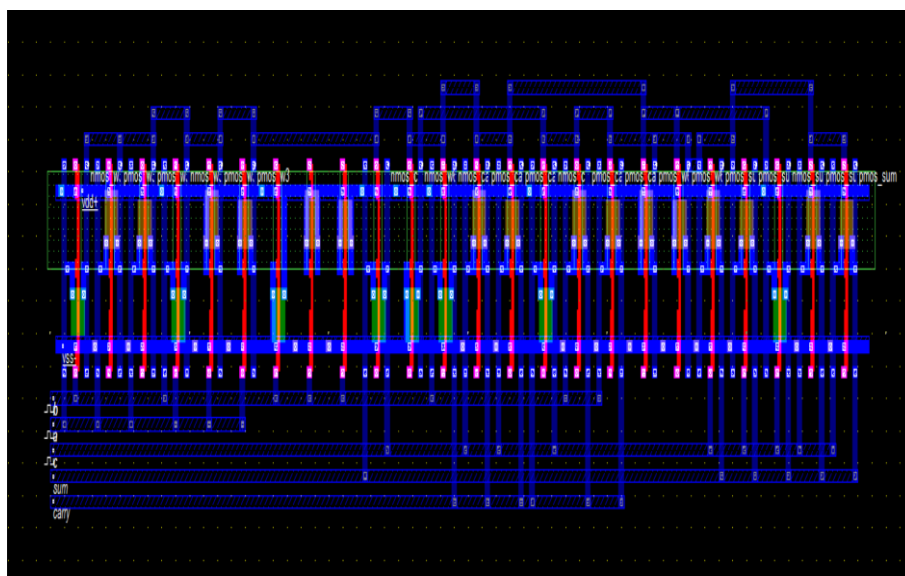**Figure 3.1.**Circuit design for 1-bit Full Adder

Figure 3.2. Layout Design

Figure 3.3. Simulation Results

4. Experimental Results

The experimental results for the above simulated adder circuits and the Subtractor circuits are tabulated below. A clear investigation in the delay, transistor count and the power consumed gives a clear image defining the circuit technology which is better than the others by the comparing power and delay individually as shown in Fig 4.1 and 4.2.
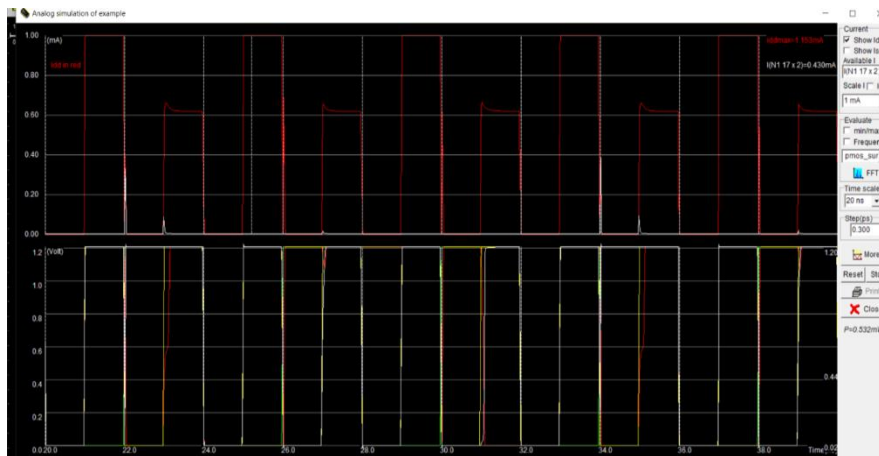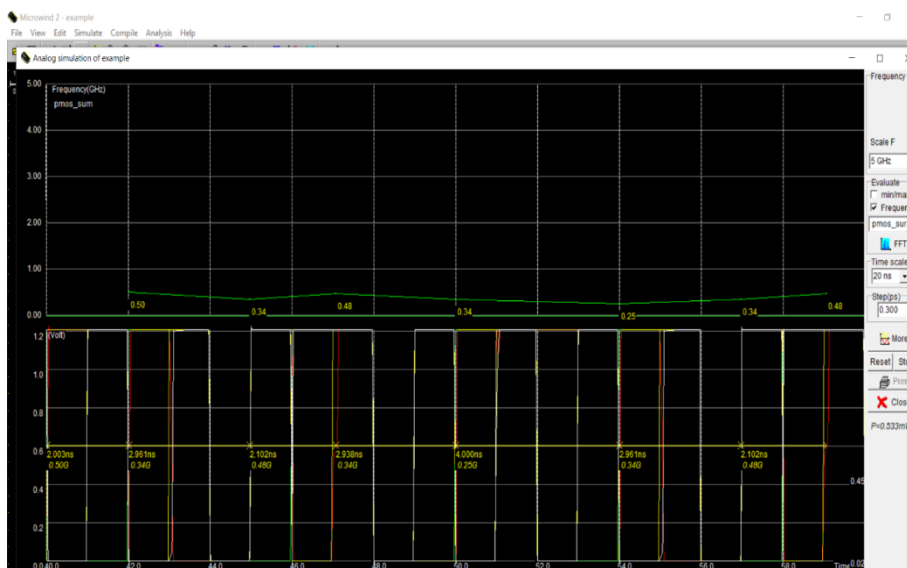

Figure 4.1. Voltages and current

Figure 4.2. Frequency vs Time

5. Discussion of Results

This project deals with the design of 1-bit Full Adder circuit with 10, 14, 20 transistors. Lowering power dissipation, supply voltage, leakage currents area of chip are the important parameters that are concentrated in the field of low power VLSI. A system's reliability can be made high by reducing the cost, weight and size and is achieved by decreasing the number of transistors. Thus, the lower power consumption and less area can be met by a decrease in the chip size. Circuits can be minimized by two ways- human method and computational method. Proposed project 1-bit hybrid Full Adder through human method with 10, 14 and 20 transistors and simulations were performed. Lastly the simulation analysis was compared with the conventional Adder in terms of power consumption, delay, and area and power delay product. According to the simulation results, we can say that as the number of transistors increase, the power delay product (PDP) also known as energy consumed by the circuital design automatically increases which does not follow the law of low power systems. Also, we have designed 1-bit Full Subtractor with 8, 15 and 20 transistors. Decreasing the Power dissipation, supply voltage, leakage currents, area of chip are the most important parameters that are concentrated in the field of low power VLSI. A system's reliability may be increased by reducing the cost, weight and physical size and it is achieved by decreasing the number of transistors. Thus, the power consumption and lower area can be met by decreasing the chip size. Circuits can be minimized by two ways- human method and computational method. Proposed project 1-bit hybrid Full Adder through human method with 10,14 and 20 transistors and simulations were performed. Lastly the simulation analysis was compared with the conventional Adder in terms of power consumption, delay, area and power delay product. According to the simulation results, we can say that as the number of transistors increase, the power delay product (PDP) also known as energy consumed by the circuital design automatically increases which does not follow the law of low power systems as shown in table1.

Table1. Power Dissipation of Designs

Design	Average Power	Delay(Ps)	PDP	No of transistors
1-bit FA	0.533mW	45	23.985	16
10T FA	6.719μW	26	17.464	10
14T FA	11.054μW	20	21.08	14
20T FA	0.255mW	10	1.02	20
24T FA	0.383mW	48	18.384	24
1-bit FS	2.935μW	7	20.545	14
14T FS	3.130μW	14	42.84	14
15T FS	1.661μW	20	33.22	15
2-bit FS	19.171μW	25	14.275	24
TGA	0.117μW	24	2.808	20
Adiabatic	8.094μW	14	13.316	15

6. Justification

Proposed 1-bit adders have lowest power consumption when compared with other simulated adder circuits. The results are described above table. The average power consumption of proposed 1-bit adder circuit is 0.522 mW, was reduced essentially by using consolidation CMOS inverters combined with solid transmission gates for 1.2 V supply voltage. Rise time and fall time of input signals in all simulations are 5% of the pulse width. It has shown that the proposed one and CMOS full adders are most power efficient cells. Proposed one is faster than the CMOS and a result, these are exhibits smaller power delay product and results are enunciated. The power delay product is fundamental parameter which is often used for measuring the quality and performance of a circuit. The average power utilization is measures in the similar input settings and a similar input range as for the propagation delay estimation. Among all the full adder circuits, proposed full adder 1 has a minimum PDP, which proved significantly improved 52% with respect to CMOS & CPL implementations, 57% with respect to the branch based logic-pass transistor implementation and 62% with respect to the TFA & TGA circuits.

7. Conclusion

The performance analysis of a low-power high-speed hybrid full adder is calculated by implementing circuits of different techniques. Initially we have implemented a full adder with 10 transistors where power, delay of this circuit has been calculated. Followed by 14 transistors and 20 transistors, the same process has been followed

and the power delay product has been calculated. The proposed hybrid circuit is implemented and the same is calculated in order to compare the results individually. The full Subtractor circuit with 8 transistors, 15 transistors, 20 transistors and the proposed circuit has been implemented in the second part of this project. The same results have been compared as a whole and with the help of timing diagrams we were able to obtain power and delay values. This project dealt with the design of a full adder in DSCH2 and Microwind tools. The proposed hybrid circuit was compared with the existing circuits in terms of power dissipation, delay and layout area depending upon transistor sizing. It is observed that the same project when carried out in either mentor graphics or cadence tools has better simulation results in view of the exact power consumption and delay parameters. Also, the area of the circuit depends upon the transistor sizing.

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