Research Article

Mitigation of Unbalance Voltages for Islanded Micro-Grids by using Five Level Diode Clamped Multilevel Inverter

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ABSTRACT— In this paper, a control strategy for paralleled three-phase inverters is proposed. The proposed local controller includes inner loop controller and droop controller and virtual impedance and unbalance compensator. The voltage/current controllers are to better mitigate voltage distortion when supplying non linear loads. Linear and non liner loads are to accurate current sharing for droop controller and virtual impedance. According to the amplitude of the negative sequence voltage by adjusting voltage reference. Compensation signal is sent to the DGs local controller, unbalance factor is reduced significantly. Unbalance is caused by single phase generators. It can be mitigated to an extremely low. In order to proposed control strategy for ac micro-grid consist of three three phase three leg inverters.

Index terms—voltage unbalances compensation, inner loop controllers, virtual impedance droop control, micro-grids

I. INTRODUCTION

Now a days, Distributed energy resources (DERs), like wind power, photovoltaic systems and micro -turbines, have gain a great increasing interest where they are economic and environment friendly. Power electronic converters are used as interfaces between DERs and the grid [1], such that electrical power with good quality and high reliability can be delivered to the load or utility grid, as shown in Fig. 1. This paper mainly focuses on islanded microgrids, the interfacing converters mainly operate as voltage source. This are participate on the voltage and frequency regulation and sharing at the same time active and reactive power accurately by adjusting output voltage. Converters are could provide power quality management ability and we can take full use of the converters available capacity. In modern system power quality issues are major problem, especially voltage/current unbalances and voltage/current distortions. For instance, in islanded microgrids, the voltage unbalance problem is a salient issue mainly produced by the use of single-phase generators/loads and it can lead to instability and power quality issues.

In order to several components are deal with the voltage unbalance compensation to enhance the voltage wave form quality, such as static var compensator (STATCOM) [2], series active power filter [3] and shunt active power filter [4]. Compensation methods are utilizing additional power converters to inject negative sequence reactive power. the unbalanced voltage by utilizing the DG interfacing converters. In [5], the DG inverter is controlled to inject negative sequence current to balance the common bus voltage. However, a surplus converter capacity is needed to generate the negative sequence current and the injecting current might be too high under severe unbalance conditions. In [6], Unbalance compensation method is proposed by sending proper control signals to DGs local controllers. However, the negative sequence component of the common bus voltage is hard to suppress, since the microgrid central controller (MGCC) uses the voltage unbalance factor as a main control variable, which value is reduced by the positive sequence voltage.

This paper proposes a control scheme located on the MGCC, those are directly acts over the negative sequence voltage. Section II will investigate the control designs of local controller, these are mainly including inner voltage/current loop, virtual impedance loop and droop controller, and then the system modeling is introduced. Section III elaborates on the strategy of the proposed direct voltage unbalance compensator. Simulation model and results of a three paralleled inverter systems is analyzed and discussed in section IV. Finally, conclusions are presented in section V

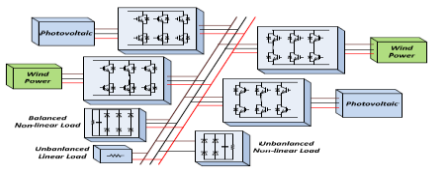

Fig .1. Architecture of a Micro grid

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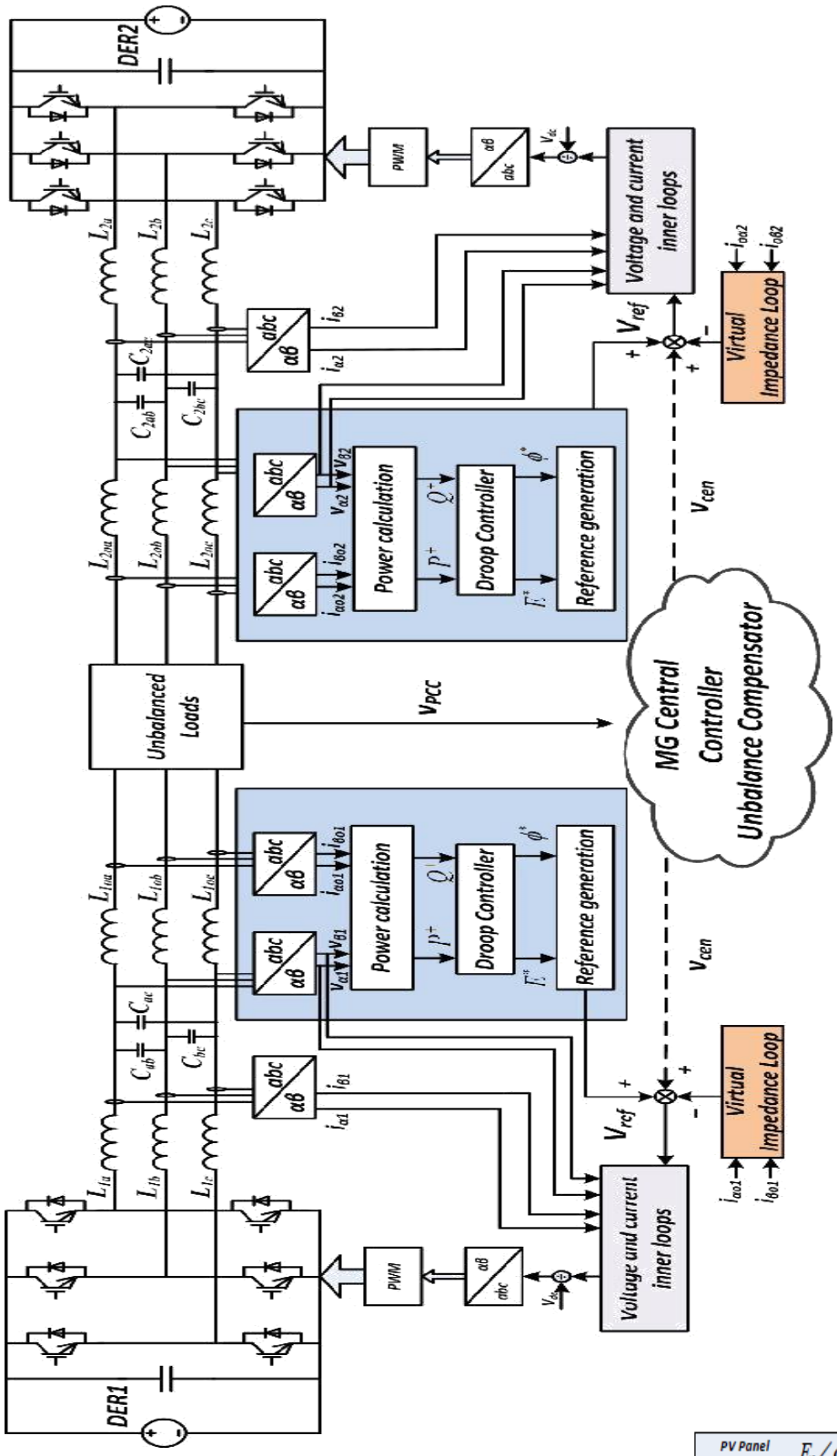

Fig .2. Block diagram of the local controllers

It can be seen from Fig. 2 that the control strategy of inverter local controllers. LCL filter is adopted and actually operates as a conventional LC filter with a coupling inductor. The grid side inductor is to optimize the dynamic performance and to shape the output impedance. Also its current is measured for power calculation. Local controller consists of three loops they

II. DESIGN OF CONTROLLER

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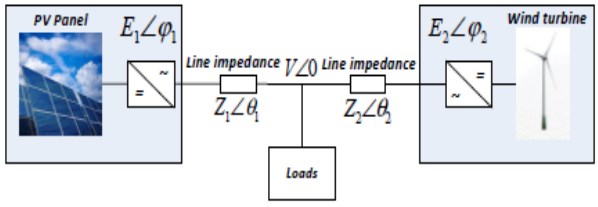
A. Voltage and current inner loop

The inner loops are implemented in two -phase stationary frame and all the measured voltage and current are transformed from *abc* to *αβ* coordinates as shown in Fig. 2, thus the computational burden is



reduced. Inner controllers are based on proportional+ resonant (*PR*) controller instead of the conventional proportional+ integrator (*PI*) controller. The reason is that *PR* controller can provide infinite gain at the selected resonant frequency to provide satisfactory tracking performance. In order to mitigate the voltage and current distortion under nonlinear loads, the *PR* controllers are tuned at fundamental frequency, 3rd, 5th, 7th, 9th and 11th order harmonics.In other words, the performance of *PR* controller at selected resonant frequency is conceptually similar to the performance of *PI* controller at 0Hz [7-9]

Implementation of the main power circuit and the inner loop controller in synchronous reference frame is established. In order to obtain the close loop transfer function, by using *abc/αβ* transformation in the power plant. Neglecting the zero quadrature components.

According to the small signal model, the control scheme can be depicted in Fig.3. The close loop transfer function is derived in (1):

$$v_c(s) = v_o^*(s) - Z_o(s)i_o(s) = \frac{G_v(s)G_i(s)G_{PWM}(s)}{LCs^2 + CG_i(s)G_{PWM}(s)s + G_v(s)G_i(s)G_{PWM}(s) + 1} v_{ref}(s) - \frac{Ls + G_i(s)G_{PWM}(s)}{LCs^2 + CG_i(s)G_{PWM}(s)s + G_v(s)G_i(s)G_{PWM}(S) + 1} i_{o(s)} \quad (1)$$

where $v_c(s)$ is the capacitor voltage, $v_o^*(s)$ is the open circuit voltage, $i_o(s)$ is the output current, $Z_o(s)$ is the equivalent output impedance, $v_{ref}(s)$ is the voltage reference,

L is the converter side inductor, C is the filter capacitor. $G_v(s)$, $G_i(s)$ and $G_{PWM}(s)$ are the transfer function of voltage controller, current controller and *PWM* delay, respectively. Their transfer function can be expressed as:

$$G(s) = k_v + \sum_{h=1,3,5,7,9,11} k_{hvr} \frac{s}{s^2+(hw)^2} \quad (2)$$

$$G(s) = k_{ip} + \sum_{h=1,3,5,7,9,11} k_{hir} \frac{s}{s^2+(hw)^2} \quad (3)$$

$$G_{PWM}(s) = \frac{1}{1+1.5T_s s} \quad (4)$$

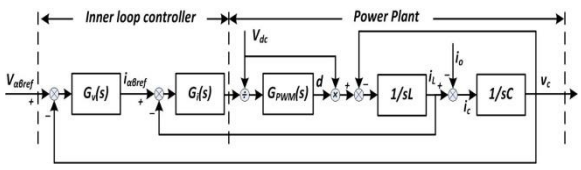


Fig .3. Control block diagram of the inverter.

Where k_{vp} and k_{hvr} are the proportion coefficients and

Fig. 4. Equivalent circuit of two parallel DGs

resonant coefficients (1st, 3rd, 5th, 7th, 9th and 11th) of voltage controller respectively. k_{ip} and k_{hir} are the proportional coefficients and resonant coefficients (1st, 3 rd, 5th, 7th, 9th and 11th) of current controller respectively; ω is the fundamental angular frequency while T_s is the sampling time.

B.Droop Control

Drop control is adapted in this paper. To avoid circulating currents among the parallel inverters without using communication link. To illustrates droop control theory, assuming two inverters connected in parallel and sharing loads at the common node. The circuit diagram as shown in Fig. 4.

From Fig. 4, the active power P and reactive power Q injected by each DG can be express in (5) and (6), respectively.

$$P_i = \left(\frac{E_i V}{Z_i}\cos\varphi_i - \frac{V^2}{Z_i}\right)\cos\theta + \frac{E_i V}{Z_i}\sin\varphi_i \sin\theta \qquad (5)$$

$$Q_i = \left(\frac{E_I V}{Z_i}\cos\varphi_i - \frac{V^2}{Z_i}\right)\sin\theta - \frac{E_i V}{Z_i}\sin\varphi\cos\theta \qquad (6)$$

Where E_i and φ_i are the amplitude and the phase angle of the output voltage of the each inverter, Z_i and θ_i are the amplitude and phase angle of the line impedance of each inverter, respectively. V is the voltage amplitude of common AC bus. Phase angle of common AC bus voltage is taken as the phase reference.

Where line impedance is mainly inductive, i.e. $Z_i \angle\theta_i \approx X_i \angle 90^\circ$. Furthermore, assuming the phase difference φ_i between inverter voltage and AC bus voltage is small enough, so that $\sin\varphi_i$ can be approximately equal to φ_i and $cos\varphi_i$ can be approximately equal to 1. Then, from (5) and (6), the following approximations can be obtained:

$$P_i \approx \frac{E_i V}{X_i}\varphi_i \qquad (7)$$

$$Q_i \approx \frac{E_i V}{X_i}\sin\theta - \frac{V^2}{X_i} \qquad (8)$$

From (7) can be seen that active power P_i is dominant by phase angle φ_i. From (8) can be seen that reactive power is mainly depend on inverter voltage E_i. Then, an artificial droop is introduced here to adjust the frequency and amplitude of the output voltage dynamically:

$$\varphi^* = \varphi_o - \left(m_p + \frac{m_1}{s}\right)\left(p^+ - p^+_{ref}\right) \qquad (9)$$

$$E^* = E_O - n_p\left(Q^+ - Q^+_{ref}\right) \qquad (10)$$

Where φ^* and E^* are the amplitude and phase angle of the output voltage reference, E_0 and φ_0 are the amplitude and phase angle of the output voltage at no load condition. P^+ and Q^+ are the instantaneous fundamental positive sequence active and reactive power, respectively, and P^+_{ref} are Q^+_{ref} are the reference of fundamental positive sequence active and reactive power, respectively; m_p and m_I are the proportional and integral coefficients of active power controller, respectively. m_I mainly influence the dynamic characteristic of the system ; n_p is the integral coefficients of reactive power controller.

It can be seen from (7) and (10) that the higher the droop coefficients is the better power sharing can be achieved. However the voltage and frequency deviation will also become larger when droop coefficients become bigger. This can be compensated by introducing secondary controller, as illustrated in [10]. Hence, both the proportional coefficients should be carefully selected according to (11) and (12):

$$m_p = \frac{\Delta f}{P} \qquad (11)$$

$$n_p = \frac{\Delta E}{Q} \qquad (12)$$

Where Δf and ΔE are the maximum allowable deviation of frequency and amplitude from its nominal value, respectively. P and Q are the rated active and reactive power.

The implementation block diagram of the droop controller is shown in Fig.5. The power calculation block, based on the instantaneous reactive power theory [13], is followed by a low pass filter, so that the power oscillation can be filtered out.

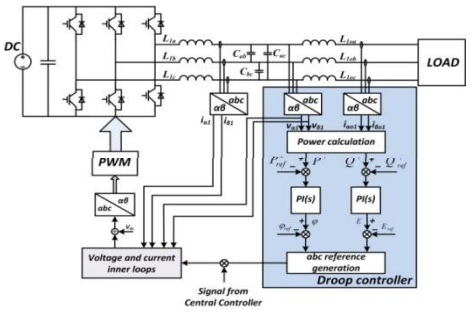


Fig.5. Implementation of the droop controller.

C.Virtual Impedance Loop

In order to share the power precisely between the distributed inverters, the output impedance of the inverter must be re-designed to mitigate the influence of control parameters and line impedance on the power sharing accuracy. Here, (1) can be rewritten as:

$$v_c(s) = G(s)v_{ref}(s) - Z_o(s)i_o(s) \qquad (13)$$

Where $G(s)$ represents the close loop transfer function of the inverter, and $Z_o(s)$ represents the close loop output impedance of the inverter. From the above equation, a two-

terminal *Thevenin* equivalent circuit of the close loop inverter can be obtained, as shown in Fig. 6.

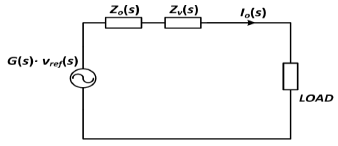


Fig.6. Thevenin equivalent circuit of the close loop inverter.

If no control loop is implemented to compensate the output impedance, the amplitude of the output impedance at fundamental frequency and 3rd, 5th, 7 th, 9th and 11th order harmonics is extremely small.

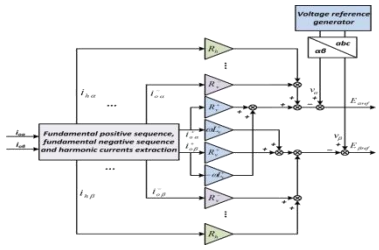


Fig. 7. Block diagram of the virtual impedance.

A Positive-sequence virtual inductor L^{+}_{v} is added to make the output impedance more inductive, so a better decoupling of *P* and *Q*. where adding the positive-sequence virtual resistor R^{+}_{v} , the system is more damped, so that the output current can be limited within an acceptable range.

Fundamental negative sequence and each order of the harmonics, a resistor is emulated at the output side to enhance the sharing of nonlinear load sharing among the DGs. Compared with using a real resistor, the virtual resistor has the advantage of no power losses and the possibility to select harmonics and sequences. The virtual impedance loop consists of three main parts, is illustrated in Fig.7. The first part is fundamental positive sequence virtual impedance loop, which only introduces virtual resistor R^{+}_{v} and virtual inductor L^{+}_{v} to fundamental positive sequence current. The second part is fundamental negative sequence virtual impedance loop which introduces virtual resistor R^{-}_{v} to fundamental negative sequence current. The third part is harmonic virtual impedance loop which introduces virtual resistor R_h to 3 rd, 5th, 7th, 9th and 11th order harmonics, respectively. Note that ω is the nominal angular frequency of the system.

Thus, the value of the virtual impedances must be selected carefully to ensure a well power sharing accuracy, and meanwhile guarantee the voltage Total Harmonic Distortion (*THD*) is limited in an acceptable range. It is worth noting that there is a tradeoff between the nonlinear current sharing accuracy and inverters output voltage distortion. This voltage distortion originates from the voltage drop on the virtual impedances. In addition, voltage distortion caused by virtual impedance is also the reason for separating the virtual impedance of harmonic and fundamental negative sequence component with fundamental positive sequence component, so that the virtual impedance of fundamental negative sequence and harmonic components can be set to a larger value.

III. UNBALANCE COMPENSATOR DESIGN

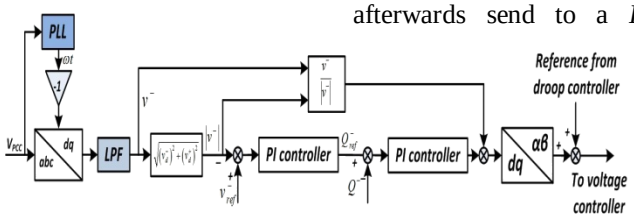
The voltage unbalance compensation method is improved in terms of controlling the negative sequence voltage directly. As shown in Fig. 2, the reference of voltage controller is the superposition of the output of unbalance compensator and droop controller.

The mathematical description of the unbalance compensator implemented in synchronous reference (*dq*) frame is shown in (14):

$$v_{cen} = \left[(|v^{-}|_{ref} - \sqrt{v^{-}_{d} + v^{-}_{q}}).PI_1(s) - Q^{-}\right].PI_2(s).\frac{v^{-}_{dq}}{\sqrt{v^{-}_{d}+v^{-}_{q}}} \qquad (14)$$

where v_{cen} is the control signal send to inverter local controller,$|v^{-}|_{ref}$ is the reference of negative sequence voltage, Q^{-} is the negative sequence reactive power at point of common coupling (*PCC)*, v^{-}_{d} and v^{-}_{q} are the *dq* components of negative sequence voltage respectively, $PI_1(s)$ and $PI_2(s)$ are the negative sequence voltage controllers, respectively. The voltage unbalance level is mitigated by controlling the *PCC* voltage directly while the negative sequence reactive power injection is controlled indirectly.

Control diagram of the unbalance compensator as shown in Fig. 8. As it can be seen, *dq* components of the negative sequence voltage at *PCC* is first extracted by rotating V_{PCC} with negative angular frequency $-\omega$ and then followed by a *low pass filter* (LPF). The amplitude of negative sequence voltage $|v^{-}|$ is calculated with filtered v^{-}_{d} and v^{-}_{q} and is afterwards send to a *PI* controller to generate the reference of negative



. Fig 8.Block diagram of the proposed unbalance compensator.

sequence reactive power Q^{-}_{ref}. Another *PI* controller fed with the error of Q^{-}_{ref} and Q^{-} is implemented here to enhance the dynamic behavior of the unbalance compensator. Finally, the output of the *PI* controller is multiplied by normalized v^{-} and transformed to $\alpha\beta$

coordinates to generate the compensation signal which is send to the voltage loop controller.

TABLE I. PARAMETERS OF POWER PLANTS

Parameters	Symbol	Value	Unit
Converter Side Inductors	L_{con}	1.8	mH
Grid Side Inductors	L_g	1.8	mH
Capacitors	C	9	μF
Nominal Voltage	V	230	V
Nominal Frequency	f	50	Hz
DC Voltage	V_{DC}	650	V
Switching Frequency	f_s	10	kHz

TABLE II. CONTROL SYSTEM PARAMETERS

Voltage/Current Inner Loop Controllers		
Parameters	Symbol	Value
Voltage Loop Controller	k_{vp}, k_{vr}, k_{3vr} k_{5vr}, k_{7vr}, k_{9vr}, k_{11vr}	0.05, 90, 5, 5, 15, ,10, 20
Current Loop Controller	k_{ip}, k_{ir}, k_{3ir},k_{5ir}, k_{7ir}, k_{5ir}, k_{11vr}	5, 200, 20, 10, 10, 10 10

Primary Controller			
Parameters	Symbol	Value	Unit
Proportional Phase Droop	m_P	0.0005	Rad·s/W
Integral Phase Droop	m_I	0.00006	Rad/W
Proportional Phase Droop	n_P	0.002	V/Var
Virtual Resistor	R_v, R_v, R_3, R_5, R_7, R_9, R_{11}	1, 4, 4, 5, 5, 5, 5	Ω
Virtual Inductor	L_v	4	mH

Secondary Controller		
Parameters	Symbol	Value
Negative Sequence Voltage Reference	v_{ref}^-	0.5
Negative Sequence Voltage Controller	K_{p_vneg}, k_{i_vneg}	5, 0.01
Negative Sequence Power Controller	K_{p_Qneg}, k_{i_Qneg}	0.01, 0.5

IV. SIMULATION AND RESULTS

Using scopes and other display blocks, the simulation results while the simulation runs. The simulation results can be put in the MATLAB workspace for post processing and visualization. Model analysis tools include linearization and trimming tools, which can be accessed from the MATLAB command line, plus the many tools in MATLAB and its application toolboxes. Because MATLAB and Simulink are integrated, in order to simulate, analyze, and revise your models in either environment at any point. Local controllers are designing of simulation model as shown in Fig 9.

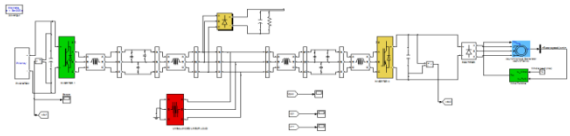


Fig .9. Design model of local controllers.

The correctness of the proposed control strategy, experiments have been carried out on a MG platform existing in the Microgrid Lab at Aalborg University [14]. The detailed control configuration is shown in Fig. 2. Unbalanced resistive loads are connected to the common AC bus to emulate unbalanced load conditions. Unbalanced linear load is connected to the common AC bus and lead to the flowing of negative sequence current. In addition, electrical setup and control system specifications can be found in Table I and Table II.

Unbalanced linear load is connected to the common AC bus and lead to the flowing of negative sequence current. Voltage unbalance appears on the PCC voltage as shown in Fig. 10. At the same time the output voltage of the DGs has good voltage quality. The DG output voltage of before and after compensation as shown in Fig.14 (a) and Fig.14 (b). The direct unbalance loop is enabled and then the corresponding compensation signal is sent to the DGs local controller. The unbalance factor is reduced as shown in Fig.11. It can be seen from Fig.10 and Fig.14 that the decrease of the PCC voltage unbalance factor is achieved by means of deteriorates the DGs output voltage. To better illustrate the effect of the unbalance compensator, the negative sequence voltage at PCC is shown inFig.12 and Fig.13. The PCC negative sequence voltage drops dramatically after the compensation enabled. Note that the unbalance factor (UF) is defined as (15):

$$UF = \sqrt{\frac{(v_d^-)^2 + (v_q^-)^2}{(v_d^+)^2 + (v_q^+)^2}}.100 \qquad (15)$$

Where v_d^+ and v_q^+ are the positive sequence of the PCC voltage respectively; v_d^- and v_q^- are the negative sequence of the PCC voltage respectively.

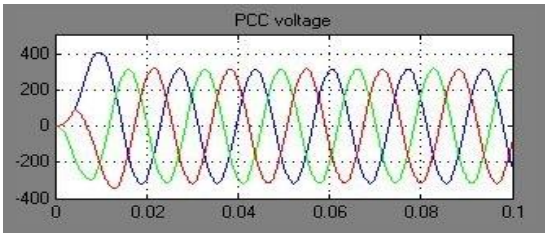


Fig.10. PCC voltage.

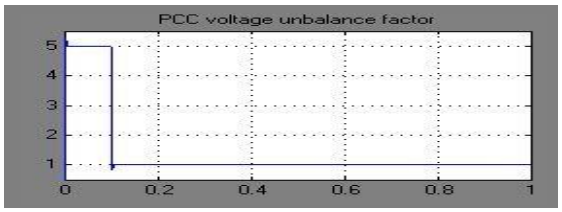


Fig.11. PCC voltage unbalance factor.

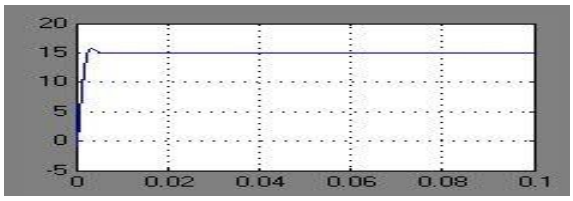


Fig.12. Negative sequence voltage of d component.

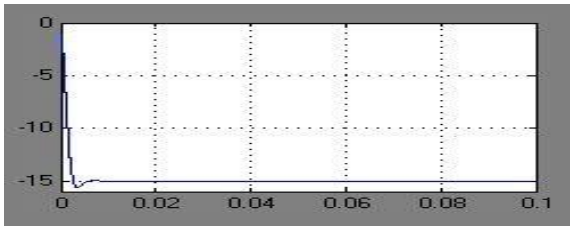


Fig.13. Negative sequence voltage of q component.

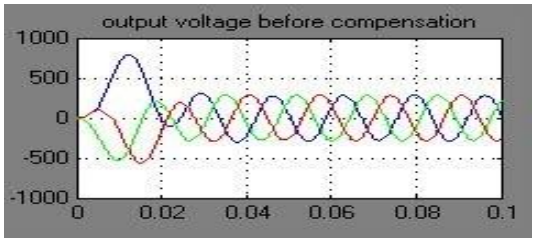


Fig.14 (a). DG Output voltage of before compensation.

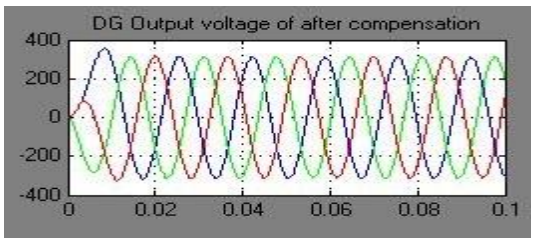


Fig.14 (b). DG output voltage of after compensation.

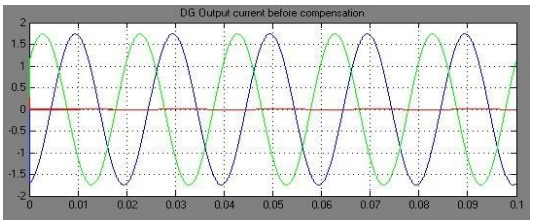


Fig.15 (a). DG Output current of before compensation.

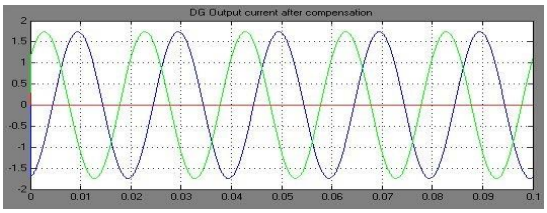


Fig.15 (b) DG Output current of after compensation.

In order to investigate the current sharing accuracy. The DG output current of before and after compensation as shown in Fig.15 (a) and Fig.15 (b). It can be seen, the output current can be shared properly among the DG converter. The current errors on DG converter are caused by the difference in line impedance.

V. CONCLUSIONS

In this paper, mitigation of unbalance voltages for islanded microgrids by using five level diode clamped multilevel inductor has been investigated. The control structure consists of two levels: first level is local controller and second level is direct voltage unbalance compensator. The local controller is takes care of the bus voltage regulation and power sharing accuracy. The direct voltage unbalance compensator contributes to better mitigate the voltage unbalance at the *PCC* by controlling the voltage reference. The effectiveness of the control scheme has been validated with three *LCL* DG converters. The results give the negative sequence voltage to satisfied load sharing accuracy.

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