A THREE LEVEL FULL BRIDGE ZERO VOLTAGE AND ZERO CURRENTSWITCHING CONVERTERS

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Abstract

Multilevel dc–dc converters making use of high frequency transformers are suitable for integration in solid-state solutions for applications in electric power distribution systems. This project presents a simplified switching scheme for three-level full-bridge dc–dc converters that enables zero-voltage and zero current switching of all the main power devices. It describes the main operational modes and design equations of the converter as well as provides simulation results to demonstrate the feasibility of the proposed ideas.

1. Introduction

Power-electronic inverters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years. The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output.

The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The multilevel inverter starts from three levels. As the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. Multilevel inverters synthesizing a large number of levels have a lot of merits such as improved output waveform, a smaller filter size, a lower EMI (Electro Magnetic Interference), and other advantages. The principle advantage of using multilevel inverters is the low harmonic distortion obtained due to the multiple voltage levels at the output and reduced stresses on the switching devices used.

2. Hard switching and Soft Switching Techniques

In the 1970's, conventional PWM power converters were operated in a switched mode operation. Power switches have to cut off the load current within the turn-on and turn-off times under the hard switching conditions. Hard switching refers to the stressful switching behavior of the power electronic devices. The switching trajectory of a hard-switched power device is shown

in Fig.2.1. During the turn-on and turn-off processes, the power device has to withstand high voltage and current simultaneously, resulting in high switching losses and stress. Dissipative passive snubbers are usually added to the power circuits so that the dv/dt and di/dt of the power devices could be reduced, and the switching loss and stress are diverted to the passive snubber circuits. However, the switching loss is proportional to the switching frequency, thus limiting the maximum switching frequency of the power converters. Typical converter switching frequency was limited to a few tens of kilo-Hertz (typically 20 kHz to 50 kHz) in early 1980's. The stray inductive and capacitive components in the power circuits and power devices still cause considerable transient effects, which in turn give rise to electromagnetic interference (EMI) problems. Fig.2.2 shows ideal switching waveforms and typical practical waveforms of the switch voltage. The transient ringing effects are major causes of EMI.

In the 1980's, lots of research efforts were diverted towards the use of resonant converters. The concept was to incorporate resonant tanks in the converters to create oscillatory (usually sinusoidal) voltage and/or current waveforms so that zero voltage switching (ZVS) or zero current switching (ZCS) conditions can be created for the power switches. The reduction of switching loss and the continual improvement of power switches allow the switching frequency of the resonant converters to reach hundreds of kilo-Hertz (typically 100 kHz to 500 kHz). Consequently, magnetic sizes can be reduced and the power density of the converters increased. Various forms of resonant converters have been proposed and developed. However, most of the resonant converters suffer several problems. When compared with the conventional PWM converters, the resonant current and voltage of resonant converters have high peak values, leading to higher conduction loss and higher V and I ratings requirements for the power devices. Also, many resonant converters require frequency modulation (FM) for output regulation. Variable switching frequency operation makes the filter design and control more complicated.

In late 1980's and throughout 1990's, further improvements have been made in converter technology. New generations of soft-switched converters that combine the advantages of conventional PWM converters and resonant converters have been developed. These soft-switched converters have switching waveforms similar to those of conventional PWM converters except that the rising and falling edges of the waveforms are 'smoothed' with no transient spikes. Unlike the resonant converters, new soft-switched converters usually utilize the resonance in a controlled manner.

Resonance is allowed to occur just before and during the turn-on and turn-off processes so as to create ZVS and ZCS conditions. Other than that, they behave just like conventional PWM converters. With simple modifications, many customized control integrated control (IC) circuits designed for conventional converters can be employed for soft-switched converters. Because the switching loss and stress have been reduced, soft-switched converter can be operated at the very high frequency (typically 500 kHz to a few Mega-Hertz).

Soft-switching converters also provide an effective solution to suppress EMI and have been applied to DC-DC, AC-DC and DC-AC converters. This chapter covers the basic technology of resonant and soft-switching converters. Various forms of soft-switching techniques such as ZVS, ZCS, voltage clamping, zero transition methods etc. are addressed. The emphasis is placed on the basic operating principle and practicality of the converters without using much mathematical analysis.

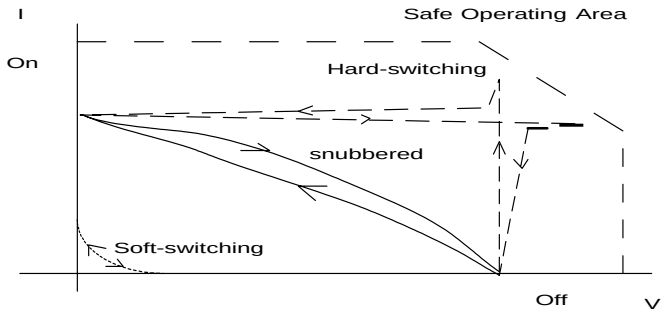
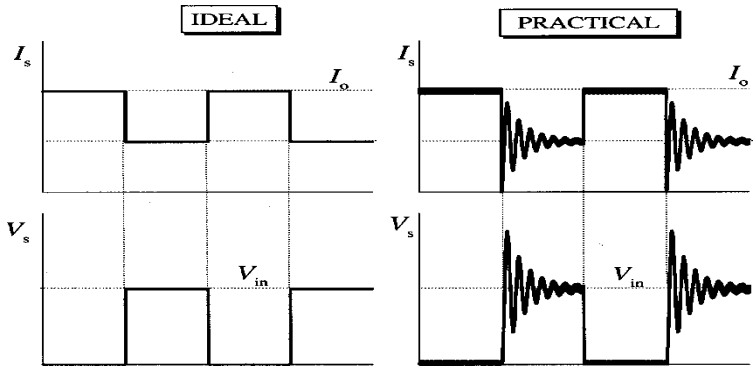


Fig.2.1 Typical switching trajectories of power switches.



1.

Fig.2.2. Typical switching waveforms of (a) hard-switched and

(b) soft-switched devices

3. Converter Operational Modes

Fig.3.1Shows the equivalent circuit for the first five of the ten operational modes since the subsequent five modes operates similarly to the first five modes, along with the sixth operational mode to show its similarity to the first. The following analysis assumes that the switching devices are ideal, the output filter is large enough to act as a constant current source for the entire period, and the blocking capacitor is large enough to act as a constant voltage source while the current is being reset.

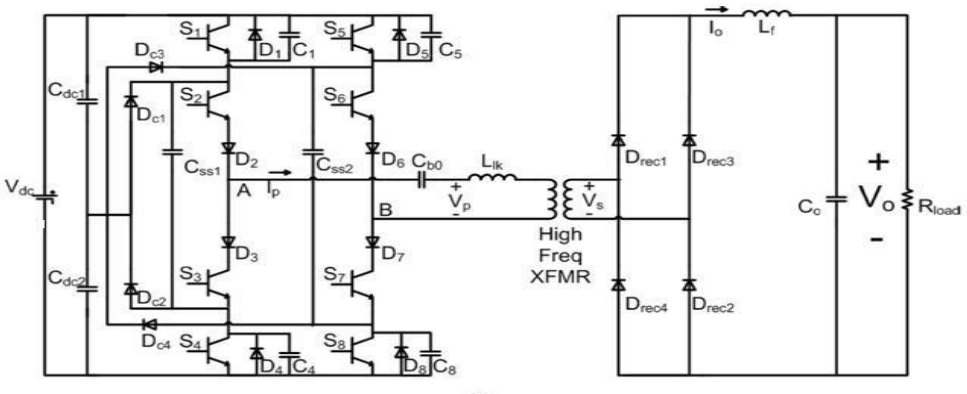


Fig 3.1 Schematic diagram for 3L FB ZVZCS converter

Mode 1: t0 ≤ t < t1

Switches S1 and S8have been ON for a (relatively) long time and Cb0 is charged to −Vcb0p. At t = 0, switches S2 and S7 begin conducting and (Vdc − Vcb0p) is applied to the primary of the transformer. As a result, the primary current rapidly rises from 0 to the reflected output current **Ip0** = Io/n.

Where Ip0 is the peak value of the primary side current going into the transformer, Io is the current through Lf, and n is the turn's ratio of the transformer. The voltage applied to the transformer leakage inductor Llk during this period is Vdc − (−VCb0) =Vdc + VCb0, and the duration of this period is t1 −0 = t1 = Llk × Ip0Vdc + VCb0

Since this period is so short, *vcb*0 is assumed to be constant throughout the period. The load current is not completely supplied by Vdc during this period, so the excess current freewheels through the secondary rectifier diodes Drec1–Drec4.

Mode 2: t1 ≤ t < t2:

The freewheeling mode ends when the primary current reaches Ip0 at t1 and diodesDrec3 and Drec4 stop conducting. The output filter is connected in series with the leakage inductance of the transformer throughDrec1 and Drec2, and acts to keep the primary current constant atIp0. Power is transferred from Vdc to the load during this mode. The duration of this mode is related to the voltage conversion ratio by the duty cycle parameter *D*, which is given by

V0/Vdc= D/n= ((ton)/ (Tsw /2))/n= ((t2 − t1)/ (Tsw /2)) n. Since interval t1 is so short, *ton* is set equal to t2 and D = t2/ (Tsw /2).The blocking capacitor is charged from −Vcb0p to +Vcb0p byIp0 during this mode.

Mode 3: t2 ≤ t < t3:

Switches S1 and S8are turned OFF at t2. Capacitors C1 and C8 are charged andC4 and C5 are discharged by ip, which is still held constant at Ip0 by the large output filter inductance. When C4 and C5are completely discharged at t3, the primary current begins to circulate through devices S2 and S7 and diodes Dc1 and Dc4. Switches S4 and S5 can be gated ON under complete ZVS at any time after t3.Since this mode is so short, vcb0 is assumed to remain constant at Vcb0p for the duration of this mode. Each of the parallel capacitors conducts Ip0/2 during this mode and has a change of voltage of Vdc/2. Using the same value Cr for capacitors C1, C4, C5, and C8, the duration of this mode is t3 − t2 = Cr × (Vdc/Ip0).

Mode 4: t3 ≤ t < t4:

As the primary current circulates through S2, S7, Dc1, and Dc4, the blocking capacitor voltage Vcb0p is applied to the transformer and the primary current begins to decrease. As soon as the primary current falls below Ip0, the output current begins to freewheel through the current is being reset. Output rectifier diodes, disconnecting the primary side of the circuit from the load and short circuiting the transformer magnetizing inductance. Thus, the reset time is dependent on the leakage inductance Treset = t4 − t3 = Llk × (Ip0/Vcb0p).

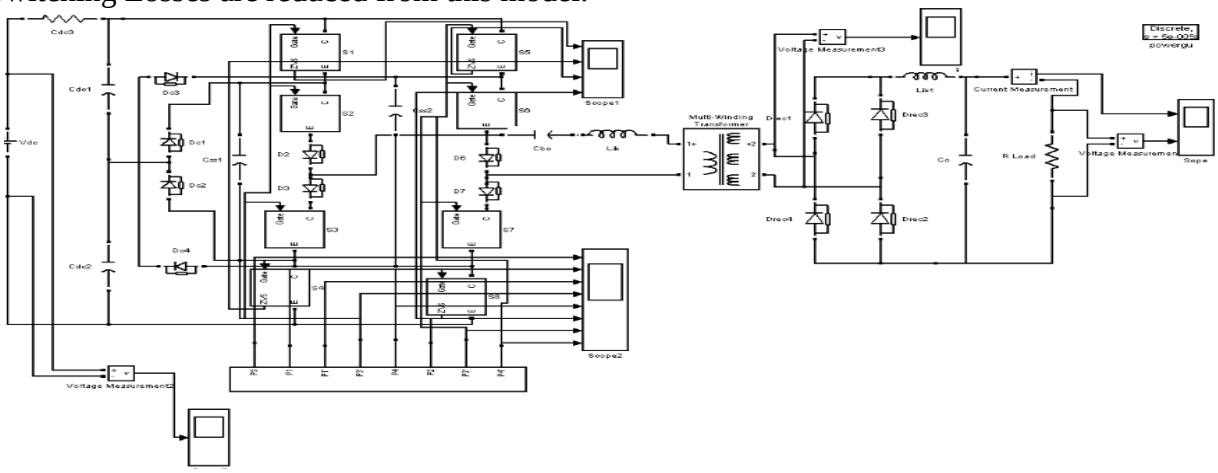
Mode 5: t4 ≤ t < Tsw /2:

Upon reaching zero, the current is prevented from flowing in the negative direction by the diodes D2 and D7. The output current continues to freewheel through the output rectifier diodes. The voltageVcb0p appears across the output terminals AB, so S1 and S8have to block (Vdc + Vcb0p)/2. At Tsw /2, S2 and S7 turn OFF under ZCS, and shortly afterward, S3 and S6 turn ON under ZCS. Since S4 and S5 are already ON, S3 and S6 conduct, and (−Vdc + Vcb0p) is applied to the primary of the transformer, beginning operational mode 6.

Modes 6–10 are similar to modes1–5 except for the reversal of the voltage and current signs

3. Simulation of Three-Phase Full Bridge ZVZCS

The dynamic model of Three-Phase Full Bridge ZVZCS is built by SIMULINK model. Switching Losses are reduced from this model.

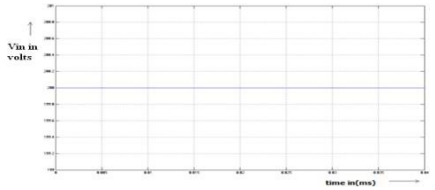


3.1 Simulation Results

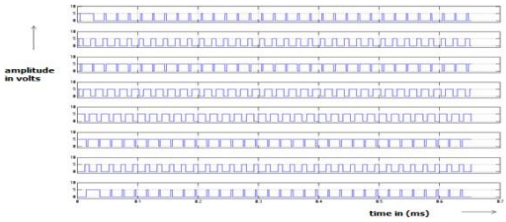
a) Parameters

Input voltage	200V
Switches (S1-S8)	IGBT
Capacitor utilized for the dc-bus (C_{dc})	2.2µF
Clamping capacitors (C_{ss})	1µF
Parallel capacitors (C1, C4, C5, C8)	4.7nF
Output filter inductor	1.7mH
Output filter capacitor	410nF
Transformer	1:1(ratio)
Output resistance (Ro)	10Ω

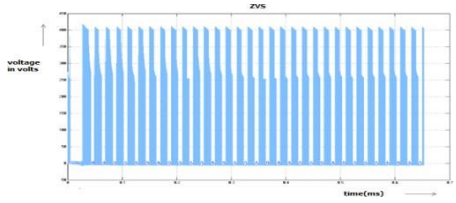
b) Input voltage



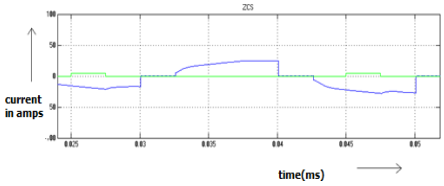
c) Triggering Pulses



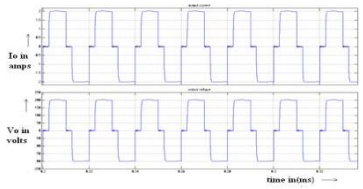
d) Zero Voltage Switching



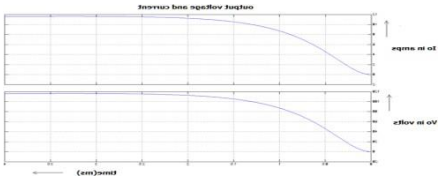
e) Zero Current Switching



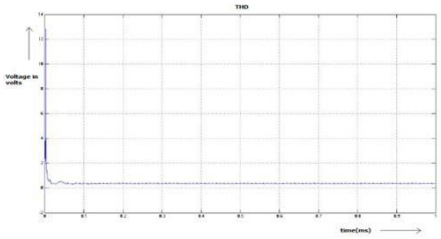
f) Three Level Inverter Outputs



g) Output Voltage & Output Current



h) Total Harmonic Distortion



4. Conclusion

This project proposed a (3L-5L) ZVZCS converter with a simplified switching scheme for use in solid-state solutions. The converter was shown to have the advantages of soft switching and reduced voltage stresses across the devices, allowing higher voltage operation. The operation of the (3L-5L) FB ZVZCS converter was analyzed. Simulation results further demonstrated the feasibility of the proposed ideas. Future research would include designing a prototype to implement an active clamp to reset the current thus eliminating the series diodes and the losses associated with them. This would have the added benefit of reducing the spikes from the rectifier diodes when the dc voltage is applied during modes 1 and 6. A $200V_{dc}/120V_{dc}$ have been simulated using MATLAB/simulink.

5. References

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