AN EFFICIENT BACK GATE BIASING SRAM ARRAY WITH ROW AND COLUMN BASED SELECTION

[1]SHAIK NANNU SAHEB, [2]Dr .RAMESH MARPU, [3]Dr.PRABODH KHAMPARIYA

[1]Research Scholar, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Madhya Pradesh, India
[2]Professor, Vaageswari College of Engineering, Karimnagar, Telangana, India.
[3]Reserach Guide, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Madhya Pradesh, India

ABSTRACT: One of the most indispensible parts of many modern VLSI (Very Large Scale Integration) designs is Static Random Access Memory (SRAM), due to its low consumption of power, higher speed and it dominates the silicon area in various applications. Normally the ICs (Integrated Chips) are most complicated for increasing the chip density and decreasing chip size. Hence for overcoming these issues the SRAM will be implemented. In this paper the efficient back gate biasing based SRAM Array with row and column selection is presented. Address decoder is used to generate the row address and column address. The novel low power 6T SRAM cell will be utilized for designing the SRAM array for improving the read stability. The energy efficiencies of SRAM will be attained with the wider structure of SRAM array with less number of rows compared to columns especially at less supply voltage. In 6T SRAM cell, the write operation is performed while charging and discharging the single BL (Bit Line), that will reduce the consumption of dynamic power. The simulation results will show that a better efficiency will be achieved for same bit density of SRAM as well as same supply voltage. SRAM array also reduces the area by minimizing the number of transistors used to implement SRAM array design.

KEY WORDS: SRAM (Static Random Access Memory), row and column selection, SRAM array.

I. INTRODUCTION

With these new technology nodes, the leakage share in cache total consumption of power and other SRAM-based memories significantly increases because the dynamic power decreases with scaling technology while leakage power increases. In nano-meter technologies, the sub-threshold leakage is the dominant leakage among many leakage components in cache as well as other SRAM-based memories but the leakage of gate can also increase at very thin gate oxides [1]. The High Energy efficiency is one of the paramount design constraints in most of the ultra-low power applications include WSNs (Wireless Sensor Nodes), implantable biomedical devices and portable electronic devices [2]. In such application, the SRAM plays a vital role in consumption of energy because of its higher cell density for the improvement of computational power. With the supply voltage, the structure of SRAM can also influence the consumption of energy. The SRAM cells might occupy most of the area of SoCs (System-on-Chip) and they have significant impact over consumption of power and performance of SoCs [3].

Reduction of transistor dimensions has resulted more integrity and higher performance. But the scaling technology has certain side effects including DIBL (Drain-Induced Barrier Lowering) that can lead to Vth (Threshold voltage) roll-of and thereby leakage current increases significantly and makes the dissipation of static power as one of the most vital concerns in modern VLSI designs [4]. Generally more than half of the total consumption of power of state-of-art VLSI chip might belong to the static power that is ignorable in earlier days in microelectronics [5]. In addition, variation of intensified procedure is another vital consequence of scaling technology. The tiny cells of SRAM will be highly vulnerable to process variations compared to other circuits because their appropriate operations rely on strength ratios of transistor [6].

The design plan of SRAM cell is characterized with three different vital metrics namely utilized strategy, number of transistors and plan innovation [7]. Every plan is compromised with specific plan for reducing the region, delay parameters and control and more over these may shift the number of transistors, certain times, the count of transistor can't differ and modifications might be made in classical SRAM cells. The new design may also require advanced new technologies when available, currently, most of the VLSI projects are conducted using the tools such as Tanner and Cadence with 45nm technology. In this paper an SRAM array is implemented based on the row column selection method using by applying back bias voltage.

II. LITERATURE SURVEY

M. H. Chang, et al [8] designed a 9T bit cell for enhancing the read ability while cutting of the positive feedback loop of SRAM cross-coupled inverter pair. During the operation of read mode, the access buffer has designed to isolate the storage nodes from the path of read for greater leakage reduction as well as read robustness. A bit-interleaving method might be allowed with presented 9T SRAM bit cell incorporation along with extra Write Word Lines (WWL) for the tolerance of soft-error.

C. H. Lo et al [9] developed an SRAM during its renovation stages and is aiming to withstand in ever-increasing process variation and supporting the ultra low power applications while utilizing the sub-threshold supply voltages. P-N-based 10T SRAM cell, where latch is formed especially by the cross-coupled P-N inverter pair. This kind of cell operates at the low voltages as 285 m V and still it demonstrates the higher resilience for process variation. However the nose margin is elevated in the hold state as well as during read operations. In [10], Carlson, A et al. presented a 6T cell using IGA (Independent Gate Access) transistors and tri-gate cross-coupled inverters. In this SRAM cell, each access transistor back gate would be connected with its adjacent bit-cell storage nodes. In this work the RSNM (Read Static Noise Margin) is increased compared to 6T SRAM using TG (Tri-Gate) devices. Though, in this approach, the read current decreases and this results larger delay in read operation.

Fatih Hamzaoglul et.al [11] designed an 153Mb (Mega Byte) SRAM design which is optimized for 45 nm higher metal gate technology. This design is completely integrated with dynamic forward body bias for achieving low voltage operations by maintaining the less power overhead and area. The dynamic sleep design is utilized with a op-amp (Operational Amplifier) based feedback control and over die programmable reference voltage generator might reduce the process variation effects as well as reduction of power. This design operates on 4.5 GHz (Giga Hertz's) at 1.1v and under forward body bias the stronger PMOS (P-channel Metal Oxide Semiconductor) improved the operating voltage by 75 mV with no increase in leakage power.

Naveen Verma et.al [12] presented an 8T bit-cell with buffered read that should eliminate the limitation of read SNM (System Noise Margin). The peripheral footer circuitry is added to this design that might eliminate the leakages of bit line. The author designed the storage cell drivers and peripheral write drivers for the reduction cell supply voltage in write operations. Given, sense-amplifier redundancy generates a favourable trade-off between area and offset. The SRAM array is build using 65nm technology might be determined as functional at 359mV and at 300 mV the data is retained correctly.

Jaydeep P. Kulkarni et.al [13] presented a Schmitt Trigger SRAM cell which has incorporated with a built in feedback method, achieved 56% of enhancement in SNM, enhancements in process variance tolerance, less probability in terms of read failure, lower voltage/lower power

operations and enhanced data retention capabilities at ultra low voltages than traditional 6T SRAM cell.

Ozdemir et. al [14] presented a design for turn-off the delay-violation as well as leaky cache lines or ways. This design is presented for allowing various segments of cache must be accessed at various latencies. However these methods improved the yield of chip, they can also affect the capacity of cache and/or speed whereas this approach keeps the actual yields without the impacts of capacity and negligible speed overhead. The leakage is reduced by selecting the higher Vth and high T_{ox} (oxide Threshold) and does not by turning of the leaky ones. So the speed of cell array and memory capacity remained intact. Meng and Joseph et al. [15] only considered the leakage variation within die and extended cache ways, while initiating from leakiest cache way if disabled ways are not utilized through the application. Since this model reduced the capacity of cache and leakage reduction is not done by disabling the cache parts.

III. ROW-COLUMN BASED SRAM ARRAY WITH BACK GATE BIASING

The Fig. 1 shows the architecture of 4X4 row column based 6T SRAM array design. The 4x4 array of SRAM system would be implemented by 16 back biased 6T SRAM cells. These 16 cells are divided as 4-columns where each column contains 4 bits. Sixteen 6T-SRAM cells with address decoder (row and column decoder), sense amplifiers and data write circuitry are employed for catering the 4 X 4 SRAM array. Address decoder is used to generate the row address and column address.

3.1 Address decoder

The address decoders might drive the signals which may go across memory core. It will drive the WL (Word line) that traverses via all the cells of memory in every row of a memory system. These are the set of cells that generate the word line signals from the word decoders. This structure takes a set of n address lines and generates word lines. At most, one of the word lines is active at a time. It can activate the WL (0-4) signal which will be essential to choose one of the row. The output word lines would be connected with every cell in each row. Column address select particular bit lines for being connected to sense amplifiers. This is accomplished either by sensing every bit line and getting a few of them out or by using pass gates to enable them to a few sense amplifier inputs.

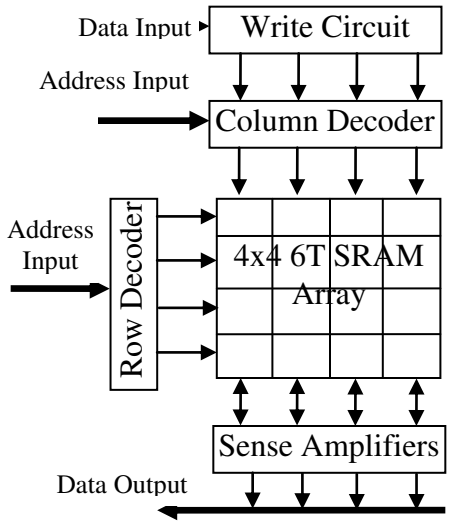


Fig. 1: Architecture of 4X4 row column selection based 6TSRAM array

3.2 Write circuit

The write driver circuit will be utilized in every column of memory array system. This will be activated by enabling the BLB (Bit Line Bar) and BL signals. If BL is enabled then the data will be written and its complement is written into Q and QB internal nodes via SRAM cell access transistors.

3.3 Sense Amplifier

The sense amplifier considers the huge capacity of memory as a rule for expanding the parasitic capacitance of bit line. Basically the sense enhancers are used for know about the Smash substance, Measure as well as SRAM cells. These would be exceptionally delicate to the clamor, their plans suggested that they may provide satisfactory commotion edges and offers greater information quality which speaks to particular memory cell substance. Two different types of sense intensifiers are namely inactive and energetic sense intensifiers. Usually the inactive sense intensifiers are used for distinguishing the rationale within inactive SRAMs and RAMs (Random Access Memory) whereas energetic intensifiers are used for sparing the vitality if moo control dissemination will be needed.

The Quick sense intensifiers will be vital in order to achieve low latency in various circuits, the common foremost space being BL perused in memories. Due to the sub micrometer CMOS (Complementary Metal Oxide Semiconductor) chips approach, the interconnection become a main on-chip delay source and the quick sense enhancers are possibly needed e.g., as a repeater to higher speed signals that should navigate the huge-chip. The analog differential sense amplifier employed in the circuit which is utilized as read circuit to read the data in SRAM system. The read operation performed through Q. In SRAM system each column contains one read circuit.

3.4 6T SRAM Cell

Here the SRAM ultra-fast data sanitization in 5 ns is illustrated using the forward back biasing against the attack namely cold boot. The back-bias applied to the body of MOSFET (Metal-Oxide Semiconductor Filed-Effect Transistor) will be used for deleting the stored data through latch state intentional distortion between the two inverters of SRAM cell that can also enclose the two n-channel pass-gate MOSFETs. These inverters might be cross-coupled for sustaining the state of latch stably until the power is supplied. The inverter would be composed with CMOS (Complementary Metal-Oxide-Semiconductor) i.e., a PMOS (a pull up p-channel MOSFET) and a NMOS (abbreviated as a pull-down n-channel MOSFET). There are two data erasing types in demonstrated data sanitization. First one is temporary erasing by back-bias to 2 p-channel MOSFETs symmetric application in every inverter.

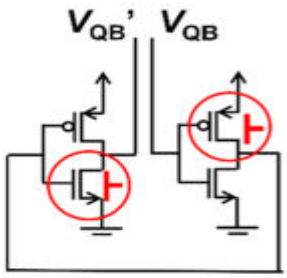


Fig. 2: Modified configuration of a 6 T-SRAM cell

The second one is permanent erasing by the asymmetric application of back-bias to the NMOS in one inverter and a NMOS in another inverter. In normal cases, the recovery of data would be allowed after the attempt of lower-level threat through hacking. In latter cases, the recovery of data will be impossible after the higher-level threat attempt through hacking. However the temporary erasing might partially disturbs the reading of data through a symmetric application of forward back-bias in an attack and after that the data which is distorted partially will be recoverable after hacking attempt cessation. Whereas the permanent erasing deletes the redundant data completely through the asymmetric application of forward back-bias against the attempt of severe hacking; thereby the erased data will be irrecoverable.

Hence the user reuses the earlier data with temporal erasing while the user can't do them in permanent erasing if the attack is completed. This model with the help of back-biasing won't demand any extra circuitry since back-biasing is generally utilized to tune the characteristics of CMOS like Vth, leakage current. The demonstrated data sanitization is analyzed for temporary erasing and permanent erasing with the simulation of physics based devices. The results will indicate that this presented back-bias approach will offer great immunity against the cold boot attack at lower temperatures.

IV. RESULT ANALYSIS

The schematic of presented SRAM array is simulated using Tanner EDA (Electronic Design Automation). Here the read operation is controlled by RWL (Read Word Line) and write signal is controlled by WWL. The result analysis of presented SRAM array is compared with the 8T SRAM array. Fig. 2 and Fig. 3 shows circuit schematic and presented 6T SRAM cell and array that is constructed using 6T SRAM cell respectively. Here, the 4X4 row Column-based 6T SRAM cell is designed. Fig. 5 shows the Spice report which indicates the net list of components that are used for implementing the design. Then the Fig. 6 and Fig. 7 shows the output waveform respectively.

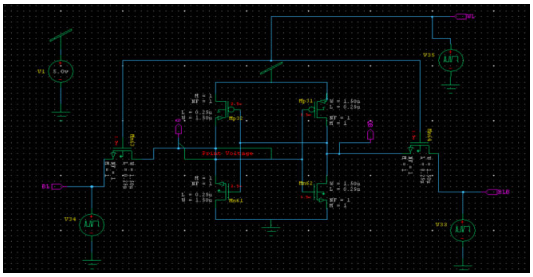


Fig. 3: Schematic of SRAM cell

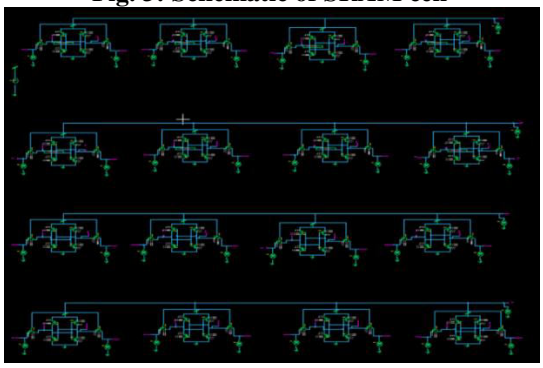


Fig. 4: Schematic of row column based SRAM Array

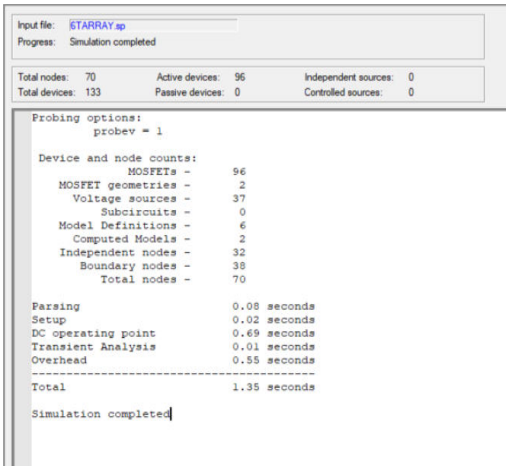


Fig. 5: Spice report of row column based row column based SRAM array

The Fig. 6 and Fig. 7 show the output waveform of row column based SRAM array. Fig. 5 shows output waveform when WL0=1, WL1=1 for BL1=1, BL2=0,BL3=1, BL4=0, BL5=0, BL6=1, BL7=0, BL8=1.

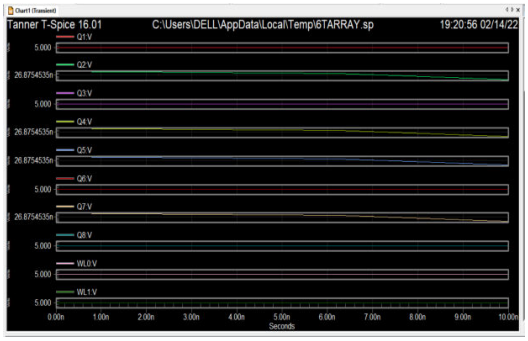


Fig. 6: Spice report of row column based SRAM array

Fig. 5 shows output waveform when WL0=1, WL1=0 for BL1=1, BL2=0,BL3=1, BL4=0, BL5=0, BL6=1, BL7=0, BL8=1.

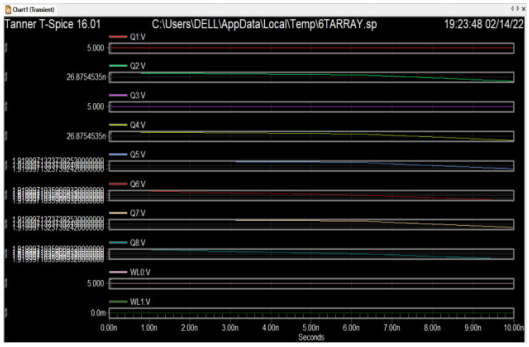


Fig. 7: Spice report of row column based SRAM array

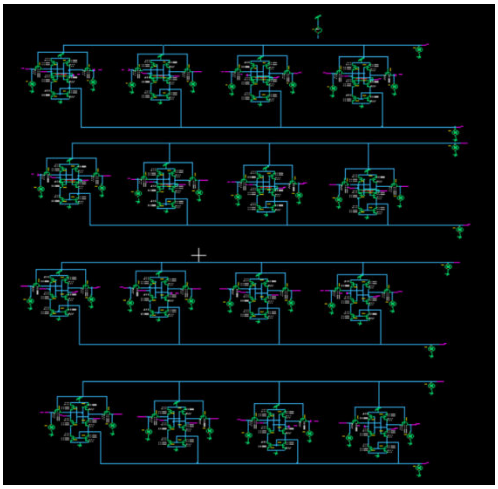
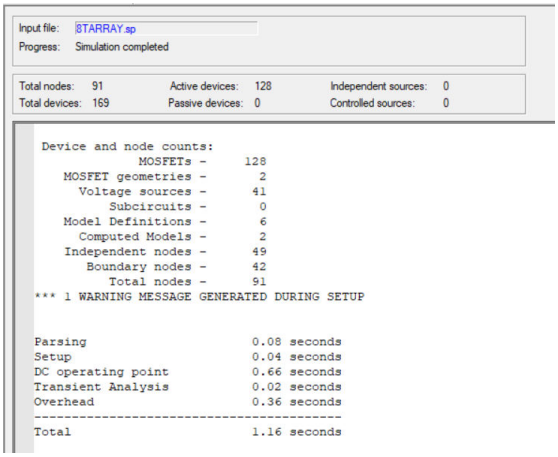


Fig. 8: circuit schematic of 8T SRAM array

Fig. 8 and Fig. 9 shows circuit schematic and spice report of conventional SRAM array respectively.



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Input file:   8TARRAY.sp
Progress:     Simulation completed

Total nodes:    91      Active devices:    128     Independent sources:   0
Total devices:  169     Passive devices:   0       Controlled sources:    0

Device and node counts:
              MOSFETs -      128
   MOSFET geometries -        2
     Voltage sources -       41
          Subcircuits -        0
   Model Definitions -        6
     Computed Models -        2
   Independent nodes -       49
      Boundary nodes -       42
         Total nodes -       91
*** 1 WARNING MESSAGE GENERATED DURING SETUP


Parsing                     0.08 seconds
Setup                       0.04 seconds
DC operating point          0.66 seconds
Transient Analysis          0.02 seconds
Overhead                    0.36 seconds
-----------------------------------------
Total                       1.16 seconds
```

Fig. 9: Spice report of 8T SRAM array

The Fig. 10 shows the comparison of SRAM arrays. It can be seen that the number of MOSFETs used to implement the row column selection based SRAM array is less than that of conventional 8T SRAM array. It also depicts the comparison of Boundary Nodes, Total Nodes and number of Independent Nodes in circuit design of SRAM arrays.

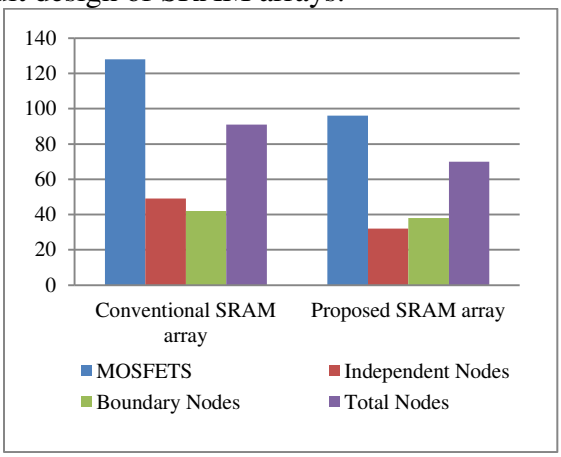

Fig. 10: RESULT ANALYSIS

V. CONCLUSION

Design of row and column selection based SRAM array using back bias technique was implemented in this paper. SRAM memory array plays important role in entire system. This paper implemented a 4×4 SRAM memory with each 6T SRAM cell. The simulations are performed on Xilinx Tanner EDA tools using CMOS process technology that provide schematic, spice report and waveforms of the design. From the obtained simulation result it is noticed that this design utilizes less number of transistors and nodes compared to existing 8T SRAM array. The read and write stability is also improved in the 6T SRAM array compared to the conventional 8T SRAM array. The 6T SRAM has better performance in terms of reduction of power dissipation and leakage currents compared to traditional 8T SRAM.

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