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Research Article

Low Power Logic Gate cell design and its performance analysis

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Abstract- This paper describes the design of a 45nm CMOS technology logic gate library cells for highly energy-efficient applications of embedded processors. Design of OR and AND, circuits is present in this paper, to improve the speed and power. The comparative analysis of different performance parameters for CMOS logic gates is presented. Average power, Static Power and Delay are the parameters evaluated using Cadence tool. For a full-chip implementation of low-power systems operating at ultra-low voltage is feasible. The power and delay is extracted for logic cells at supply voltages 0.8 V, 1.0 V & 1.2 V at different frequencies.

Keywords:- CMOS Technology, Power-Delay Product, Average Power.

1.INTRODUCTION

In IC design technology where numbers of logic gates are integrated, constant and continuous works is being carried out by different experts to reduce the power dissipation. It is still a big challenge for researchers to design a reliable circuit with very low power dissipation [1]. There are different approaches to minimize the power dissipation base on architecture, circuit level, layout, and process technology. Among all these techniques, at the circuit design level considerable amount of power savings [2] can be achieve by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents [3] are strongly influenced by the chosen logic circuit. Another approach to reduce power dissipation [4] is by using stack technique where each of the NMOS and PMOS in the logic gate is split into two transistors. Sub threshold [5] circuit design operation technique also reduces power dissipation in CMOS where circuits should be operated in near-threshold region [6]. Another effective way is by reducing the supply voltage as CMOS total power dissipation depends upon two power i.e. dynamic power and static power [7]. As these both power depends upon VDD if supply voltage [8] is reduced the total power can be minimize.

2. GENERAL REVIEW OF TOTAL POWER CONSUMPTION IN CMOS.

The basic equation governing the total power in CMOS circuit is given by

$$P_{Total} = P_{Dynamic} + P_{Static}$$

$$P_{Total} = ½\, CLV_{DD}\, 2af + I_{Sc}V_{DD} + I_{Static}V_{DD} \quad (1)$$

Where CL is the load capacitance, f is the frequency of operation, a is the activity factor, ISc is the short circuit current [9]. The equation (1) implies that both the dynamic and static power depends upon the supply voltage VDD [10] at large. The dynamic power consumption is mainly due to the charging and dis-charging of the capacitance and short circuit current. A short circuit current flows when the pull up and pull down networks in a CMOS circuit are simultaneously on and a direct path exists between the supply line and ground. Dynamic power [11] is directly proportional to the square of the supply voltage. Therefore, dynamic power reduces in a quadratic manner when the supply voltage is reduced. Leakage power is dependent on the leakage current [12] flowing in the CMOS circuit. If the supply voltage VDD is reduced the total power dissipation in the CMOS circuit [13] can be decrease tremendously. This work is carried out at supply voltage of 0.8V, 1.0V 1.2V with 45nm CMOS technology by scaling the size [14] of MOS transistor to its minimum optimum level so that the basic gate operation is not affected.

3. CIRCUIT IMPLEMENTATION

The Design of logic gates includes AND gate and OR gate. Schematic & Layouts are developed for logic gates and Simulation is carried out with a supply voltage of 0.8V, 1.0V & 1.2V at different frequencies (100MHz, 200MHz, 250MHz, 400MHz 500MHz).Average power and delay [15] is measured at different supply voltages and frequencies. A stream of bits is used as input bits. Each of the bits with magnitude 0.8V,1.0V &1.2V corresponds to logic 1 and the ground state corresponds to logic 0. AND & OR Gates are simulated two input terminal A and B with output terminal Q.

3.1 AND GATE

AND gate is inverter operation of the universal gate NAND performs bitwise operation on two or more number of inputs. When the inputs all are high (logic '1') then the output is high (logic '1'). In the remaining cases, the output is low

(logic ‘0’). The truth table for two input AND gate is given below. In the same way the 32-bit AND gate performs operations on individual bits of two inputs A and B.

Fig: 1 Schematic circuit of AND gate

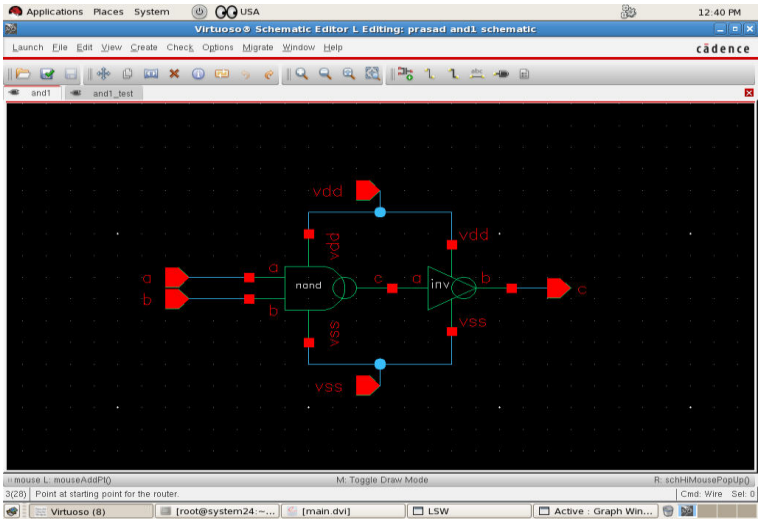

Fig: 2 Layout circuit of AND gate

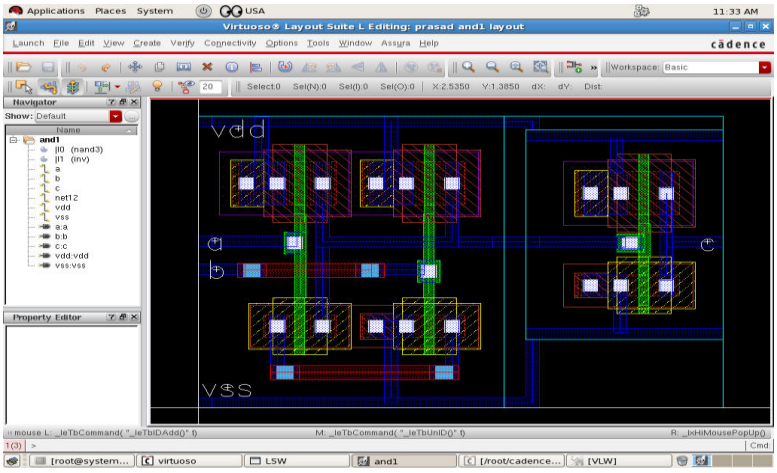

Fig :1 shows schematic circuit & Fig:2 shows layout diagrams of AND Gate

Power, Delay and PDP Results and Analysis of AND gate:-

Table 1: Schematic power consumption of AND gate

Schematic Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	40.54	80.54	100.5	160.1	199.7
1.0	64.28	127.9	159.6	254.3	317.3
1.2	92.56	184.3	230.0	366.9	457.9

Table 2: Layout power consumption of AND gate

Layout Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	73.76	146.7	183.0	291.6	363.8
1.0	116.4	231.6	288.8	460.9	575.2
1.2	167.1	332.7	415.4	662.8	827.4

Table 3: Static power consumption of AND gate

Static Power(pW)		
Supply voltage(V)	Schematic Power	Layout Power
0.8	12.4417	12.4425
1.0	21.9231	21.9244
1.2	36.8899	36.8919

Table 1 shows average power of schematic circuit at different supply voltage and different operating frequencies. Table 2 shows average power of layout at different supply voltage and different operating frequencies. Table 3 shows static power of Inverter at different supply voltages of AND gate.

Table 4: Delay comparison of AND gate

	SchematicDelay (pS)		Layout Delay (pS)	
Supply Voltage(V)	Minimum	Maximum	Minimum	Maximum
0.8	23.6	74.6	37.39	135.0
1.0	13.2	33.3	20.25	58.9
1.2	9.73	21.8	14.67	37.9

Table 5: Schematic PDP of AND gate

Schematic Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	3.024	6.008	7.497	11.943	14.897
1.0	2.141	4.259	5.315	8.468	10.566
1.2	2.018	4.018	5.014	7.998	9.982

Table 6: Layout PDP of AND gate

Layout Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	9.958	19.805	24.705	39.366	49.113
1.0	6.856	13.641	17.010	27.147	33.879
1.2	6.333	12.609	15.744	25.120	31.358

Table 4 shows delay for Schematic & Layout design, Table 5 shows Power-Delay product of Schematic design and Table 6 shows Power-Delay product of Layout design of AND Gate.

Fig: 3 Power comparison of AND gate at 0.8 V, 1 V & 1.2 V supply voltage

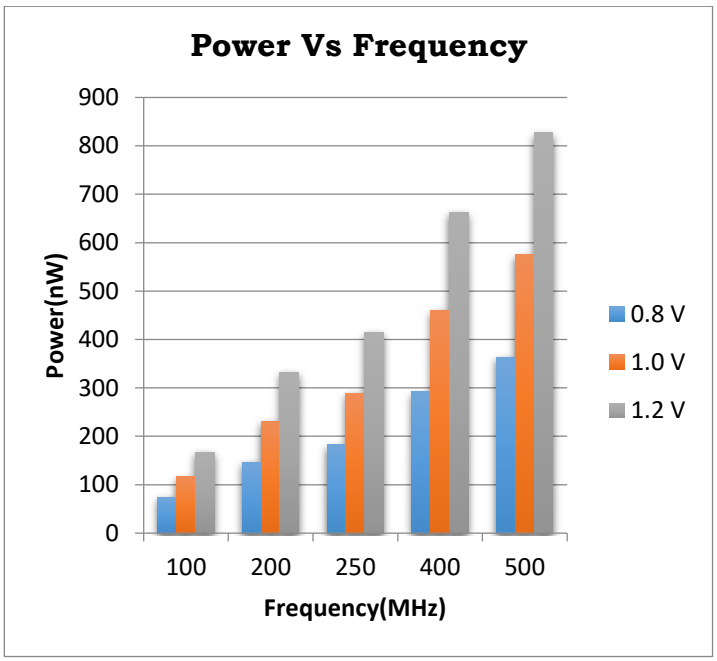

Fig: 4 PDP comparison of AND gate at 0.8 V, 1 V & 1.2 V supply voltage

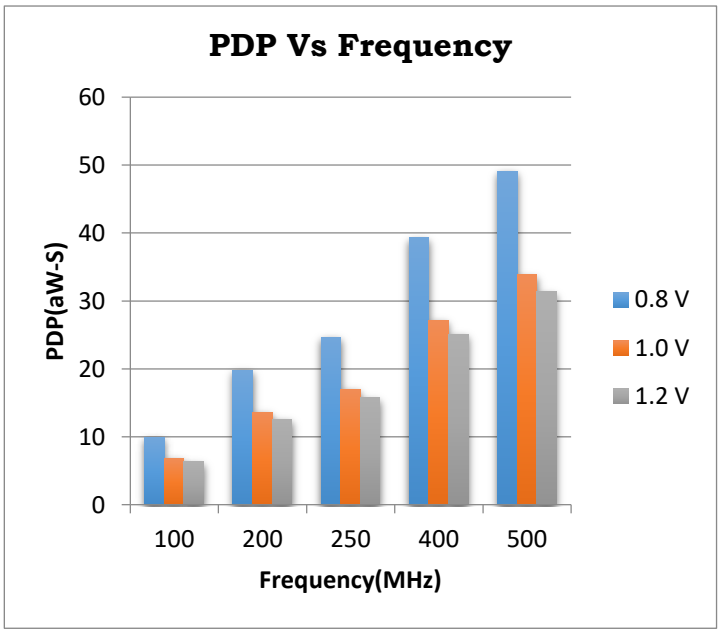

Fig 3 shows comparison of Layout power at different frequencies and supply voltages and Fig 4 shows comparison PDP at different frequencies and supply voltages of AND Gate.

3.2 OR GATE

OR gate is an inverter function of the universal gate NOR performs bitwise operation on two or more number of inputs. When all the inputs are low (logic ’0’) then the output is low (logic ‘0’). In the remaining cases, the output is high (logic ‘1’). The truth table for two input OR gate is given below. In the same way the 32-bit.

Fig: 5 Schematic circuit of OR gate

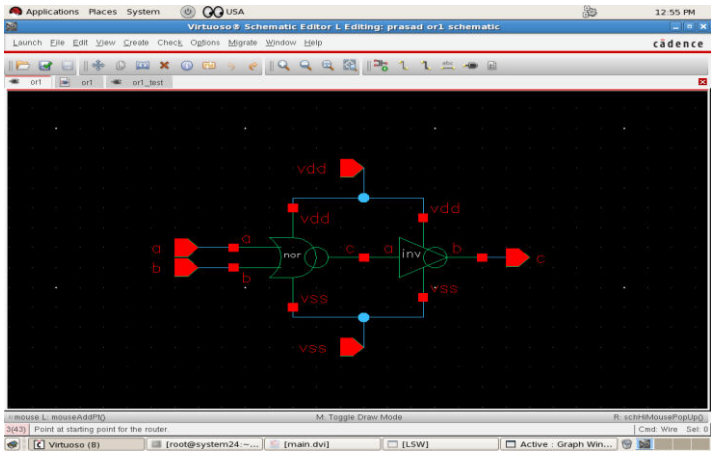

Fig: 6 Layout circuit of OR gate

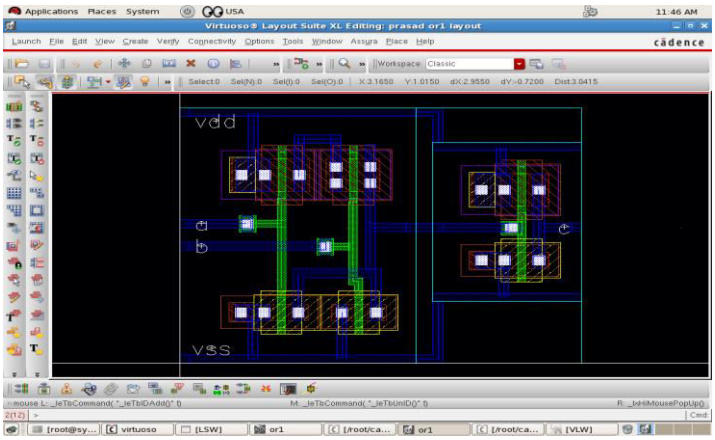

Fig :5 shows schematic circuit & Fig:6 shows layout diagrams of OR Gate.

Power, Delay and PDP Results and Analysis of OR gate:-

Table 7: Schematic power consumption of OR gate

Schematic Average Power(nW)					
Supply voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	42.71	85.41	106.6	170.1	212.2
1.0	71.95	144.2	180.2	287.8	359.3
1.2	111.5	223.8	279.7	447.2	558.5

Table 8: Layout power consumption of OR gate

Layout Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	67.86	135.5	169.2	269.9	336.8
1.0	111.0	222.1	277.5	443.2	553.4
1.2	166.2	333.0	416.3	665.4	831.2

Table 9: Static power consumption of OR gate

Static Power(pW)		
Supply Voltage(V)	Schematic Power	Layout Power
0.8	8.97101	8.97093
1.0	16.7556	16.7555
1.2	29.7096	29.7094

Table 7 shows average power of schematic circuit at different supply voltage and different operating frequencies. Table 8 shows average power of layout at different supply voltage and different operating frequencies. Table 9 shows static power at different supply voltages of OR Gate.

Table 10: Delay comparison of OR gate

	Schematic Delay(pS)		Layout Delay(pS)	
Supply Voltage(V)	Minimum	Maximum	Minimum	Maximum
0.8	34.94	61.6	59.36	99.4
1.0	17.87	31.0	29.2	48.6
1.2	12.71	21.3	20.25	32.9

Table 11: Schematic PDP of OR gate

Schematic Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	2.631	5.261	6.567	10.478	13.072
1.0	2.230	4.470	5.586	8.922	11.138
1.2	2.375	4.767	5.958	9.525	11.896

Table 12: Layout PDP of OR gate

Layout Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	6.745	13.469	16.818	26.828	33.478
1.0	5.395	10.794	13.487	21.540	26.895
1.2	5.468	10.956	13.696	21.892	27.346

Table 10 shows delay for Schematic & Layout design, Table 11 shows Power-Delay product of Schematic design and Table 12 shows Power-Delay product of Layout design of OR gate.

Fig: 7 Power comparison of OR gate at 0.8 V, 1 V &1.2 V supply voltages

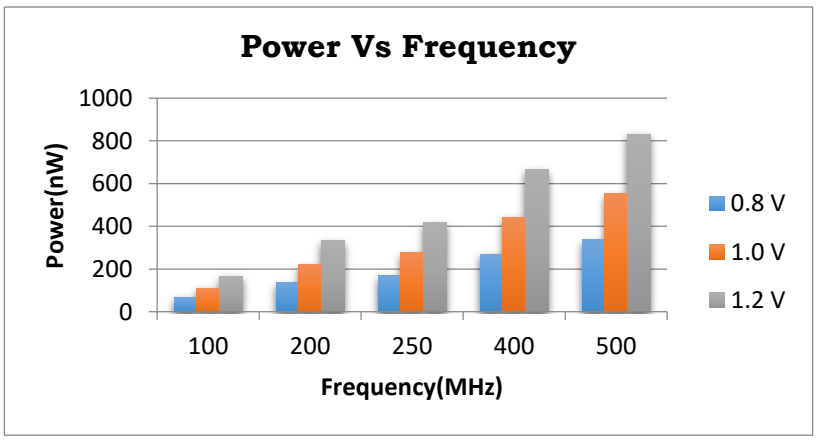

Fig: 8 PDP comparison of OR gate at 0.8 V, 1 V &1.2 V supply voltage

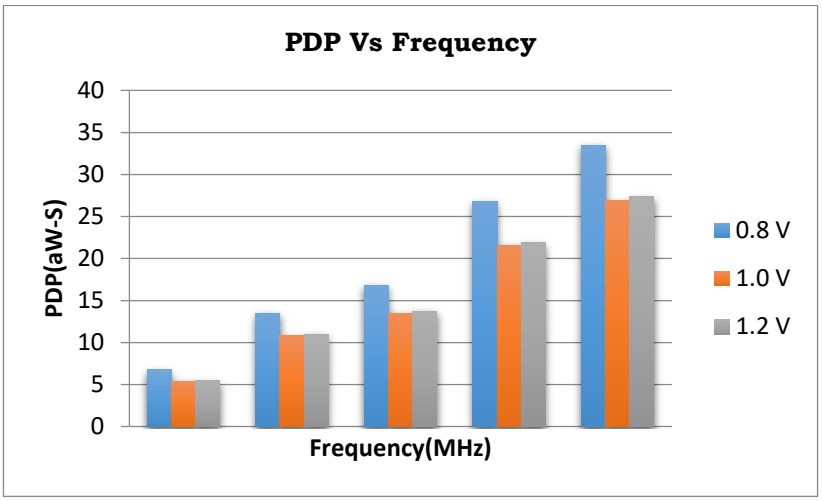

Fig 7 shows comparison of Layout power at different frequencies and supply voltages and Fig 8 shows comparison PDP at different frequencies and supply voltages of Inverter.

4. CONCLUSION

In order to perform basic arithmetic operations AND & OR gates are designed using 45nm CMOS Technology which consumes very less power. The delay comparison is also done & Power Delay Product (PDP) is calculated. Experimental results show that the average power of AND gate is reduced by 43% when supply voltage is changing from 1.2V to 1.0V at 500 MHz. Average power is reduced to 58% when supply voltage changing from 1.0V to 0.8 V at 500 MHz. The average power of OR gate is reduced by 50% when supply voltage is changing from 1.2V to 1.0V at 500 MHz. Average power is reduced to 64% when supply voltage changing from 1.0V to 0.8 V at 500 MHz. By reducing supply voltage, power reduction is achieved effectively for logic gate design.

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