DESIGN AND EVALUATION OF AREA-EFFICIENT PIPELINED TURBO ENCODER AND DECODER

[1]NAGARAJU PAIDIMALLA, [2]TUMMAPALA LALITHA PRASANNA
[1]Assistant Professor, Dept of ECE, Srinivasa Institute of Engineering and Technology, Cheyyeru Village, Amalapuram, East Godavari, Andhra Pradesh, India
[2]M.Tech Scholar, Dept of ECE, Srinivasa Institute of Engineering and Technology, Cheyyeru Village, Amalapuram, East Godavari, Andhra Pradesh, India

ABSTRACT: In this project design and evaluation of area efficient pipelined turbo encoder and decoder is implemented. Turbo coding is very effective technique for correcting errors. These codes widely used in communication systems. Wireless communications (3G & 4G) includes turbo codes within it for accurate error correction. Earlier, the polar codes are implemented using 8 bits, so polar decoder is restricted by the inherent iterative process to compile the data at a higher rate. High decoding accuracy is the major flaw of polar coding implementation. Hence in this work, implementing 64-bit turbo encoder and decoder to compile the data at higher rate with reduced area and delay. The system is implemented and correlated in Application Specific Integrated Circuit (ASIC). At last compared with existed system, proposed system gives effective outcome in terms of delay and area.
KEY WORDS: Application Specific Integrated Circuit (ASIC), Polar Decoder, Turbo Encoder and Decoder, CRC (Cyclic Redundancy Check), FIFO (First In First Out), S-Box (Substitution Box).

I.INTRODUCTION

In digital communication, the transmission of the data is processed by converting the decimal or octal decimal to the binary or binary coded decimal (BCD) [1]. After being processed the data, at the receiver side again this BCD can be converting into the familiar numbers or symbols. This process of encrypted the data is called as Encoding, this process can be done by the device or element is known as Encoder. And conversely the decryption of data can be done by the device Decoder, and this process is called Decoding. Here the decoder works opposite to the encoder.

One format of code or information is transmitted into another format by using an encoder, It may be a device, a circuit, software program, an algorithm or a person. The main objective of encoder is uniformity, high speed, privacy, security and compression of memory size. Encoders are contradictory to decoders and they are called as combinational logic circuits. Encoder generates a multi bit output code by taking one or more inputs.

As encoder is contradictory to decoder they perform reverse operations to that of decoder. Encoder consists of M number of input line and N number of output lines [2], only a single line is active at once out of these M number of input lines and produces a code that is equivalent to N lines of output. In case of more number of bits in input code than that of output code in a device then the device is considered as an encoder device.

Digital Encoder is frequently called as Binary Encoder, All the data inputs are accepted at once and it transforms the data into a single output that is encoded. Unlike this digital encoder, multiplexer accepts single input data line and it transforms data into a single switch or data output line. By this it is concluded that binary encoder is a combinational logic circuit with multi-inputs. It transforms the input of logic level "1" data into an identical binary code as an output.

Basically, A 2-bit, 3-bit or 4-bit code outputs is generated by digital encoders that rely upon data input number lines. 2^n number of input lines and n-bit output lines including 4-to-2, 8-to-3 and 16-to-4 configuration lines are present in "n-bit" binary encoder [3].

Encoders are the digital IC's (Integrated Chips) which are used to perform the encoding operation. That means an encoder can convert the decimal form of the 2^N inputs into the binary N outputs [4]. So the encoder can encode the information from the 2^Ninputs to N outputs. In order to do the operation by using the encoder there is a need to give active high input to the encoder enable. If only one input line is active in the encoder then it is assumed as simple encoder.

In all digital communication systems encoders are very essential element. Binary functions are performed on the binary data only [5]. So the decimal values are can be converted into the binary data by using the Encoders. Interrupts in the microprocessor is detected by using the priority encoder.

A decoder can perform tasks like accepting multiple-inputs, producing multiple-output logic circuit which transforms coded inputs into coded outputs, where the input and output codes vary from each other e.g. n-to-2n, binary-coded decimal decoders. Decoding is essential in applications like data multiplexing, 7 segment display and memory address decoding. An AND gate is an example of decoder circuit and only when all its inputs are "High", the output of an AND gate is "High". Such output is called as "active High output". The output will be "Low" (0) in case of connection with NAND gate instead of AND gate only when all its inputs are "High". Then the resultant output is known as "active low output" [6].

The n-to-2n type binary decoder is little bit complex type of decoder. Such types of decoders are combinational circuits that transform binary data from 'n' coded inputs to an extent of 2n unique outputs [7]. The decoder may consist of less than 2n outputs when 'n' bit coded information has unused bit combinations. 2-to-4 decoder, 3-to-8 decoder or 4-to-16 decoder are some other examples.

A parallel binary number is given as input to decoder which can identify the presence of particular binary number input and the output represents weather the specific number is present at the decoder input or not.

The Decoder is a combinational logic circuit. it converts a binary code into desired output signals. It performs the reverse process of encoder hence it is called decoder. The process of converting binary input code into desirable output is known as decoding [8].

Based on the combination of the current inputs, when the decoder is enabled, one of the outputs is active high state. It means that a certain code can be detected by the decoder. The decoder output is minterms of n input variable lines, when it is enabled.

The decoder is a logical circuit which is based on combination and it accept the set of inputs can be represented as binary number and only the output can be activated and it is corresponding to the binary input number [9]. The inputs of decoder determines the which binary number is

present and only one output is activated that similar to the number and remaining outputs are inactivated.

The basic decoder function is used to detect the presence of the combination of input bits and also indicates the presence of code by a specific output level. Generally, decoder have n input lines for handling the n bits, also it indicates the presence of one or more n bit combinations, it takes the one out of 2n output lines [10].

II. EXISTED SYSTEM

The below figure (1) shows the block architecture of existed system. There are three main components used in this existed system, they are feedback encoder, commutator and PE (Processing Element). To perform the operation in parallel format N-Bit decoder uses delay elements like registers and log2 N PEs elements. Therefore in our design folding factor is take as N/2. After the last stage of PE, two multiplexers (MUXs) are used in each h node.

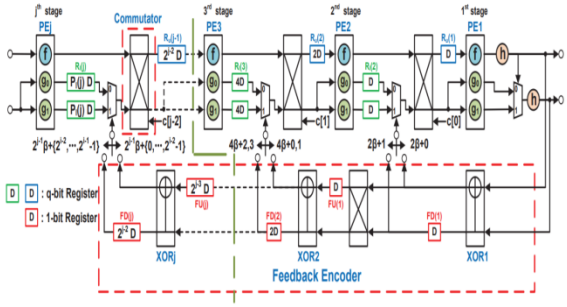

Fig. 1: BLOCK ARCHITECTURE OF EXISTED SYSTEM

To store the intermediate signals delay elements are utilized. These delay elements are based on the properties of pipelining and folding. The green dashed line shows the delay elements from figure (1). In each stage there are three registers. Ru(j) is the register set which is in the upper path, Rl(j) consists of two identical register sets which consists of lower paths for each g node.

There are two MUXs in commutator. These MUXs are combined with a single bit control signal c[j]. This will perform the switch operation in each stage j. By using (n − 1)-bit counter, switching rate is controlled in commutator. Forward path in commutator is represented as μ. By using (n − 2) bit counter, feedback path is controlled in commutator. Feedback path in commutator is represented as μf b.

For each subsequent stage, switching rate of the commutators is doubled. The PEs interval is reduced to half between two inputs. To build the polar encoder, feedback encoder is utilized and this will calculate the partial sum in polar encoder. Feedback encoder is simplified to (n−1) stages. At last in each stage MUX based on uˆsum is utilized to get exact output.

IV. PROPOSED SYSTEM

The below figure (2) shows block diagram of proposed system. Initially inputs and keys are given and assigned in particular format. Cyclic Redundancy check (CRC) will check whether the bits consist of errors or not. If there are errors it will check and correct those errors. After that bits are substituted using S-Box. Inter leaver operation is performed for substituted bits and those bits are encoded using turbo encoder. Hence the inverse operation of this encoder is decoder.

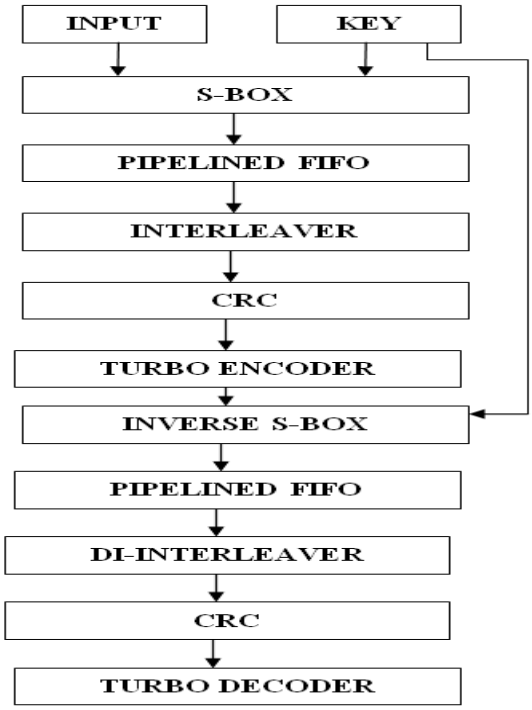

Fig. 2: BLOCK DIAGRAM OF PROPOSED SYSTEM

S-box (substitution-box) is a basic component of symmetric key algorithms which performs substitution. In block ciphers, they are typically used to obscure the relationship between the key and the cipher text, thus ensuring Shannon's property of confusion. The inverse S-box is simply the S-box run in reverse. For example, the inverse S-box of 0xdb is 0x9f. It is calculated by first calculating the inverse affine transformation of the input value, followed by the multiplicative inverse.

An interleaver permutes symbols according to a mapping. A corresponding deinterleaver uses the inverse mapping to restore the original sequence of symbols. Interleaving and deinterleaving can be useful for reducing errors caused by burst errors in a communication system.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. ... On retrieval, the calculation is repeated and, in the event the check values do not match, corrective action can be taken against data corruption.

The Turbo Encoder block encodes a binary input signal using a parallel concatenated coding scheme. This coding scheme employs two identical convolutional encoders and one internal interleaver. Each constituent encoder is independently terminated by tail bits.

To decode the coded input signal, turbo decoder utilized the parallel concatenation. While performing turbo decoder, inverse S.BOX, De-Interleaver operations are performed.

V. RESULTS

RTL schematic of proposed system is shown in below figure (3). RTL schematic is the combination of both inputs and outputs.

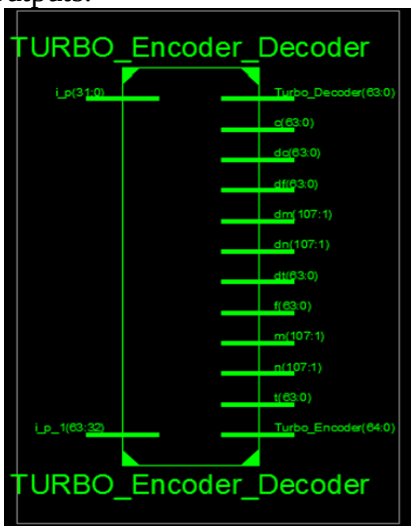

Fig. 3: RTL SCHEMATIC OF PROPOSED SYSTEM

Technology schematic of proposed system is shown in below figure (4). Technology schematic is the combination of LUT's, Truth tables, K-Map, Equations and Buffers.

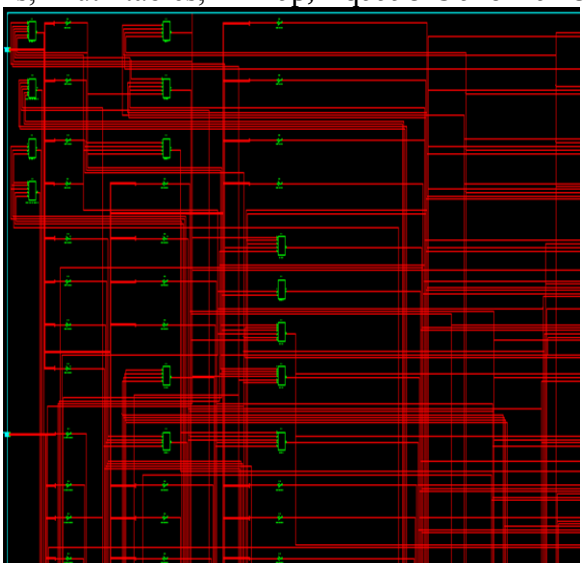

Fig. 4: TECHNOLOGY SCHEMATIC OF PROPOSED SYSTEM

The below figure (5) shows the output waveform of pipelined turbo encoder and decoder. The output is obtained as "00100101010010101010001010100100001010100100101001010 00010100101".

Fig. 5: OUTPUT WAVEFORM

Table. 1: COMPARISON TABLE

S.NO	Parameters	Existed System	Proposed System
1	LUT's	614	556
2	Total Delay	16.4 ns	14.9 ns
3	Memory Used	341 Mb	257 Mb

The above table (1) shows the comparison table of existed and proposed system. In this number of LUT's, total delay and memory used are given in detail manner. Compared with existed system proposed system gives effective outcome in terms of LUT's, Total Delay and memory used.

VI. CONCLUSION

Hence in this paper design and evaluation of area efficient pipelined turbo encoder and decoder was implemented. A turbo decoder has been implemented which increases the throughput. Hence the proposed structure will produces best reliability and area when compared to existed system. In future we can extend this project to 128, 256, 512, 1024, etc the number of bits. This paper can be implement in backend tools like Tanner tools, Mentor Graphics by using GDI(Gate diffusion input) Technology and as well as in hardware technology also.

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