*Turkish Journal of Computer and Mathematics Education Vol.12 No. 12(2021), 4819-4825*
*Research Article*

# DESIGN AND IMPLEMENTATION OF A HIGH SPEED AND AREA EFFICIENT VLSI ARCHITECTURE OF BINARY ADDER

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**ABSTRACT: In this paper design and implementation of a high speed and area efficient VLSI architecture of binary adder is implemented. Basically, adders plays very important role in DSP (Digital Signal Processing) and micro processor applications. Input 'a' and input 'b' are assigned in particular order. Next pre-processing stage will be performed. In pre processing stages both propagator and generator signals are generated. Propagator and generator unit generate the signals of propagate and generate. Black cell and grey cells are generated in Carry generation unit. Addition is performed using adder tree block. At last output is saved in post processing stage. From results it can observe the RTL (Register Transfer Logic) schematic, Technology schematic of proposed system. Hence the binary adder gives effective results.**

**KEY WORDS: Binary adder, Pre Processing Stage, Adder tree, VLSI (Very Large Scale Integration), Post Processing stage, Black cells and Grey Cells.**

## I.INTRODUCTION

In Digital computers summation is mostly used in to perform operation in arithmetic. Also, it serves in structure building for combination of perform operations in arithmetic. It efficiently develops an arithmetic cell. Summation of binary framework and its cell perform operation very difficult in hardware [1]. Arithmetic operation in system looks that there adjust a more number of various device framework with various speed behavior and hugely used in the work.

Hence more developer's deals with the binary summation framework which are required. It depends on comparison speed research. Here have to known that approximate calculation classification of binary adder architectures. Between the more number of summation use VHDL (Hardware Description Language) code for Ripple-carry, Carry-select and Carry-look ahead to highlight usual speed attributes with to their classification

Based on variation expand time and area difficulty, the summation of binary can be divided into 4 main classification. The given below output in the table are the largest support word correct method, hard large section width value. 1st classification contains easy ripple-transfer summation with the shortest location. In the 2nd classification, the transfer-skip, transfer-select transform with different stages have short place specification and decreases calculation. In 3rd classification, the transfer-look forward summations from the 4th classification, the similar name summation constitute the speed added rules with the longest place difficulties

In digital electronics summation logical device develops sum in the integers [2]. To compute address by using summation in more systems, other types of CPU, also same operations, table indicates the arithmetic logical cell and also in other types of the CPU. It can be developing the framework of numerical same as pair cipher digit.

Compact data and low power are very important parts in sensor nodes and acts as a link between

data processing and sensors. And also in very high speed massive parallel sensors like imagers, every photodiode comprise of compact ADC (Analog to Digital Converter) for parallel conversion and moderate accuracy [3].

Conversion of that data faces challenges if CMOS (Complex Metal Oxide Semiconductor) implementations are used. Mainly there are two challenges. Most difficult and first challenge tedious thing is that integrating of ADC's with each and every channel or pixel since analog circuits have large area. This is highlighted by poor analog circuit scaling in CMOS (Complex Metal Oxide Semiconductor) because advanced technologies have various process variations. Second one is that ADC's higher static power. To balance the performance and area/power, most of image sensors with high speed uses image sensors in sensor arrays in column parallel ADC's. Though, image sensors having high frame rate are needed for emerging application images like time-of-flight, vision in integral machine, 3-D HD television imaging.

Fastest technologies are developed in present days. In present days, reduction of device size, fast operation and low power consumption are required. In mobile communication low power VLSI system plays very important role. Low power consumption is obtained because of high speed and small silicon area consumption. In the computations, FU (Floating point unit) and ALU (Arithmetic logic unit) are the main parts. Arithmetic logic unit (ALU) will process the addition, subtraction, multiplication, division operations along with that AND, OR, INV operations also [4].

In digital signal processors and microprocessors data path plays very important role. This will increase the speed of operation, reduce the area and power. All these parameters based on the data path efficiency. Subtraction, addition, division and multiplication are the complex operations available in data path. Data path performance performs the complex computations which are based on the hardware units.

The executed operation in data path is addition. To perform the addition operation binary adder is utilized [5]. The most important task is to reduce the complexity while performing the operations of decimal operations, multiplication and division. Efficient results are obtained by utilizing the adder.

## II. LITERATURE SURVEY

**Meenu Pareek, Manish Singhal, "Low power high speed area efficient Error Tolerant Adder using gate diffusion input method", 2016. [6]**

There is need of accurate outputs in digital VLSI circuits. Hence the researchers focus on the designing of error tolerance circuits which gives good output for computation. In this error tolerant adder (ETA) is designed to obtain high speed performance and good power. 32-bit ETA based on GDI is adopted in this paper depend on the emerging logic style. This will reduce the area and delay in very effective way.

**Rommel M Anacan, Josephine L. Bagay, "Logical Effort Analysis of various VLSI design algorithms", 2015. [7]**

Delay estimation is considered as one of the basic issues in the advancement of any Very Large

Scale Integration (VLSI) plan calculations. It is otherwise called one of the elements to dissect in the plan of superior execution coordinated circuit. Neither of these is normally applied to notice the exhibition of different VLSI geographies. Elite execution incorporated circuits regularly use adders to accomplish better speed to the detriment of force utilization, commotion edges or plan exertion.

**R. Suganya, D. Meganathan, "High performance VLSI adders", 2015. [8]**
The target of the work is to plan and analyze execution and energy effective VLSI adders for the different piece level up to 64-cycle utilizing progressed CMOS innovation. To think about the exhibition of the adders, late calculations of Weinberger, Ling and Manchester convey Manchester convey chain snake presents chain is chosen among the superior presentation adders. These three calculations are picked in light of the fact that their proficient designs make least reliance on bits over power, energy and postponement than other VLSI adders. It has been seen that even though more deferral than other VLSI adders because of its affixed design, it devours less power because of its decreased semiconductor count.

**M. Vinod Kumar Naik, Mohammed Aneesh Y. "Design of carry select adder for low-power and high speed VLSI applications", 2015. [9]**
In this paper carry select adder for low power VLSI design is implemented. Basically, in the applications of multi standard wireless receivers, portable mobile devices and bio-medical applications adders are most widely used. Main component in arithmetic unit is adder which plays major role.

**N. Ravindran, R. Mary Lourde, "An optimum VLSI design of a 16-BIT ALU", 2015. [10]**
In this 16 bit ALU is designed to optimize the VLSI design. By using the mixed logic families, 16 bit Arithmetic Logic unit is designed. Mixed logic families are the combination of pseudo-NMOS (N-Type Metal Oxide Semiconductor) for AND logic and Pass Transistor logic for multiplexers, CMOS (Complex Metal Oxide Semiconductor) for basic logic functions. This will optimize the performance. Design is validated based on the schematic editor which implements the chip level design.

## III. VLSI ARCHITECTURE OF BINARY ADDER

The below figure (1) shows the structure of VLSI architecture of binary adder. Input 'a' and input 'b' are assigned in particular order. Next pre-processing stage will be performed. In pre processing stages both propagator and generator signals are generated. Propagator and generator unit generate the signals of propagate and generate. Black cell and grey cells are generated in Carry generation unit. Addition is performed using adder tree block. At last output is saved in post processing stage.

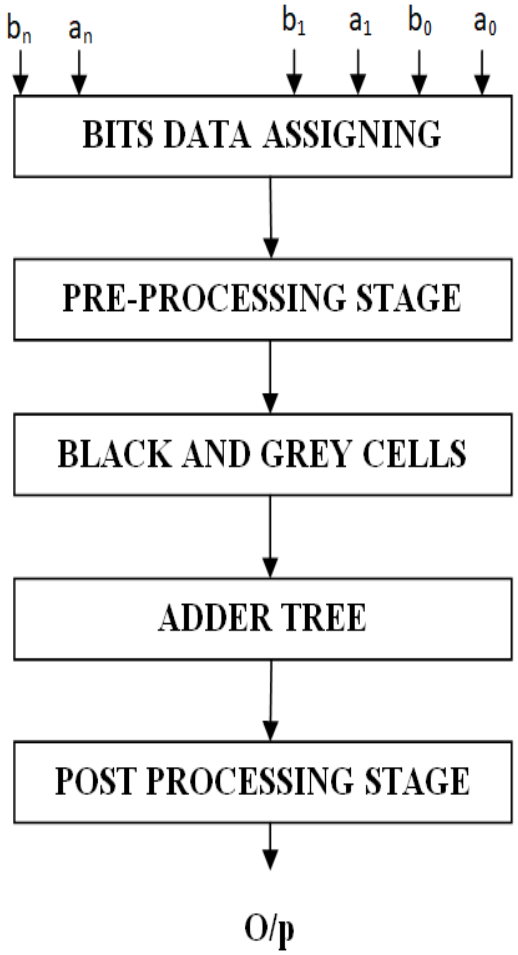


**Fig. 1: STRUCTURE OF VLSI ARCHITECTURE OF BINARY ADDER**

**Stage 1:** In this pre-processing stage carry propagate and generate signals are produced. For binary adder it has carry propagate and generation logics which performs XOR and OR gates. Only one gate for each signal therefore, the delay is 1τ.

**Stage 2:** By using the carries and bits calculation of carry generation stage is performed. By using parallel format entire operation is performed. Generate and propagate signals are obtained from intermediate signals. Propagate and generate signals equations are given below. Equations are implemented by the black cell and grey cell.

Pi:j = Pi:k AND Pk-1:j

Gi:j = Gi:k OR (Pi:k AND Gk-1:j)

**Stage 3:** Based on the input bits calculation is performed in post processing stage. In post processing stage Sum and carry is generated.

## IV. RESULTS

RTL schematic of proposed system is shown in below figure (2). Inputs are represented as ‘a’ and ‘b’. Outputs are represented as sum and carry.

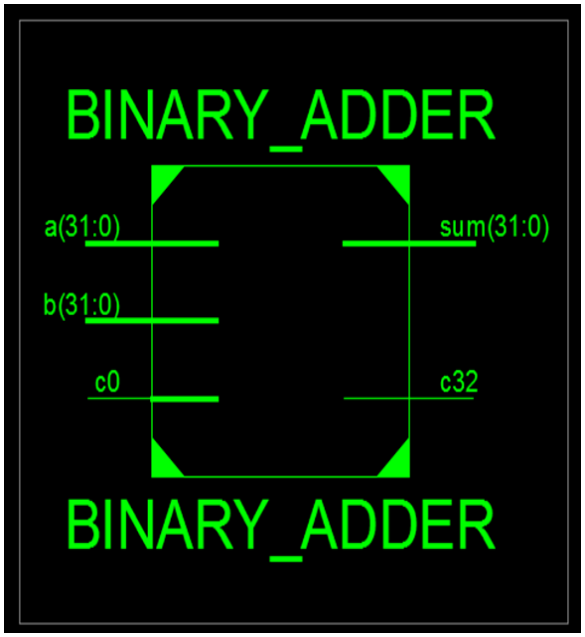


**Fig. 2: RTL SCHEMATIC OF PROPOSED SYSTEM**

The technology schematic of proposed system is shown in below figure (3). Technology schematic is the combination of look up tables, truth tables, K-Map and equations.

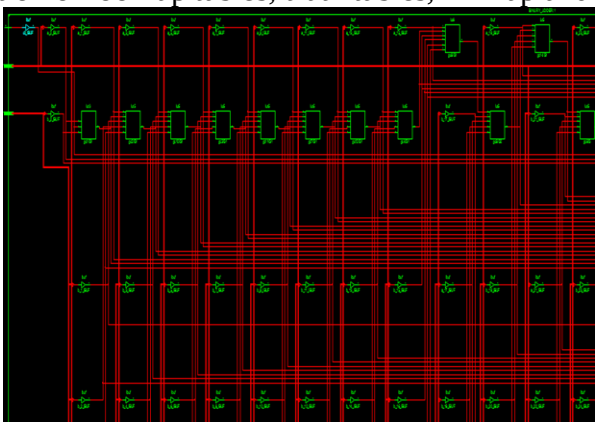

Fig. 3: **TECHNOLOGY SCHEMATIC OF PROPOSED SYSTEM**

**Fig. 4: OUTPUT WAVEFORM OF VLSI ARCHITECTURE OF BINARY ADDER**

The comparison table of existed and proposed system is shown in below table (1). In this LUT's, Total Delay and memory used parameters are utilized. Compared with existed system, proposed

system gives effective outcome.

**TABLE. 1: COMPARISON TABLE**

| S.NO | Parameters | Existed System | Proposed System |
|---|---|---|---|
| 1 | LUT's | 68 | 53 |
| 2 | Total Delay | 14.4 ns | 9.6 ns |
| 3 | Memory Used | 312 Mb | 273 Mb |

The comparison of LUT' for both existed and proposed system is shown in below figure (5). Compared with existed system, proposed system will use less number of LUT's.

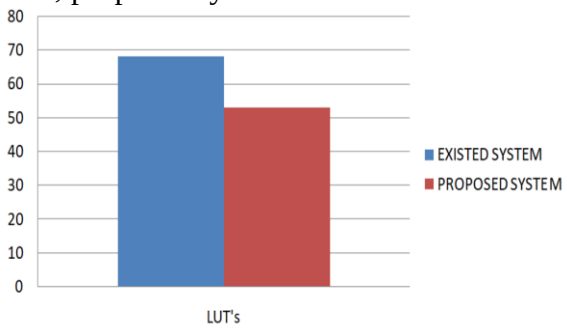


**Fig. 5: COMPARISON OF LUT's**

The comparison of total delay for both existed and proposed system is shown in below figure (6). Compared with existed system, proposed system will reduce the delay.

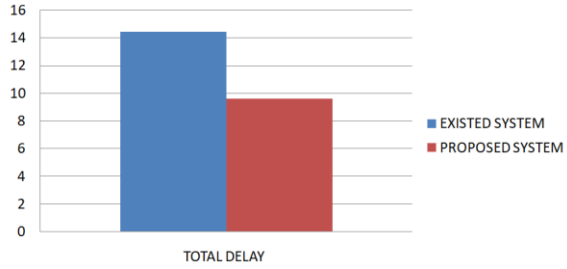


**Fig. 6: COMPARISON OF TOTAL DELAY**

The comparison of memory used for both existed and proposed system is shown in below figure (7). Compared with existed system, proposed system will reduce the usage of memory.

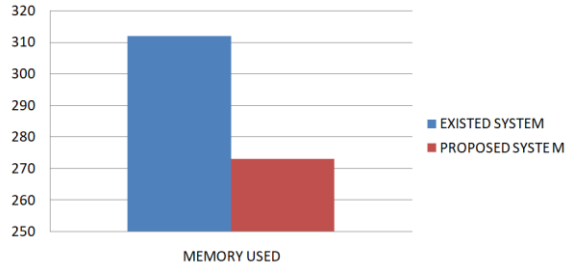


**Fig. 7: COMPARISON OF MEMORY USED**

## V. CONCLUSION

Hence in this paper the design and implementation of a high speed and area efficient VLSI architecture of binary adder was implemented. Propagator and generator unit generate the signals

of propagator and generator. From results it can observe the RTL schematic, Technology schematic of binary adder. In future, Arithmetic based sub systems will consists of Shannon based adder cell, high performance low power full adder, high speed counter using GDI technique and Vedic multiplier designs.

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