DESIGN AND IMPLEMENTATION OF AREA EFFICIENT PIPELINED FFT PROCESSOR

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ABSTRACT: In this paper the design and implementation of area efficient pipelined FFT processor is implemented. Basically FFT supports the bit size which is suitable to the system and mostly used in long term evolution systems. Transport triggered architecture is utilized to customize the size of fault free FFT processor. The inputs 1 and 2 are controlled by control unit. Input 1 performs the addition operation and input 2 performs the multiplication operation. Address generation unit will generate the address for both input 1 and input 2. Radix-2 FFT processor will process the entire data by generating address. Twiddle factor will increase the speed of operation. Hence all the data will be saved in memory unit. At last from simulation result it can observe that reconfigurable memory based FFT processor gives effective outcome.
KEY WORDS: FFT (Fast Fourier Transform), Radix-2, Multiplier, Adder, Twiddle Factor, Memory Unit, Control Unit.

I.INTRODUCTION

The FFT network design is much essential in the fields like communications and digital signal processing circuits. It has a great design approach for developing any software or hardware fields. The various functions can be implemented in VLSI circuits based on single-path delay feedback (SDF) arrangement [1]. Initially it is concentrate only on single radix computation. Recently this technique extends its computation capability to a multiple radix processing. This FFT method is broadly utilized in several signal processing and communication related applications.

This system needs efficient operational speed, low power utilization, diminished truncation error and minimized chip size. By utilizing FFT numerical idea can be effortlessly developed in real time applications. It is likewise fit for changing the information starting with one mode then onto the next mode. OFDM is an emerging technique which can able to implement many practical life applications.

The OFDM stands for orthogonal frequency division multiplexing. By using VLSI and system-on-chip (SoC) design technology in which millions of components were implemented on a single chip so it's possible to fabricate huge FFT network on a single chip. This technology can bring remarkable challenges and diagnosis [2]. Especially the cost of the diagnosis increased rapidly with the complexity of the chip.

So it's a very important to control the cost of a circuit design. Hence it's essential to implement a technique which works on fault detection. The fast growth of these VLSI technologies increases the complexity and decreased the feature size the components. So it's a highly complicated to get better accuracy and standards of chip. Therefore a technique called fault-tolerance will be required. Various testable structures and fault-tolerant design methods are developed to improve the exhibition of the chip testability and reliability of FFT systems.

The floating point based fault- tolerant FFT processor comprises of butterfly units with defect discovery circuit, switching circuit and control circuit. This arrangement can make a perfect connection with shuffle. The control circuit can be able to control the switching circuit and it also arranges a transition which can be useful to determine the connections between output and input of butterfly units.

There is a another method called Modular Redundancy (MR) which is used to triple a block and select among three output in view of detecting and correcting errors. The soft errors mitigation techniques give a less system performance because it gives huge overhead in terms development of system.

A method to detect and correct the errors based on algorithmic properties of the circuit is known as algorithm based fault tolerance (ABFT). This technique can limit the overhead that needs to ensure a network. ABFT technique will be well opted in the fields like VLSI and communication. To protect digital filters from overhead several methods were implemented. The information about distribution of output of filter is also utilized to detect and correct faults with lower overheard. It's also very important to protect FFT filters from overhead, because FFT will be used various applications.

A system will be introduced that simply dependent on the error detection and correction codes (EDC). In this technique each filter can be considered as identical of a bit in an EDC and by utilizing addition operation the redundant bits are determined. The discrete Fourier transform (DFT) is one of the practical examples of this technique [3]. In practical, to execute this procedure it is imperative to anticipate that there can be simply single fault on the system at any snapshot of time. For an assurance against radiation actuated soft errors, this is the basic expectation.

Since there a drastic growth in the communication and signal processing fields, concept of IC (Integrated Circuit) technology evaluated and by using this technology millions of transistors are designed on a single chip. It decreases power consumption, size and area but in turn it is more sensitive to errors. So those faults or errors are minimized by using fault tolerance methodology. Two redundancy techniques are available. They are software redundancy or hardware redundancy and information redundancy. The coding that related to error correction or fault detection can be mainly processed with binary data.

The binary data has two values such as binary 0 and binary 1. So it is very easy to identify the faulty location. In computers the information is transferred by means of binary data. In the computers the special error correction techniques will be used to detect and then correct the errors with a great accuracy and precision [4]. After correction of errors it can able to activate the operator in the sense that there exist errors in the system.

The input data is generally in binary form. The data in binary form will be derived from analog data using ADC. This conversion requires sampling and quantization operation to convert analog signal into digital signal. Original modules can transfer the same information to comparison

section. Similarly input is also fed the comparison block but after it is passed through redundant module.

The redundant modules filter the unwanted data so that its output is data without unessential data. The comparison block consists of two types of inputs, one is original data and another one is a redundant data. After performing the comparison operation it sends the data to a butterfly unit [5]. Both the FFT and Inverse FFT are almost same in terms of their mathematical notation with a small variation.

II.RELATED WORK

It's a very essential to maintain better computing accuracy and deriving large discrete Fourier transform (DFT) while designing a digital signal processing circuit. This can be achieved by a FFT design. The FFT circuits are most preferable because this circuit gives better throughput and performance. Choi and Malek introduced a fault model scheme which was developed based on re-computation via another path. This is fault tolerance method implemented for FFT [6].

This technique decreases the throughput of a system so it requires maximum time overhead to protect the circuit. It's essential to determine FFTs or digital filters in parallel because the signal processing or communication circuits are became more complex. In digital filters or in communication based systems in which the circuits consist of MIMO structure. The MIMO stands for multi-input and multi-output. The OFDM was effectively used in various communication circuits.

These two techniques are used together in FFT design for modulation and demodulation. This technique reduces power consumption, area and errors occurred in a circuit. The soft error mitigation method is used to reduce soft errors while designing any circuit. This technique requires a huge overhead for circuit development [7]. The error detecting and correcting codes are needed to make a system as fault tolerant by the way of detecting and correcting the errors.

At present a technique will be introduced to maintain a fault -free system called error detection and correction codes (EDC). The technique that mostly uses the term butterfly for the computational issues is called Cooley–Tukey FFT algorithm. In this algorithm, the most frequently the large FFT can be broken into smaller. In this method the sum of individual output is equal to the sum of some inputs. This is faithful to any operation that based on linearity. There are two redundancy methods to reduce the error in FFT network [8].

The NMR (N-module redundancy) is capable to definite error detection and correction. Though it's an optimized technique in terms of fault tolerance, but it consumes high rate of power. The overhead becomes doubled in typical triple modular redundancy (TMR) when compared to the conventional design techniques. A new technology was developed in 2006 by Snodgrass known as Reduced Precision Redundancy (RPR), the main idea of behind this technique is maintain a good balance in between calculation accuracy and power consumption [9].

Another technique that was based on information redundancy is additionally, capable to reducing the fault tolerance and errors in the circuit to better extent. Concurrent error detection (CED) is also a better information redundancy method to reduce the overhead. For FFT design circuit

computation, two conventional techniques are implemented. First Parseval's theorem based on sum of squares (SOS) check bit and convolution theorem.

These two techniques has capable of reduce the overhead of the circuit and in turn protect the circuit in an effective way. The architecture of conventional FFT consists of three components such as Butterfly (BF2) architecture, Delay unit and commutator (C2) block. This architecture is most efficient proposal for better implementation of FFT algorithm for radix -2. This can rearrange the data easily for FFT/IFFT algorithm. In this technique, the FFT circuits with hybrid radix can be computed [10]. For different FFT sizes the better reading and writing of data for data storage can be implemented by 2D-FIFO arrangement.

III. PIPELINED FFT PROCESSOR

The below figure (1) shows the block diagram of proposed system. The inputs 1 and 2 are controlled by control unit. Input 1 performs the addition operation and input 2 performs the multiplication operation. Address generation unit will generate the address for both input 1 and input 2. Radix-2 FFT processor will process the entire data by generating address. Twiddle factor will increase the speed of operation. Hence all the data will be saved in memory unit.

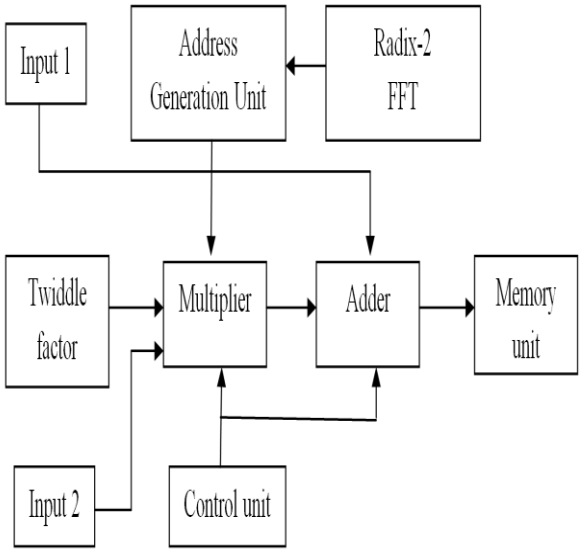

Fig. 1: BLOCK DIAGRAM OF PROPOSED SYSTEM

Twiddle factors (represented with the letter W) are an set of values that is used to speed up DFT and IDFT calculations. The twiddle factor is a rotating vector quantity. All that means is that for a given N-point DFT or IDFT (Discrete Fourier Transform or inverse Discrete Fourier Transform) calculation, it is observed that the values of the twiddle factor repeat at every N cycles. The expectation of a familiar set of values at every (N-1) th step makes the calculations slightly easier. (N-1 because the first sequence is a 0).

Radix 2 means that the number of samples must be an integral power of two. The decimation. In time means that the algorithm performs a subdivision of the input sequence into its. A fast Fourier transform (FFT) is an algorithm that computes the discrete Fourier transform (DFT) of a sequence, or its inverse (IDFT). Fourier analysis converts a signal from its original domain (often time or space) to a representation in the frequency domain and vice versa.

IV. RESULTS

RTL schematic of proposed system is shown in below figure (2). RTL schematic of the combination of both inputs and outputs.

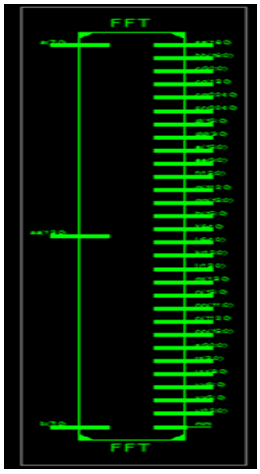

Fig. 2: RTL SCHEMATIC OF PROPOSED SYSTEM

Technology schematic of proposed system is shown in below figure (3). Technology schematic is the combination of LUT's, Truth tables, K-Map, Equations and Buffers

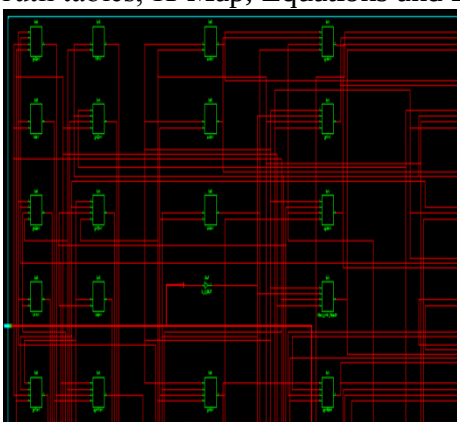

Fig. 3: TECHNOLOGY SCHEMATIC OF PROPOSED SYSTEM

The below figure (4) show the input waveform of proposed system.

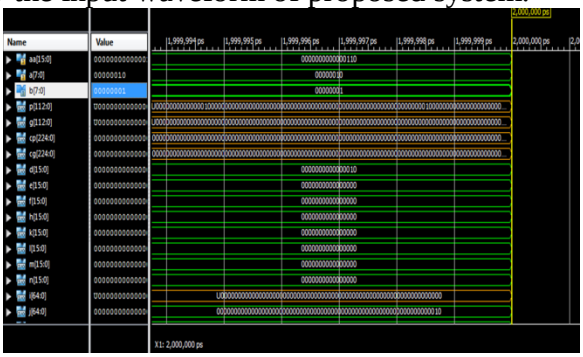

Fig. 4: INPUT WAVEFORM OF PROPOSED SYSTEM

The below figure (5) show the input waveform of proposed system.

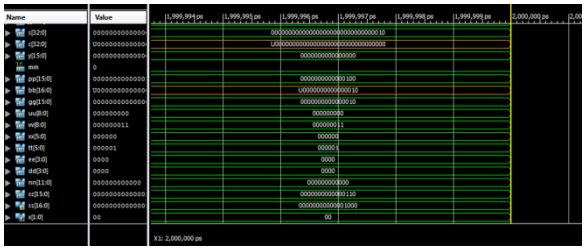

Fig. 5: OUTPUT WAVEFORM OF PROPOSED SYSTEM

TABLE. 1: COMPARISON TABLE

V. CONCLUSION

In this paper the design and implementation of area efficient pipelined FFT (Fast Fourier Transform) processor was implemented. In present day sign preparing circuits, it is entirely expected to discover few channels working in parallel. Reconfigurable memory based FFT processor framework is a zone productive system to identify and address single mistakes. Address generation unit plays very important role in entire system. From results, it can observe that the proposed system gives effective output

S.NO	Parameters	Existed System	Proposed System
1	LUT's	581	532
2	Total Delay	19.6 ns	17.4 ns
3	Memory Used	412 Mb	333 Mb

VI. REFERENCES

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