DESIGN A LOW-LATENCY NOVEL FPGA BASED SIGNED MULTIPLIER FOR COMMUNICATION APPLICATIONS

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ABSTRACT: The most expensively utilized arithmetic operation in broad range of application is multiplication. For providing high performance and resource efficient multipliers earlier researches has been presented various accurate and approximate multiplier designs majorly utilized for ASIC (Application Specific Integrated Circuits)-based systems. Though the infrastructural differences among FPGA-based and ASIC system confines the multipliers effectiveness for FPGA (Field Programmable Gate array)-based systems. In addition many of these designs of multiplier are only valid to unsigned numbers. For bridging this gap design of a low-latency novel FPGA based signed multiplier for communication applications is presented in this paper. This multiplier design can be implemented in four steps pre processing, barrel shift register, parallel adder and post processing stages. Partial products are generated in preprocessing stage which are used to realize propagate and generate signals. Then these partial products are shifted and aligned in a sequential order for further computation using barrel shift register. From this barrel shift register partial products are applied to parallel adder structure for the carry generation and propagation. Then final product output can be obtained in the post processing stage by performing the final addition operation. The implementation of presented design is simulated using Xilinx ISE design suit 14.7v software.
KEYWORDS: Field-Programmable Gate Array (FPGA), multiplier, partial products, barrel shift register, parallel adder.

I. INTRODUCTION

The multiplication operation is one of the primary arithmetic operations and it is extensively utilized in image processing and DSP (digital signal processing) environments. Vendors of FPGA are Intel & FPGA, provides DSP blocks to accomplish fast multipliers [1]. However the DSP blocks offers the high performance, usage of these blocks may not be effective in area requirements & overall performance for few applications. It might have possibility for performing manual floor planning to optimize the overall performance of an application for small applications. Although for FPGA resources, the complex applications with contended requirements may not be feasible for optimizing required FPGA resources placement to improve performance gain. In the same way the implementation of JPEG-encoder representing huge number of DSP blocks (overall available DSP blocks are 56%) usage. These kinds of applications will exhaust available DSP blocks and makes them less available/unavailable to critical operation performance of other applications which are executing simultaneously in same FPGA & LUT (Look Up Table) - based multipliers are necessitated [2-5].

In the earlier days by using addition, subtraction & shift operations multiplication was performed. Multiplication process can be hard in terms of repeated additions [6]. By adding number many times product can be obtained i.e., multiplier with another number produces multiplicand. At each addition step partial product is produced. In several processors, normally operand consist equal number of bits. If the operands are taken as integers then length of the product is typically twice of the operands length because without loss it contains the information. This repetitive addition increments the product length as to area by the arithmetic algorithm which is slow that has been replaced with an algorithm that can makes the positional

representation utilization [7]. The multipliers are possibly divided as 2 parts. For the generation of partial product term first part is assigned, second part collecting the partial products & adding them. The basic principle of multiplication process having 2 main processes, they are partial production estimation & shifted partial products gathering. This can be performed by the columns successive addition of shifted partial product matrix. To get the suitable 'multiplicand' bit the 'multiplier' is shifted effectively. Adding them again forms the product bits. Hence multiplication is an operation of multi operands [8]. For broadening the multiplication to the both unsigned & signed numbers in a convenient system is the two's complement format representation

II. LITERATURE SURVEY

S. Bokade and P. Dakhole, [9] in this examination, Radix4 MBE (Modified Booth Encoding) is utilized for partial production generation. Based on pipelining a 32-bit multiplier is presented. The major objective of this presented multiplier is delay reduction of higher bit multiplier and to fasten the computation. This multiplier is implemented through Xilinx 14.2. Achieved delay is 2.826ns in 32x32 bit signed multiplication computing with 353.832 MHz maximum frequency over device. R. Balakumaran and E. Prabhu, [10] in this examination new technique for accumulator and multiplier is presented through combining hybrid carry look-ahead adder (CLAA) and reversible logic functions. Here modified booth algorithm provides less delay compared to basic multiplication operation. In addition it moderates the number of partial products.

The CLAA is utilized to control the total MAC (Media Access Control) delay. The reason behind designing reversible logic is reducing the information loss, consumption of power and complexity of circuit. A survey is carried out over feasible ways for making a design of full adder utilizing various reversible gates. In addition they reported a novel hybrid CLAA from existing hierarchical CLAA that obtains high performance in terms of consumption of power, area and computation in their examination. Further they reported resulted design delay, power and area complexities.

In P. Saxena, [11] examination, the architectures of CSA (carry select adder) are presented utilizing PPA (parallel prefix adder) instead of RCA (Ripple carry adder), here PPA i.e BK (Brent Kung) adder is utilized for designing regular linear CSA. Basic building blocks in any digital integrated circuit based designs are Adders. The RCA is the more impact design but it requires more computation time. The CLA is utilized in critical time applications for deriving fast result this in turn leads to large area requirements. The CSA is a compromise among CLA and RCA in terms of delay, area. The RCA has large delay so that it is replaced with PPA which provides faster results. Here the architectures of 16-bit regular linear BK CSA, Regular SQRT (square root) BK CSA, Modified SQRT BK CSA and Modified Linear BK CSA are designed.

V. Vijayalakshmi, R. Seshadri and S. Ramakrishnan,[12] their research discussed the comparison between VLSI design of 32-bit unsigned integer multiplier based on CSLA (carry select adder) and the VLSI design of 32-bit unsigned integer multiplier based on CLAA. Both these multiplier designs multiply two 32-bit unsigned integers and produce 64 bit products. The multiplier based on CLAA utilizes 99ns delay time to perform the operation of multiplication while the CSLA based multiplier also utilizes approximately same delay time for performing the operation of

multiplication. But the area required in CLAA multiplier is decreased to 31% through CSLA multiplier for completing multiplication.

S.Srinivas, K.Nagarjun [13] presented a novel concept of multiplication utilizing reversible logic gates and modified booth algorithm. Here reversible logic gates with modified booth algorithm are simulated and synthesized by Xilinx ISE simulator. M. N Shanmukha Swamy, Ravindra P Rajput [14] presented a high speed 8x8 MBE (Modified Booth Encoder) multiplier design for unsigned and signed numbers. The CLAA and CSLA adders are utilized to increase the speed of multiplication for producing different simulation results for given binary form unsigned and signed numbers in the presented 8x8 MBE multiplier. Nishat Bano [15] presented a design of booth multiplier and is implemented in Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). In addition presented multiplier compares delay and power consumption of radix-4 & radix-2 booth multipliers. The radix-4 booth multiplier consumes 22.9 less power than traditional radix-2 multiplier when radix-4 is implemented over FPGA.

III. FPGA BASED SIGNED MULTIPLIER

The Figure 1 represents the proposed memory based multiplier architecture. The whole system is categorized into following modules. The following modules are inputs A and B, pre processing stage, partial products, Barrel shift register, parallel adder and post processing stage. Now barrel shifter will shift the data words by sequential bits. Then the alignment of partial products generator will be done. Now these bits perform the addition operation using parallel adder and give the final product by subsequently performing post processing operation.

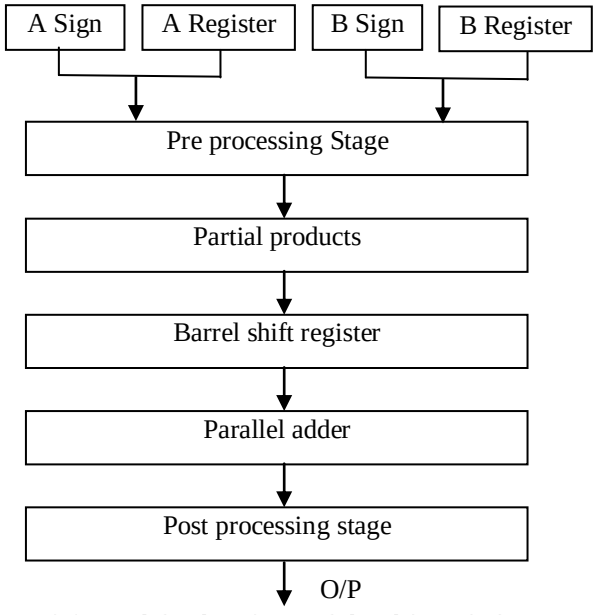

Fig. 1: BLOCKDIAGRAM OF FPGA BASED SIGNED MULTIPLIER

First the operands are placed in to multiplier design, here A, B are the input operands. The arithmetic operations such as multiplication and addition are performed. The shifter saves these obtained results. The function of irreducible polynomial is not utilized in this system. The multiplier register is used for storing the representation of bits and producing a(t) polynomial output. The operation of parallel load is carried out in the position of MSB (most significant bit).

Similarly the shift operation is done at MSB. The utilized multiplicand (md) bi as b(t) value is saved in the register. In addition the operation of parallel load is applied in multiplicand and the resulted value is saved in register. In register block right shift operation is carried out. For transferring the multiplicand register data a Crypto core processor is utilized.

3.1 Preprocessing Stage

In this stage it can computes signal pair named as propagate signals & generate that will corresponding to each i^{th} state of input sets of A & B. Generate & propagate signals computation is represented in below equations:

$$G_i = A_i \; AND \; B_i \qquad \text{---------- (1)}$$

$$P_i = A_i \; XOR \; B_i \qquad \text{---------- (2)}$$

3.2 Partial-Products

An alternative method to solve the problems of multi – digit multiplication is Partial –Product Multiplication. Based on the multiplication distributive property this strategy works. Multiplier LSB creates the first partial product; the second bit of the multiplier creates the second partial products, etc. Using accurate adder circuit the final partial products are added.

3.3 Barrel Shifter

Barrel shifter is a digital circuit that shifts the word data with specified number of bits and uses combinational logic only and do not use any sequential logic. This barrel shifter contains load multiplier (mr), roots are considered as inputs of this block. Generally the multiplier register is connected to finite field arithmetic circuit. Similarly the multiplicand register contains daya_in, load_md and shift bits that are considered as inputs of barrel shifter. This can load the data and shifts them in efficient manner. The result register contains output and stores whole arithmetic operations results. Presented system provides better results compared to traditional systems. In barrel shifter block both b(t), a(t) values are assigned. In barrel shifter the resulted values shifts the bits to adder block. Addition operation is performed in this adder block. The bits are shifted to result register after completing the specific operation. The result register stores the final output as product. Finally barrel shifter can perform the parallel operation in an effective manner.

3.4 Parallel Adder

Parallel adders are used to find the arithmetic sum of two numbers which is more than one bit in length and corresponding pairs of bits are processed in parallel form. The efficiency of a squaring circuit can be improved by using parallel adders. A carry and sum are generated by the parallel adder at last the MSB to be added. An 'n' bit parallel adder requires 'n' full adders for performing the addition operation. In this process much earlier the carriers have been computed utilizing 2 cells that are explained below.

Black Cell: As input it considers 2 pairs of generate & propagate signals (G_i,P_i) & (G_j, P_j) and for current phase these signal pairs (G, P) are computed as output.

$$G = G_i OR \; (P_i AND P_j) \qquad \text{------- (3)}$$

$$P = P_i AND P_j \qquad \text{------- (4)}$$

Grey Cell: As input it considers 2 pairs of generate & propagate signals (G_i,P_i) & (G_j,P_j) and for current phase generate signal G is computed as output.

$$G = G_i OR \; (P_i AND P_j) \qquad \text{------- (5)}$$

3.5 Post Processing Stage

The final stage for computing sum is common in all PPA family adders. In this step sum computation is involved, and is given as

$$S_i = P_i XOR\ C_{i-1} \qquad \text{------- (6)}$$

$$C_{out} = G_n \qquad \text{------- (7)}$$

IV. RESULTS

The Xilinx design environment was used to implement and examine the developed algorithm. The FPGA architecture of proposed FPGA based signed multiplier design is shown in Fig. 2 & Fig. 3. The below Fig. 2 and Fig. 3 shows the RTL schematic and technology schematic of FPGA based signed multiplier. RTL schematic is the combination of inputs and outputs. Register-transfer logic deliberation is utilized in equipment portrayal dialects (HDLs) such as Verilog and VHDL for making elevated circuit level portrayals from lower-level portrayals and at last legitimate wiring can be found.

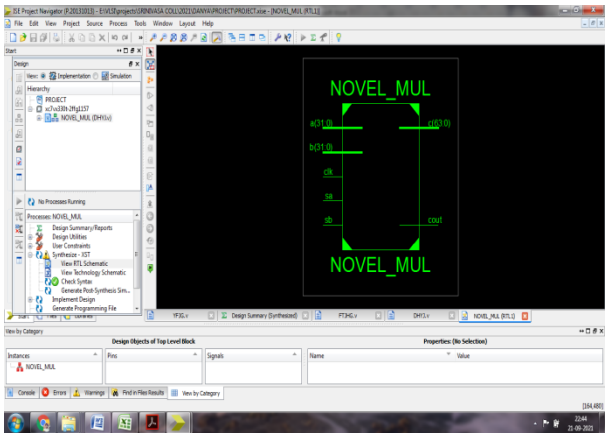

Fig. 2: RTL SCHEMATIC OF PROPOSED MUTIPLIER

Technology schematic is the combination of equations, K-Map, Truth tables and Look up tables. The presented adder technology schematic is shown in Figure 3.

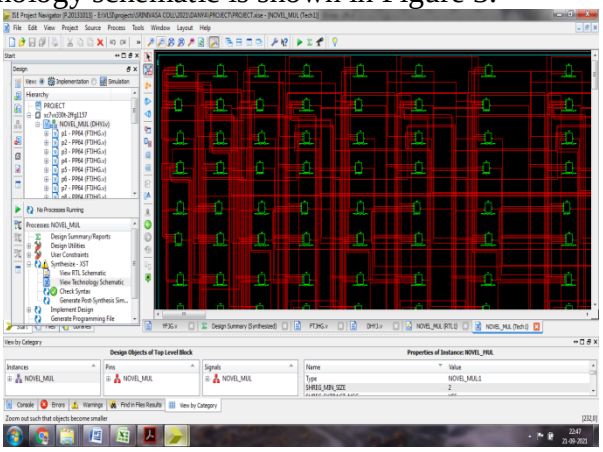

Fig. 3: TECHNOLOGY SCHEMATIC OF PROPOSED MUTIPLIER

After optimization & synthesis process technology target phase, the schematic is generated. The schematic represents the design in terms of optimized logic components for Xilinx target device, the logic components are carry logic, LUTs, I/O buffers & other specific technology components.

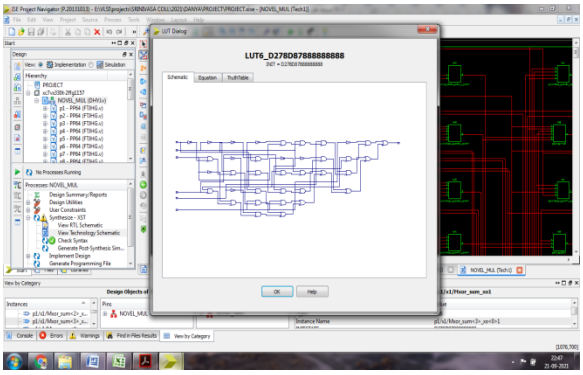

Fig. 4: LOOK UP TABLE (LUT) OF PROPOSED MUTIPLIER

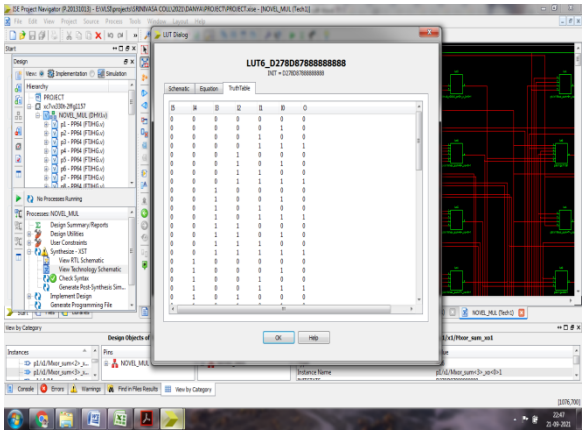

Fig. 5: TRUTH TABLE OF PRESENTED MUTIPLIER

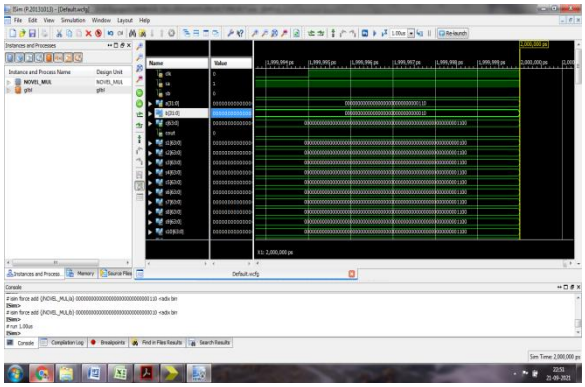

Fig. 6: OUTPUT WAVEFORMS OF PROPOSED MUTIPLIER

V. CONCLUSION

Design a low latency novel FPGA based signed multiplier for communication applications was presented in this document. This multiplier architecture has four-stage structures to get final output such as preprocessing stage, barrel shift register, parallel adder and post processing stage. In the first stage of preprocessing, propagate and generate signals obtained by taking the two input signed numbers. Then the partial products are generated by using a partial product

generator. Barrel shift register was used to shift the partial products by sequential bits to order them in alignment. The aligned partial products are then added utilizing parallel adder and give the final product by subsequently performing the carry propagation in post processing stage.

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