An Effective Approach for MSIC: An Applicationof Built inSelf-Test

V. Madhavi[1], M. Lalsingh[1], Sravan Kumar P[1]
Department of Electronics and Communication Engineering, Sree Dattha Institute of Engineering and Science, Telangana, India.

Abstract

In BIST design the ATPG is the one of critical thought. The execution likewise the relies on upon the suitable ATPG era. In our paper we propose the novel technique for multiple single input change (MSIC) test designs that are planned for the sweep chain. So as to build up any technique, we have to consider the region and power angles for the progressed VLSI plans, and furthermore ready to play out the test proficiently utilizing test-per-clock and the test-per-check procedures. The correct investigation for the plan of MSIC additionally gave. The execution assessment is finished by planning in VERILOG and utilizing reenactment and union instruments like Model-sim 6.6 and Xilinx14.3 the yield exhibit and check ISCAS benchmarks can be utilized. The proposed technique gives proficient blame scope without increment of BIST design and test time.
Keywords: BIST, Test Pattern Generation, Circuit-under-test, MSIC, LFSR and SIC

1. Introduction

VLSI on chip testing is extremely troublesome and an essential thought for the present propel frameworks. To accomplish the run time testing we presents the idea called worked in individual test (BIST), in this giving the testing environment alongside the circuit-under-test (CUT). In conventional BIST structures the hand-off on the linear feedback shift register (LFSR) and multiple input mark register (MISR) are utilized for the era of Test examples. By utilizing the techniques for test designs causes the downsides like high exchanging action and high-Power utilization and more test time, this may influence the conduct operation of the CUT and has the maturing issue. By utilizing these strategies, we have to create the greater number of test example for the powerful blame scope.

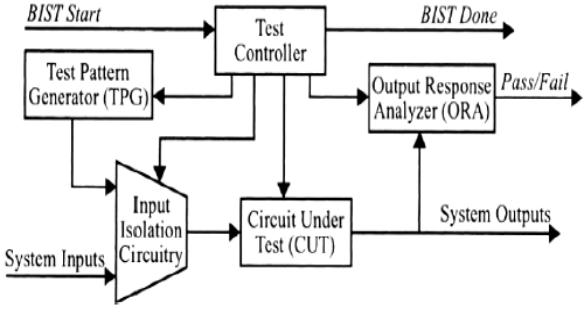


Figure 1. BIST Basic block diagram.

The customary pseudorandom designs can't be able to distinguish the new blames. They are by and large patched for the conventional blame identifications. These test techniques have high blame scope with least number of test examples moreover. Yet, the significant issue that related with these techniques are the high zone and power overhead conditions. Distinctive progress less power examine based technique are proposed in past by changing the less power models and rolled out a few improvements in sweep way plans keeping in mind the end goal to got unchanged input when taking care of the shift operations. In another approach that uses the

many sweep empowers by utilizing the many output chains that enacts any one at ones that likewise decreases the general utilization of operation force of sweep-based tests of CUT.

2. Literature Review

This is one of the designs for testability (DFT) instrument that can ready to test the circuit at the run time. The propel configuration highlight that has fit for tasting utilizing the implicit test setup that ready to build the testing norms and furthermore the testing time. The fundamental BIST requires the components like vermin example generator for demonstrating the test input designs, test controller utilized for whole test control and reaction analyzer utilized for the investigation of yields of shape the CUT and tells whether test is pass or fizzle.

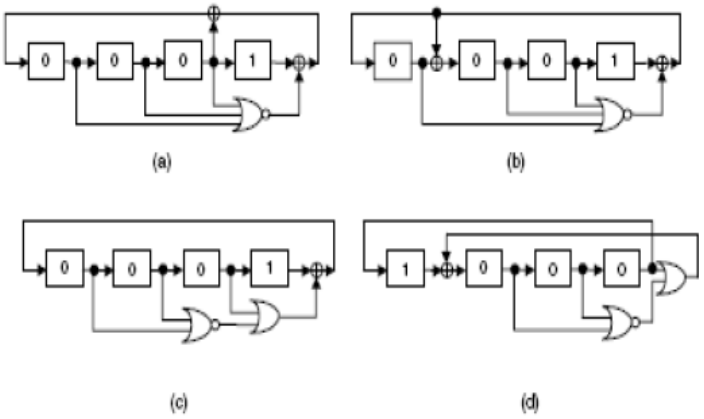


Figure 2. Example of LSFR.

The above demonstrated are the distinctive LFSRs utilized for the era of test example era. In any case, the real disadvantage that has with utilization of these LFSRs as test example generator (TPG) that gives high exchanging power significantly more than the ordinary operation of the CUT that causes the expansion of operation power and that likewise drives the operation delay.

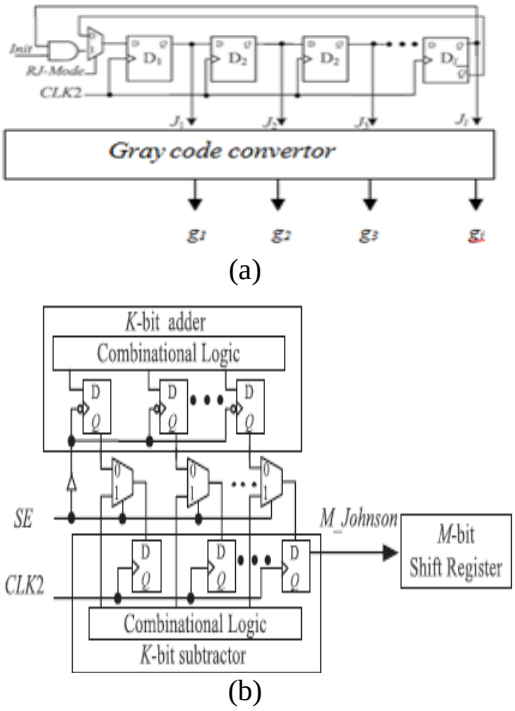
3. Proposed Method

This area depicts the proposed test patter outline that ready to give the less move test vectors connected for the multiple output chains. In the first place, the essential mark vector is loosened up to poly code words and these are XOR with the proposed outline marks and bolstered to the all sweep chains. The proposed BIST setup comprises of the fundamental LFSR and mark assessment circuit that comprises of the Johnson Counter and the dark code converter.The primary vectors that are generated from the LFSR are can be termed as the $S(t) = S0(t)S1(t)S2(t), \ldots, Sm-1(t)$ and the vector generated by an l-bit Johnson counter can be labeled as as$J(t) = J0(t)J1(t)J2(t), \ldots, Jl-1(t)$. For the first clock cycle, $J = J0\ J1\ J2, \ldots, Jl-1$ will bit-XOR with $S = S0S1S2, \ldots, SM-1$, and the results $X1Xl+1X2l+1, \ldots, X(M-1)l+1$ will be shifted into M scan chains, respectively.

In next clock cycle, $J = J0\ J1\ J2, \ldots, Jl-1$ will be gray coded as $J = g0,g1\ g2, \ldots, gl-1$, which can be bit-XOR with the seed $S = S0S1S2, \ldots, SM-1$. The resulting $X2Xl+2X2l+2, \ldots, X(M-1)l+2$ will be agitated into M scan chains, respectively. After the l clocks, every scan chain will be fully adulterated with a singular Johnson codeword, and signatures $S0S1S2, \ldots, Sm-1$ will be fed to m PIs. Depend upon the scan lengths this method able to generate two different types of SIC generators to generate Johnson code words and vectors separately.

The main purpose of concept is to mitigate the switching activity of CUT. The area of the design can be reduced by providing the appropriate relation with the decomposed vectors of certain particular vectors. That has feature of providing the selective patter allocation which

increase the evaluation. Major aspect that these patters should has unique to the each other that facilitates the reduction of test conduction time, in general when the pattern are repeating the overall test time also will increase which will not be ideal for the present advance VLSI systems. Finally, unique patterns are intended to reduce the test length (patterns that are required for the efficient fault coverage). The main aim of this section is to provide the required test vectors for the selective configured CUT. The implementation of the weighted-pattern generation scheme is based on the full adder. Therefore, in order to transfer the carry input to the carry output, it is enough to set.



(a)

(b)

Figure 3.SIC generators. (a) Gray coded Johnson counter. (b) Scalable SIC counter.

Table I. Truth table of the full adder

#	Cin	A[i]	B[i]	S[i]	C_{out}	Comment
1	0	0	0	0	0	
2	**0**	0	1	1	**0**	$C_{out}=C_{in}$
3	**0**	1	0	1	**0**	$C_{out}=C_{in}$
4	0	1	1	0	1	
5	1	0	0	1	0	
6	**1**	0	1	0	**1**	$C_{out}=C_{in}$
7	**1**	1	0	0	**1**	$C_{out}=C_{in}$
8	1	1	1	1	1	

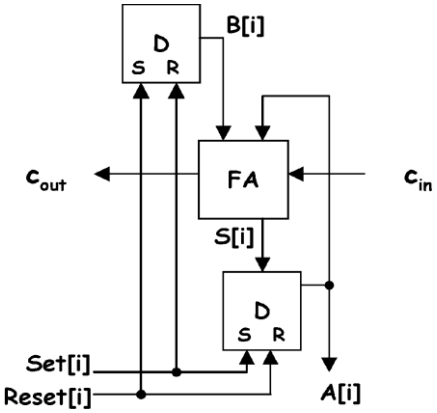


Figure 4. Accumulator cell.

The proposed plan depends on this perception. The execution of the proposed weighted example era plan depends on the collector cell introduced in Fig. 4, which comprises of a Full Adder (FA) cell and a D-sort flip-flop with non-concurrent set and reset inputs whose yield is likewise headed to one of the full snake inputs. In Fig.5, we accept, without loss of consensus, that the set and reset are dynamic high flags. In a similar figure the individual cell of the driving register B[i] is additionally appeared for this gatherer cell, one out of three designs can be used, as appeared in Fig.4.

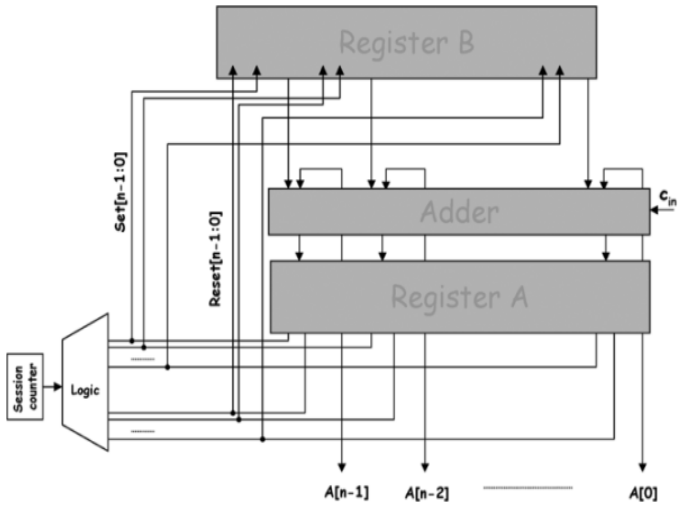


Figure 5. Proposed scheme.

Linear feedback shift register (LFSR) utilized as a part of numerous designs since it has the component of low power and furthermore possesses less territory. In this paper likewise we consider the LFSR as the fundamental component in proposed technique association and took after by the altered Johnson counter and dark code converter

4. Simulation Results

We have planned our proposed technique that will give the novel test designs that is appeared in roar fig6 reproduced wave shape. By this we can take note of that the dynamic force of the test design era can be lessened in light of the fact that the change of test examples is not that highly struck contrasted with past

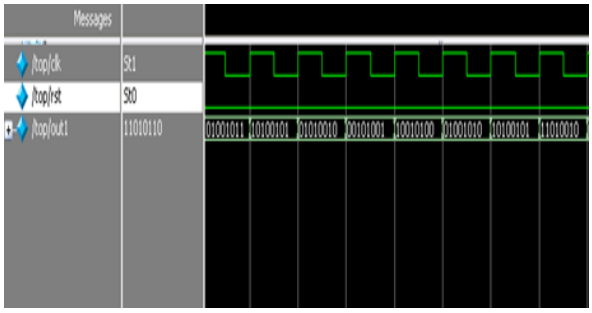


Figure 6. simulation of test pattern generator.

Supply Summary Source	Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.006	0.000	0.006
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.002	0.000	0.002

Supply Power (W)	Total	Dynamic	Quiescent
	0.020	0.000	0.020

Figure 7.power of test pattern generator circuit.

The static force of the proposed technique can be lessened. Whereas in the current strategy add up to power utilization can be 0.042A yet our proposed technique can use just 0.020A as it were. The force of the framework can be lessened that can be appeared in fig. 7.

5. Conclusion

We outlined a novel propelled strategy for test patter generator circuit which can reducers the static and element control effectively. Furthermore, lessens the maturing issue of the circuit. At the point when contrasted and the past strategy the hard product overhead can be lessened and furthermore truncates the aggregate test time and furthermore the aggregate power. Exploratory outcomes and check can be portrayed.

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