Energy-Efficient Routing for Ant Colony Optimization in VLSI Design

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Abstract— Due to the rapid advancement and growth in Very Large Scale Integrating VLSI design posed a number of challenges. With an increasing number of transistors in a chip, reducing power consumption is a very important goal and a major priority for designers to increase efficiency. The efficient development of a system with a billion chips and blocks on a printed circuit board requires extensive it is important to optimize the usage of different design areas such as chip size, component separation, interconnecting length. Optimizing the Routing phase in the VLSI design cycle is a very important option to reduce power consumption in VLSI design. The role of the routing process is to determine the shortest paths to connect between the chip components. Reducing wire lengths is very important because it leads to reducing the capacitance of the chip and hence power consumption. There are many algorithms that try to decrease wire lengths and decrease capacitance like Ant Colony Optimization(ACO), Artificial Bee Colony (ABC), Particle Swarm Optimization (PSO). In this paper we will try to improve Ant Colony Optimization (ACO) algorithm to remove some of the limitations of the original ACO algorithm. ACO algorithm used to find optimal routes with minimum capacitance for interconnect routing on VLSI chips.

Keywords— Ant colony optimization(ACO), VLSI design, global routing, wire length, power consumption, interconnect.

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1. INTRODUCTION

VLSI is the process that combines many numbers of transistors into Single Integrated Chip (IC). As the number of transistors increases the interconnecting wires lengths increase. As interconnecting wires lengths increase the capacitance and time delay increase which leads to increasing power consumption and hence decreasing efficiency of the chip. Also, the interconnecting wires have constraints like fixed area and width which make the wire length is a very important parameter in the VLSI design. Due to this, there is routing techniques are very important in VLSI design. So the routing phase plays an important rule n VLSI physical design cycle. The minimization of wire length will make an efficient VLSI design. Routing

is very important to follow the design rules of the chips in VLSI design. Where minimizing the wire length leads to decrease capacitance then decreases power consumption. Routing between nodes is considered an NP-complete problem hence there is no certain algorithm to find the optimal routing in polynomial time. Due to the high complexity of the VLSI routing problem there are many solutions to this problem. So the routing problem is usually solved by the usage of a two-stage approach which is global routing followed by detailed routing [1]. Global routing first divides the routing region into nodes and decides nodes to nodes paths for all nets and its function is to optimize total wire length and circuit timing. Capacities and various constraints are assigned to the edges and vertices in this 3D routing graph so routing can optimize routability, timing, power. Then, the detailed routing guided by

the paths obtained by global routing to assign the tracks and vias for nets trying to minimize the design rule violations. This paper deals with the global routing phase which we will try to minimize the wire length hence decrease time delay of the circuit. Many algorithms tried to solve VLSI routing problems like genetic algorithm [2], particle swarm optimization [3], ant colony algorithm [4], and artificial bee colony algorithm [5]. In this paper, we have proposed a global routing algorithm based on the Ant Colony Optimization algorithm (ACO) trying to improve the ACO algorithm trying to get better results so we can minimize wire length hence decrease power consumption and increase the efficiency of VLSI design and also follow the VLSI design rules.

2. RE LATE D WORK

Many algorithms tried to solve the VLSI routing problem. Some of these algorithms used the Ant Colony Optimization algorithm to construct Steiner trees: a minimum-weight tree connecting a designated set of vertices, called terminals, in an undirected graph or points in space. Yu hu [6] proposed an ACO approach for building rectilinear Steiner trees using the heuristic approach which requires ants to be connected at each cell and to meet as rapidly as possible. This heuristic 'let ants meet fast' achieves better wire minimization than the luyet's [7] rectilinear Steiner tree algorithm that also uses an ACO approach. The limitation with the Steiner tree approaches is that the Steiner trees are

limited to routing within a single plane, so they are unable to utilize multiple layers that are available for routing on VLSI chips. Also, there is some VLSI routing algorithms using Particle Swarm Optimization (PSO) algorithm. Huang et al. [8] proposed an OAXSMT construction algorithm based on PSO, which is the first to specifically solve the problem of single-layer X-architecture around the Steiner tree problem. PSO has the characteristics of simple execution, few parameters, and fast convergence. Two

union-based genetic operators are applied to the PSO process of Huang, namely crossover and mutation operations, which adjust particle velocity and location and further enhance the search ability. In addition, they also combined some heuristic strategies to further optimize the quality of the global optimal particle Huang et al [9] proposed an algorithm called mlxr, which is based on a lookup table and constructs a 3d obstacle free minimum tree as the basic architecture. An efficient obstacle avoidance technique based on projection is used to accurately capture the correct Steiner point location in a multi-layer environment. Mlxr first builds a 3d obstacle-free minimum tree to connect all pins and constructs two lookup tables based on this obstacle-free minimum tree to quickly provide

information inquiry for the post steps. The 3D obstacle-free minimum tree is then converted into a multi-layer XSMT by means of a lookup table. Finally, the obstacles are handled by two refinement strategies. The experimental results show that compared with the most advanced algorithms, MLXR is excellent in both the total wire length and the running speed. Lu et al. [10] proposed a two-stage transistor routing approach for CMOS standard cells. This two-stage approach synergizes the merits of channel routing and ILP approach. The segment-based ILP makes its router more scalable than a grid-based ILP. Liu et al. [11], [12] combined PSO and ILP to solve the GR problem under X-architecture. They adopted the partitioning strategy to reduce the size of the GR problem, thus contributing to the efficient solution of the ILP model by PSO. Zhang et al. [13] proposed a heuristic algorithm that constructs an extended rectilinear Steiner tree grid as a routing graph, ensuring that the routing graph contains at least one optimal solution for RSMT problem and one near optimal solution OARSMT problem. And by modifying the shortest path heuristic algorithm, a step-growth heuristic algorithm is designed to solve the constrained SMT problem. The precomputation strategy is used to avoid frequent calculation of slew rate. DE algorithm[14] is a global routing algorithm based on the Differential Evolution (DE) technique. It aims at evolving a population of M-dimensional parameter vectors, so-called in- dividuals, towards the global optimum. M stands for the number of parameters. DE algorithm involves four stages, namely initialization, mutation, crossover, and selection. works more efficiently than DPSOM described in [15], ABC, and FLUTE described in [16].

3. PROPOSED ALGORITHM

The main aim of the proposed algorithm is to reduce the wire length that connects the components of VLSI chip so the capacitance decrease that leads to a decrease the power consumption. The proposed algorithm will useAnt Colony Optimization (ACO) algorithm and will try to improve it and decrease its disadvantages. Our goal is to develop a routing algorithm that minimizes the power consumption of the chip. Active power (P) on a chip is determined by the equation.

$$P - aCV^2 f(1)$$

where a is an activity factor, V is voltage, f is frequency and C is capacitance. From this equation we can decrease power consumption by decreasing capacitance. Wires contribute to capacitance and hence power. Thus, the capacitance minimized by our algorithm uses the following equation:

$$C - 2\varepsilon - 16(wirelength)(2)$$

These capacitances are approximations; in reality they will vary according to process size for any particular chip. 'Ant Colony Optimization' provides a multi-agent frame- work for combinatorial optimization problems. This nature- inspired metaheuristic originates from the capability of ants to find the shortest paths from their nest to food sources. Natural ants achieve this goal through constant coordination and indirect communication through a chemical substance called pheromone. This collective problem solving ability results from a reinforcement process in which ants deposit a pheromone trail as they return from food source to their nest. Since ants following the shortest path can complete their trips in less time, they will make more trips between their nests and the food source, and deposit more pheromone on shorter paths compared to longer paths. The strength of pheromone on each path guides the remaining ants to the food sources. In analogy to the biological example, ACO is based on the indirect communication of a colony of simple agents, called artificial ants, mediated by artificial pheromone trails. The pheromone trails in ACO are distributed numerical information used by the ants to provide probabilistic solutions to the problem solved.. Ants continuously modify the pheromone during the algorithm's execution to reflect their search experience so that the strength of pheromone on a route at any time is a good approximation of the goodness of that route in the overall solution. The goal of the ACO algorithm is to minimize capacitance (C) in Eq. 2. This is achieved by having ants find the shortest possible routes and then choose from those routes the one that minimizes capacitance. The ants follow the decision rule that ants meet soon to ensure that ants take the shortest possible route to connect to other cells so that wire length is minimized. In contrast to, when an ant meets another ant, these ants do not die, but rather a particular connection is marked as completed. Completing those paths also reduces

redundant paths. The best solution that minimizes capacitance in Eq. 2 is chosen from the routes of all ants. The following flowchart gives an overview of the basic ACO algorithm.
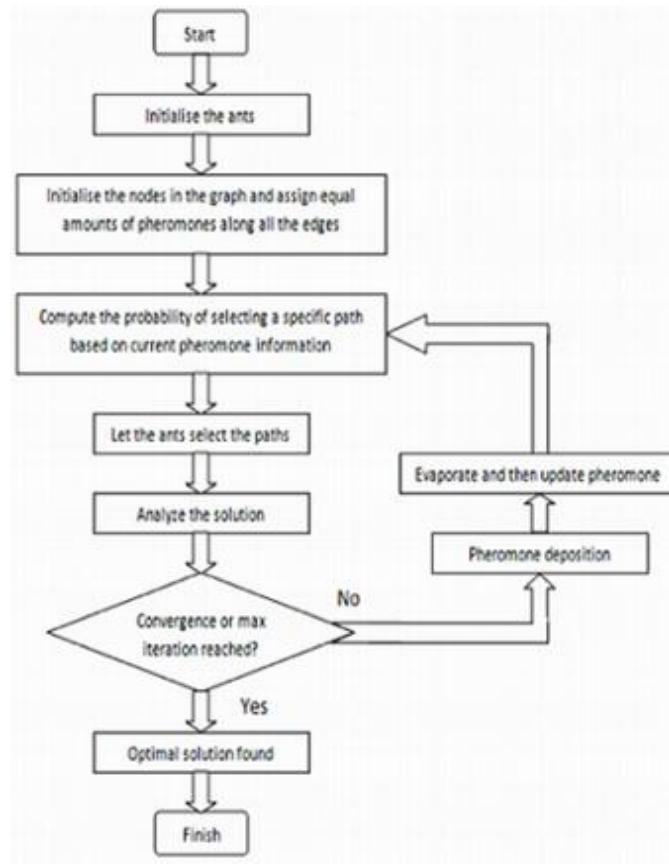
The metaheuristic imitates the food searching behavior of the ants on the basis of pheromone trails left along with the entire space of search of the ants. The various terminologies and steps involved in the Ant Colony Optimization technique are as follows. The decision making in the ACO algorithm greatly affects on the searching behavior of the ant in the algorithm. An ant that reaches node i uses the pheromone trail tij to find the probability of selecting j as the next node.

$$Pi,j = \frac{(\tau i,j)^{\alpha}(\eta i,j)^{\beta}}{\sum (\tau i,j)^{\alpha}(\eta i,j)^{\beta}}$$

where Pi, j is the probability that an ant at node i will move to node j, tau i, j is the amount of pheromone on the path (i, j), eta i, j is the desirability of any path(i, j), alpha denotes the parameter to control the influence of tau i, j and beta denotes the parameter to control the influence of eta i, j. All ants start at terminal nodes. When an ant A meets another ant B, all the intermediate points covered by ant A are added to the route list of ant B, and all the intermediate points covered by ant B are added to the route list of ant A. The paths for ants A and B are marked as completed, which helps reduce the redundant steps taken by ant A to reach the starting point of ant B and vice versa.During routing

ants are not informed about which paths are used by other routes and which are available for routing. This allows ants to find the best possible routing solution for any net. There are cases when ants find a solution that uses a path that is already being used for routing of some other nets. The ACO algorithm calculates the length of the already routed net which

overlaps with yet to be routed net. If the only common point is a non-terminal node, the algorithm compares the length for which both the 'net routes' run without changing direction. In this paper we are trying to improve the Ant Colony algorithm (ACO) algorithm by playing on an important parameter in the ACO routing algorithm which is the decision made by when it reaches at node i then select the next node to move to it. An ant that reaches at node i uses the pheromone trail tij to find the probability of selecting j as the next node. So the probability is the parameter that controls the decision of the ant in the ACO algorithm. Our

proposed will update the probability by which the ant chooses the next node in the ACO algorithm. So the probability will be as follow

$$Pi,j - \frac{(\tau i,j)^\alpha (\eta i,j)^\beta}{\sum (\tau i,j)^\alpha (\eta i,j)^\beta * min((\tau i,:)^\alpha (\eta i,:)^\beta))}$$

The updated probability is the probability of the basic ACO algorithm divided by the minimum of a certain term. This term is the amount of pheromone (tau) values of the paths from point i to all js (j is the next node) multiplied by the desirability (eta) values of the paths from point i to all js (j is the next node). By applying the proposed algorithm using this updated probability the results of the ACO algorithm became better. The results of the proposed algorithm is better than the results of the basic ACO algorithm.

4. EXPERIMENTAL RESULTS AND ANALYSIS

The proposed algorithm is implemented by Matlab code on the Octave program. The efficiency and performance of the Ant Colony Optimization algorithm (ACO) is measured by the cost of the path. The cost of a path in the grid graph is the sum of the costs of edges and the bends' cost (which represent vias) in the grid graph. The best routing algorithm which has the minimum best cost. Tn table.1 the data set that will apply the proposed algorithm on it. We will compare between basic ACO algorithm and the proposed algorithm based on this data set (Table.1). This data set is a group of coordinates of the nodes of the net. These coordinates represent the coordinates of the components of the chip in VLSI design.

TABLE I
POINTS COORDINATES - DATA SET 1

Point no.	1	2	3	4	5	6	7	8	9	10
X	82	91	12	92	63	9	28	55	96	97
Y	66	3	85	94	68	76	75	39	66	17
Point no.	11	12	13	14	15	16	17	18	19	20
X	15	98	96	49	80	14	42	92	80	96
Y	71	3	27	4	9	83	70	32	95	3

Fig.1 illustrates the graph of nodes before applying proposed algorithm on it. Fig.2 illustrates the graph of nodes after applying proposed algorithm on it. Those 2 graphs applied on data set 1 (Table 1)
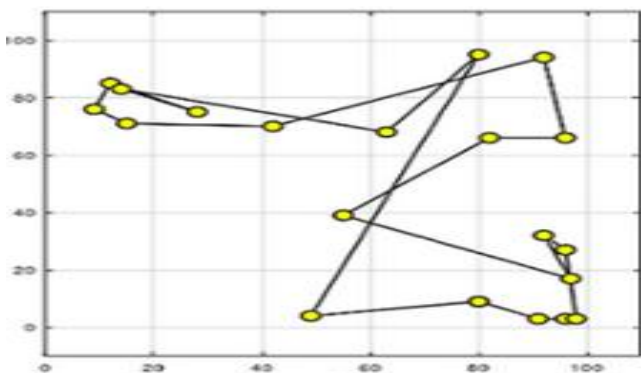

Fig. 1. Graph of data set 1 at the first of applying proposed algo

Fig.3 is a graph between the basic ACO algorithm and the proposed algorithm. In Fig.3 it is illustrated that the y-axis is the best path cost and the x-axis is number of iterations, the blue graph is the proposed algorithm and the red graph is the ACO algorithm. This graph resulted from the data set 1 in Table.1. It is illustrated that the proposed algorithm has minimum best path cost than the basic ACO algorithm so when the path cost becomes smaller this means that wire length that connects the components of chip in

VLSI design will become smaller and the capacitance will be small hence the power consumption will be small so we reached our goal in this paper that we decreased the power consumption.
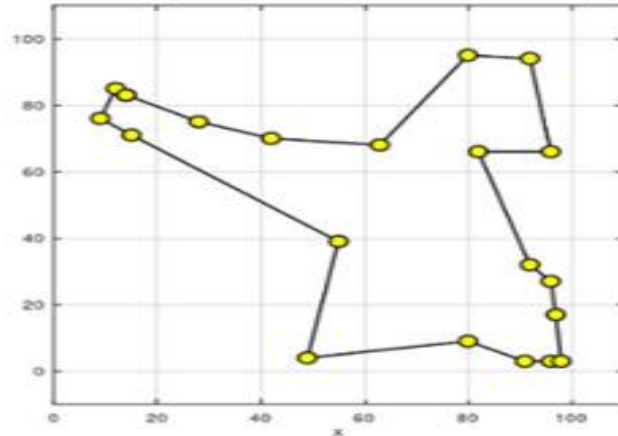

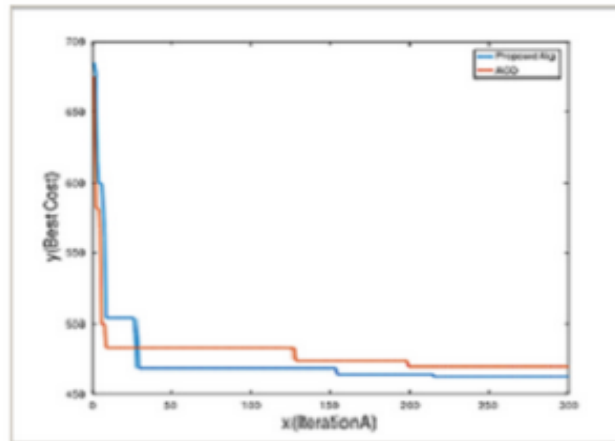Fig. 2. Graph of data set 1 at the end of applying proposed algo

Fig. 3. Proposed alg. vs. ACO alg. in terms of best path cost

As showed in Fig. 3 that the proposed algorithm has better results than the basic ACO algorithm. The best path cost becomes smaller after iteration number 20 in the proposed algorithm graph in Fig. 3. The second comparison will be between the DE algorithm [14]. The comparison will be applied to data set 2 in Table.2. The graph in Fig.4 illustrates the DE algorithm in terms of path cost applied on Data set 2 (Table. 2). These coordinates represent the coordinates of the components of the chip in VLSI design. The graph in Fig.5 illustrates the proposed algorithm in terms of the best path cost applied on Data set 2 (Table. 2). As illustrated in Fig. 4 that the best path cost of the DE algorithm is 317. As illustrated in Fig. 5 that the best path cost of the proposed algorithm is 362 at iteration 300. So the results of the DE algorithm are better than our proposed algorithm because the DE algorithm has a smaller path cost than the proposed algorithm. The DE routing algorithm will lead to smaller power consumption than the proposed algorithm because it resulted in a smaller wire length. The minimum path cost leads to minimum wire length hence small capacitance which leads to smaller power consumption in the chip. The bar chart in Fig.6 illustrates the values of the best path cost of the proposed algorithm and the ACO algorithmand the DE algorithm on data set 2.

TABLE II
POINTS COORDINATES - DATA SET 2

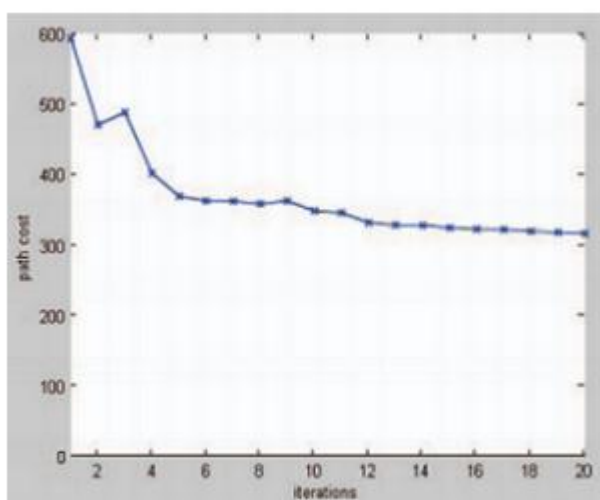| Point no.	1	2	3	4	5	6	7	8	9	10
X	101	36	87	99	20	120	12	66	61	47
Y	49	99	133	111	101	60	56	98	75	29
Point no.	11	12	13	14	15	16	17	18	19	20
X	115	117	111	39	128					
Y	52	139	37	130	147					

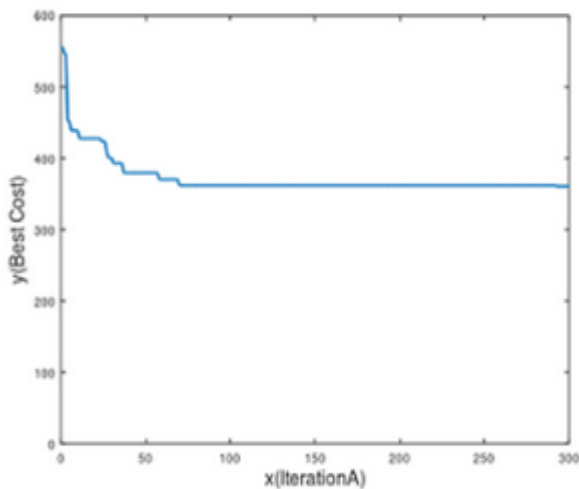Fig. 4. DE algorithm in terms of values of path cost

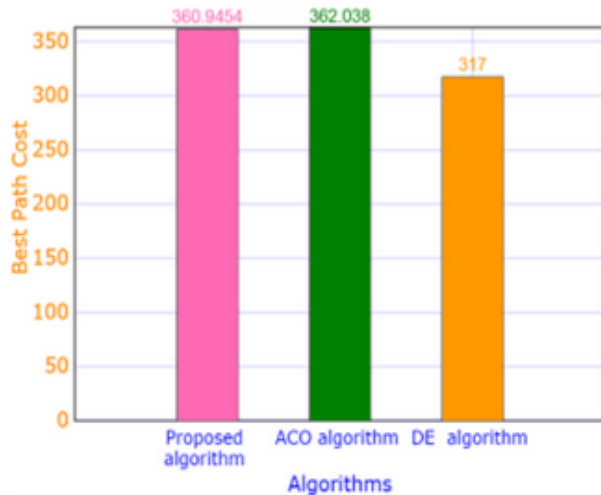
Fig. 5. Proposed alg. in terms of best path cost

Fig. 6. Proposed alg. vs. ACO. vs. DE in terms of best path cost

CONCLUTION AND FU TU RE W OR K

In this paper a new improved Ant Colony Optimization (ACO) algorithm for VLSI global routing algorithm proposed to improve the ACO algorithm by getting smaller best path cost. The smaller path cost means smaller wire length connected between the components of the chip, the small wire length leads to smaller capacitance hence smaller power consumption. As power consumption decrease the efficiency of the VSLI design becomes better. By applying and deploying the proposed algorithm it is possible to enhance and improve the process of global routing in VLSI design. Our experimental results and analysis show that the proposed algorithm is more efficient than the ACO algorithm. From the previous comparisons and results analysis, we observe that our proposed algorithm is better than the ACO algorithm in decreasing the value of the best path cost and this is a great achievement. But we found that the proposed algorithm is not the most efficient global routing algorithm but there are some routing algorithms that gives better results than the proposed algorithm like the DE algorithm. We found that the DE algorithm [14] is better than the proposed algorithm in terms of decreasing the path cost. So the better VLSI routing algorithm which have minimum path cost so it leads to smaller power consumption the chip. Our future work is to

try in decreasing the path cost more and more and decreasing the execution time of the routing algorithm.

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