An Energy Dissipation and Cell Optimization of Vedic Multiplier Topologies for Nanocomputing Applications

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Abstract: Quantum-dot cellular automata is a cutting edge enumeration methodology that suggests less area and high speed compare CMOS methodology. The CMOS circuitry having issues related to short channel and device density so QCA is better and powerful alternative to reduce the area as well as increase the speed of the circuitry. QCA could be a modern computing innovation that's made of quantum cell containing two electrons and dots. A multiplier is a vital part of Digital Signal Processing (DSP) and many more digital circuits applications. We emphasize Vedic multiplier topologies structures agreeing to Vedic science from old Indian figures. In this article, we suggested a efficient, less complex Vedic 2×2 and 4×4 multipliers topologies using proposed ultra efficient Half Adder (HA), Full Adder (FA) topologies in QCADesigner simulation environment for less energy and fast speed for nano computing application. The simulation waveform suggests an architecture outstrip in comparison to the parameters of cell count, area, latency related to past QCA layouts. The proposed QCA 2×2 Vedic multiplier design shown 37.62% improvement in QCA cell count and 4×4 Vedic multiplier design shown 71.72% improvement in cell counts as well as 29.62% area is decreased for 2×2 QCA Vedic multiplier and 43.38% area decreased from 4× 4 QCA Vedic multiplier as related to its best existing designs.

Keywords:QCA, DSP, Vedic Multiplier, nano scale

1. Introduction

Quantum Dot Cellular Automata (QCA) recommends higher densecircuitry, low power consumption and quick switching speed architecture. Traditional CMOS has abounded our manufacture in afterward a long time and illustrate to be a better alternate than previousmechanizationapproach. Quantum computing, atomic computing and nano computation are few developmental nanotechnologies executeddepends on Coulomb repulsion. Now a days circuit design researchers are driving towards a progress onenforcingscience, reliant on electron polarization is called as QCA, thatpresentsadvantageousoutcome regarding the reduction and the cost function of the excessive lessboundary.

QCA-based layouts are best for the boundaries of density (1012 device/cm2), frequency or speed (range of terahertz), energy dissipation (100 W/cm^2). This paper mainly emphasized in the design of 2×2 and 4×4 Vedic QCA multipliers suggested using an efficient and less complex QCA half adder, QCA full adder as a multiplier is a basic element which is proficient in terms of area, quantum cost and latency. Earlier array multipliers have been broadly examined using the QCA simulation environment. Be that as it may, there are also numerical functions utilizing the Vedic methodology which are exceptionally quick and desire less hardware structure. This will be utilized to progress the computing speedy processors. A tremendous adders count is utilized to achieve partial product summation for greater order multipliers. This methodology of Vedic multipliers governed by 16 Vedic sutras and explained the easy action of determining all mathematical issues.

1.1 Contributions in The Paper

- The most commitments of the article are as-
- Designing an ultra efficient XOR gate QCA layout.
- Designing an efficient Half Adder (HA) QCA layout.
- Design of QCA Full Adder (FA) topologies.
- Design of an efficient QCA Ripple Carry Adder (RCA) topologies.
- Designing of cost efficient QCA 2×2 and 4×4 and 8×8 Vedic Multipliers topologies and design extended up to n×n Vedic Multiplier using conventional formula we find the majority gate calculation and number of inverters used.
- The suggested architectures are comparing a summarized according to the cell count, area occupied, latency, and the cost that asserts the recommended plans having less area and more way better quantum cost associated with its previous designs.

1.2 The Paper Alingment

The paper is summarized as Section-II explained the QCA terminology. Section-3 allocate by Proposed QCA layouts of XOR gate topologies, QCA half adder (HA), QCA full adder (FA) topologies, and QCA Vedic 2×2 Multiplier topologies and QCA RCA topologies, followed by Section-4 explained QCA 4×4 Vedic Multiplier topologies. Further the design is extended up to n×n Vedic Multipliers explained in Section-5. Section-6 shows the conventional calculation of majority gate and inverter counts in a n×n Vedic Multipliers. Section-7 encircle simulation outcome of all planned QCA architectures. Section-8 deals the energy dissipation and kink energy evaluation of suggested architectures and performance comparison of various multipliers and at last, in Section-9 we conclude the work.

2. Quantum Dot Cellular Automata Terminology

QCA is an arrangement of action of quantum cells. The cell has broadcast info electrostatically by neighboring cells. The cell is elaborated with a twin electrons in a cubicle. Columbia's revulsion of the electrons to include the dots in a QCA cell thattakes over the undermost energy category of the circuits.

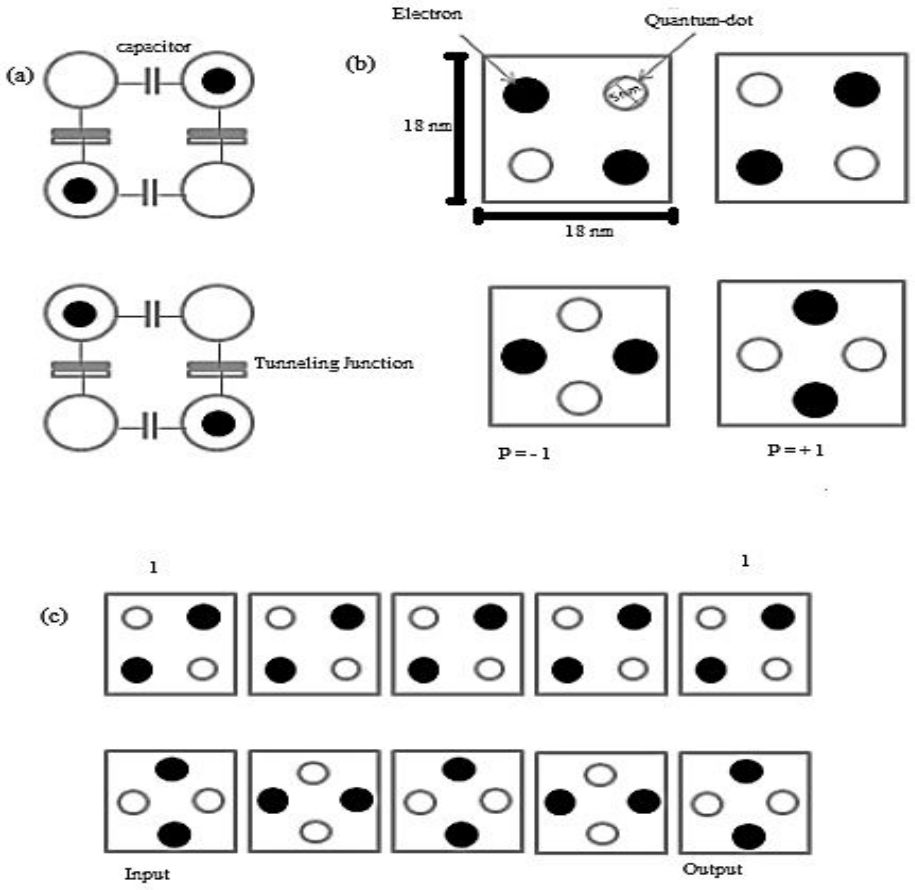
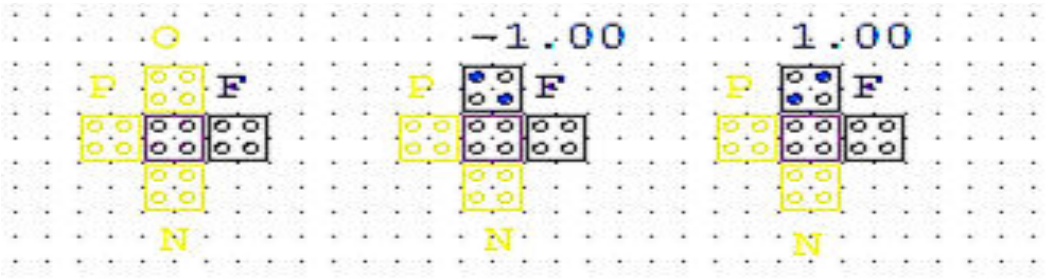


Figure 1. QCA Cells, Patterns (a) Functional diagram (b) Cells Polarization (c) QCA wire

2.1. Majority Gate

Majority gate is a combination of 5 cells in such a way that 2 cells are input 1 is polarization cell 1 is normal cell and 1 output cells are used in majority gate. It plays a crucial part in QCA computing presented in Fig.2.



(a) Majority Gate (b) QCA AND Gate (c) QCA OR Gate

Figure1. Basic QCA Logic Gates Architecture

2.2 Clocking in QCA

At QCA-cell, the meta-stable phase-run parallels the polarization, cells that will not be characteristically unsurprising as logic 1 or logic 0 that contain 4 phases:

- Switch: un-polarized cells determined by some inputs and get polarized subordinate on its acquaintance polarization,
- Control: cells enclosed within the equivalent binary phase, so it may spreadlike the input to the various cells,
- Release: obstructionisheldunderneath and cells remains un-polarized and
- Relax: cell un-polarized.

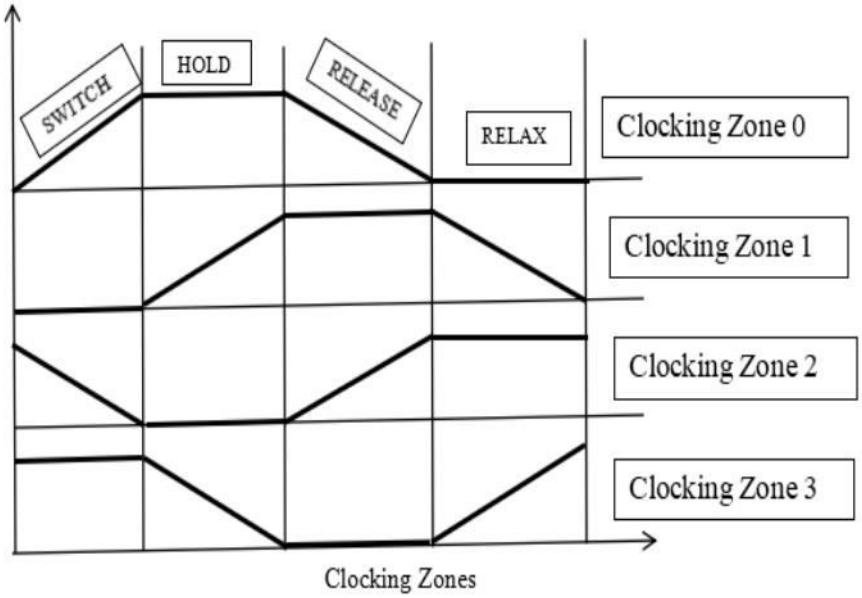
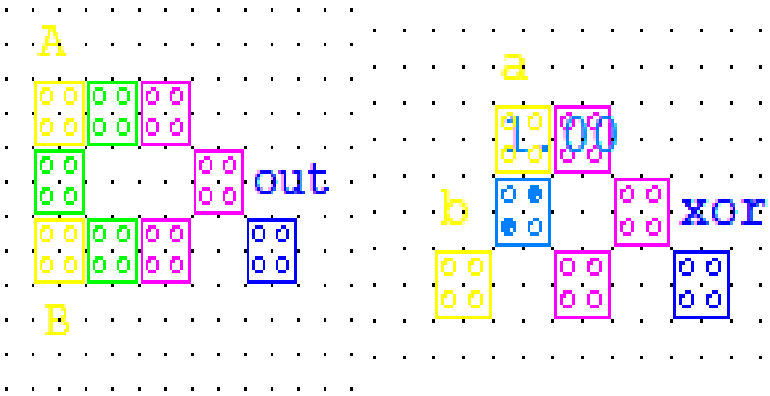


Figure2. QCA Clock concept

3. Proposed QCA Logic Circuit Architectures

3.1 The Proposed QCA XOR Gate Design

The following section provides an idea about a digital logic circuitry named as XOR gate. In literature, various QCA designers create XOR gates that are mentioned (Bahar A.N., 2018). This part explained an optimal and cost efficient QCA layout 2-input XOR gate topologies.



(a) N9 (b) N7

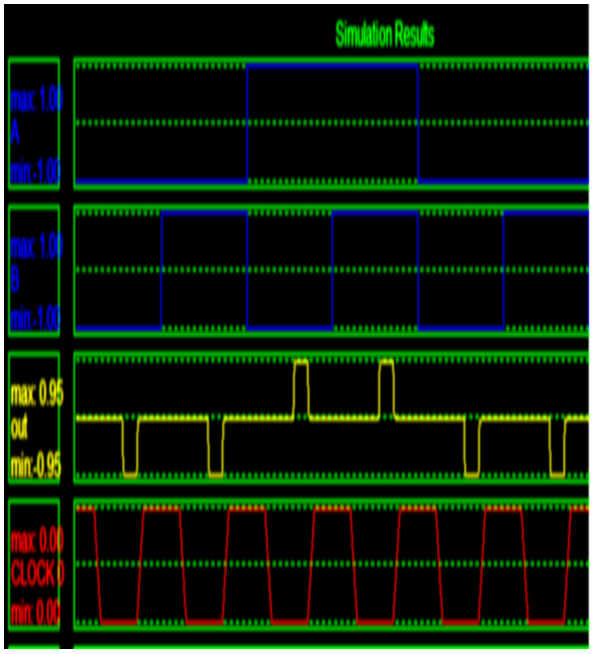


Figure4. QCA XOR Gate (a) Proposed-1 (N9) Layout (b) Proposed-2 (N7) Layout (c) Simulation Waveform

The suggested design is ultra-efficient in comparison to past design. The QCA architectures of XOR gate are displayed in fig. 4.

3.2 The Proposed QCA Half Adder

An adder is a base of each modern IC and ALU, in electronics that execute accumulation of binary numbers. The proficient suggested QCA Half Adder is displayed in Fig.5. Suppose A and B are 2 binary numbers so sum and carry may be estimated by given formula,

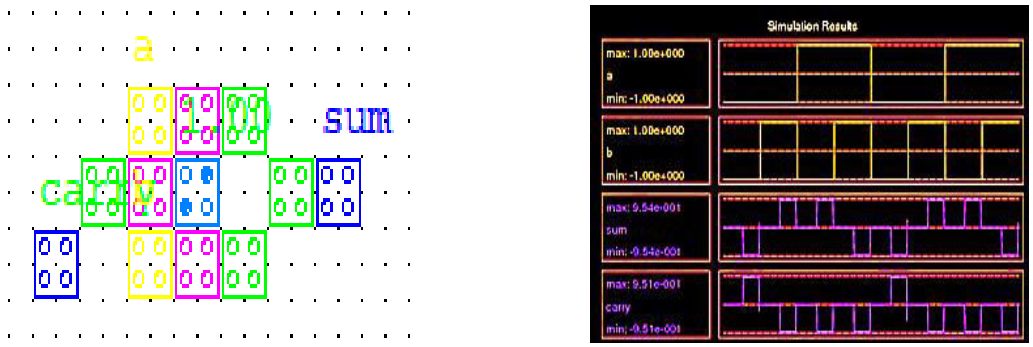
Lemma 1.

carry = AB

Sum = $Maj.(\overline{Maj.(A,B,0)}, Maj.(A,B,1),1)$

Proof.

Sum = $\overline{(A\bar{B}+\bar{A}B)} = (\overline{AB})+(A+B) = maj.(\overline{maj.(A,B,0)},\ m(A,B,1)1)$ (2)



(a) N(12) (b)

Figure5. Proposed QCA Half Adder (N12) (a) Layout (b) Sımulation Waveform

3.3 The Proposed QCA 2× 2 Vedic Multiplier

The Vedic Multiplier is established on Urdhva-Tiryakbhyam that can be used for binary as well as decimal multiplication (Pooja, 2018). A Vedic multiplication gives bitwise multiplication and gives product and column wise additions. The most common performance of Vedic multipliers is that we are able to calculate partial products and sums that must be satisfied at the same time. It is simple to clarify the methods of multiplying 2*2 bit all steps are

1. Firstly A0 and B0 will be multiplied takes 1 AND gate. The primary initiative is the cross multiplication A and B and implies 2 AND gates and output is S0 i.e. S0=A0.B0
2. The A's LSB is multiplied with the B's MSB and B0 and the A's MSB is multiplied with the B's LSB and further those products will be summed by half adder and generates output i.e. C1S1=A1B0+A0B1
3. The A's MSB is multiplied by the B's MSB i.e. (A1× B1) and summed to the previous carry C1 using second HA and final product i.e. C2S2= C1 + A1B1
4. Lastly, the 4-bit output C2S2S1S0 comes after 2 ×2 binary numbers multiplied.

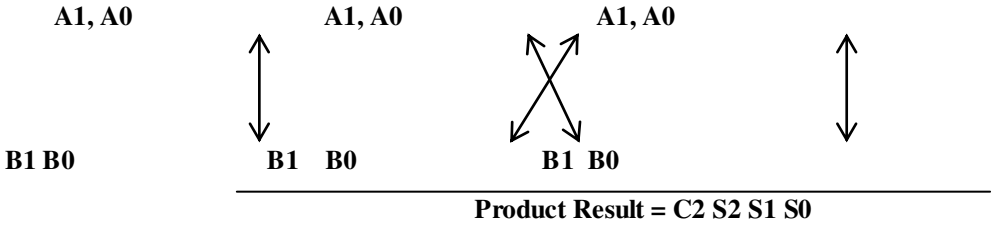
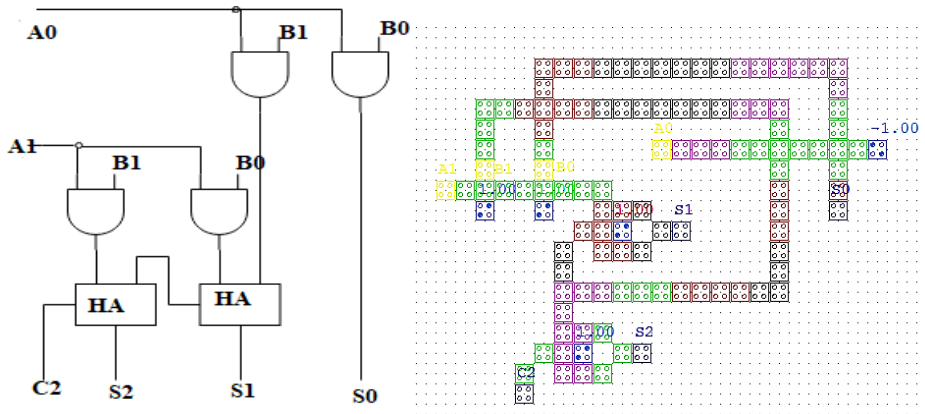
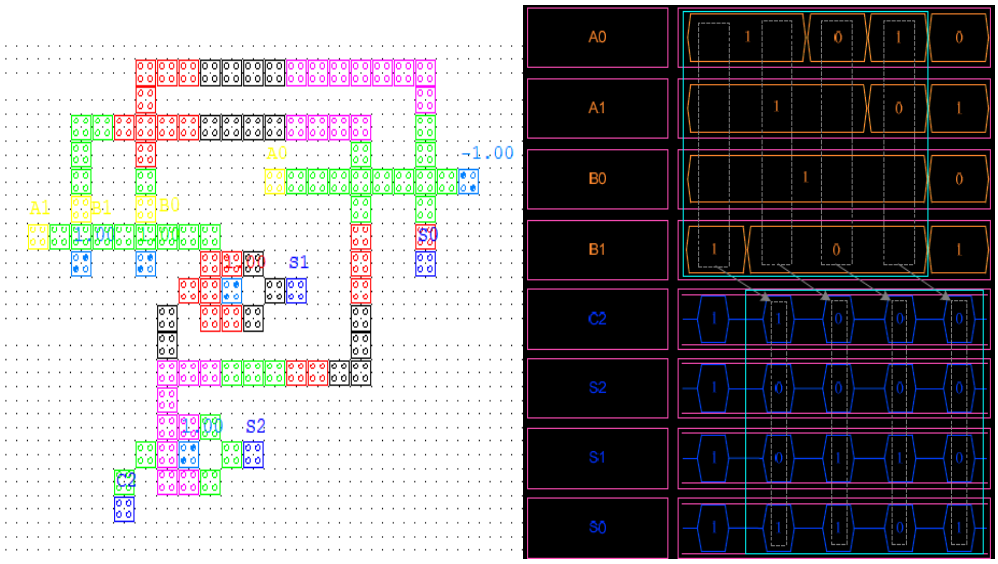


Figure 6. Step by Step Multiplication of 2×2 bit



(a) (b) N(119)



(c) N(105) (d)

Figure7.2×2 Vedic Multiplier (a) Conventional Block Structure (b) Proposed-1 QCA layout (N119) (c) Proposed-2 QCA layout (N105) (d) Simulation wave form of a proposed 2×2 (2-bit) Vedic Multiplier

The proposed QCA 2-bit(2×2) Vedic multiplier topologies contain 119 quantum cells and $0.17\mu m^2$ area 105 quantum cells and $0.14\mu m^2$ area and which is the lowest as related to the previous existing designs.

3.4The Proposed QCA Full Adder Topologies

A full adder is a combinatorial circuitry which executes the summation of 3- input bits: A, B and input carry is Cin, from a preceding addition and it generates the equivalent sum 'Sum' and 'Carry' as output as displayed in Fig.8.

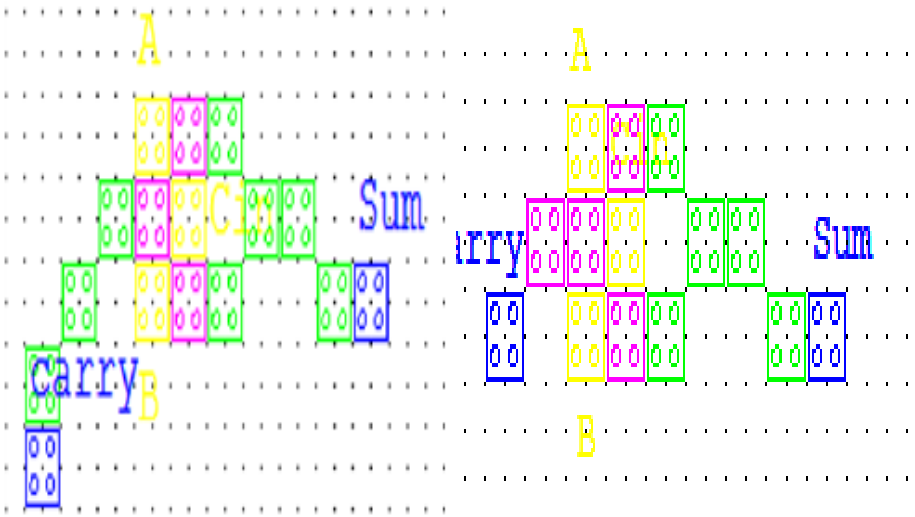
Lemma1.

Maj.(A,B, $\overline{maj.(A,B,C)}$) = Maj.(A,B,$\bar{C}$)

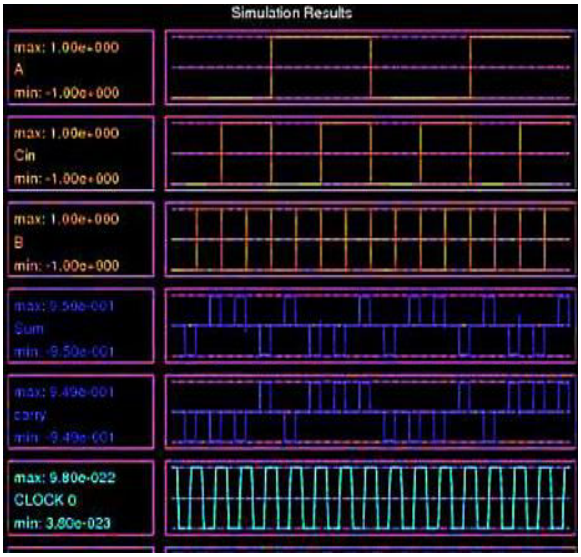
Proof.

Maj(A,B, Maj.($\overline{maj.(A,B,C)}$) = AB + A($\overline{AB}$ + $\overline{BC}$ + $\overline{CA}$) + B($\overline{AB}$ + $\overline{BC}$ + $\overline{CA}$) = AB + A$\overline{BC}$ + $\overline{AB}\overline{C}$

$= A(B + \bar{B}\bar{C}) + B(A + \bar{A}\bar{C}) = A(B + \bar{C}) + B(A + \bar{C})$ = Maj.(A, B, C) (3)



(a) Proposed Design-1 N (16) (b) Proposed Design-2 N(14)

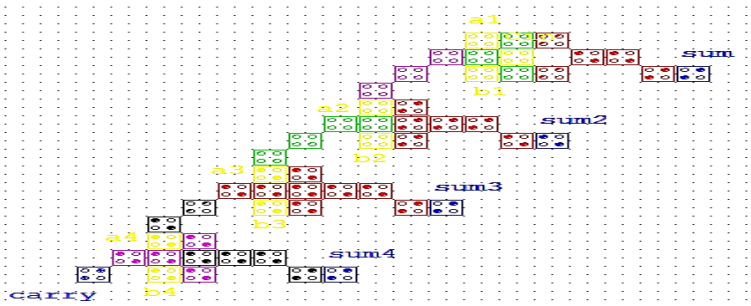


(c)

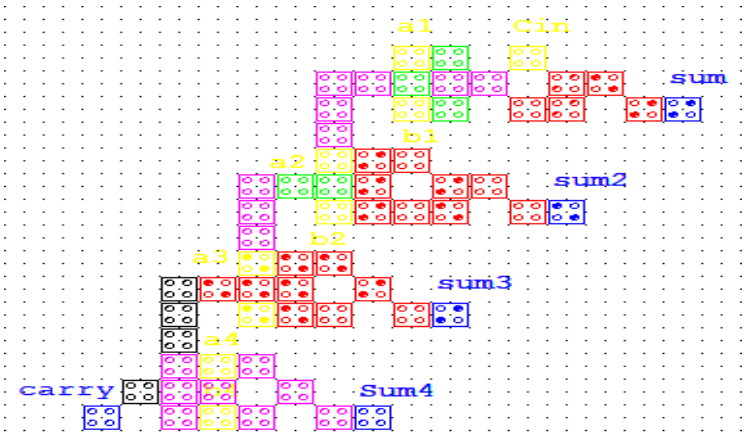
Figure8.QCA Full Adder (a) Proposed design-1 layout N(16) (b) Proposed design-2 layout N14 (c) Simulation Waveform

3.5The Proposed QCA Ripple Carry Adder Topologies

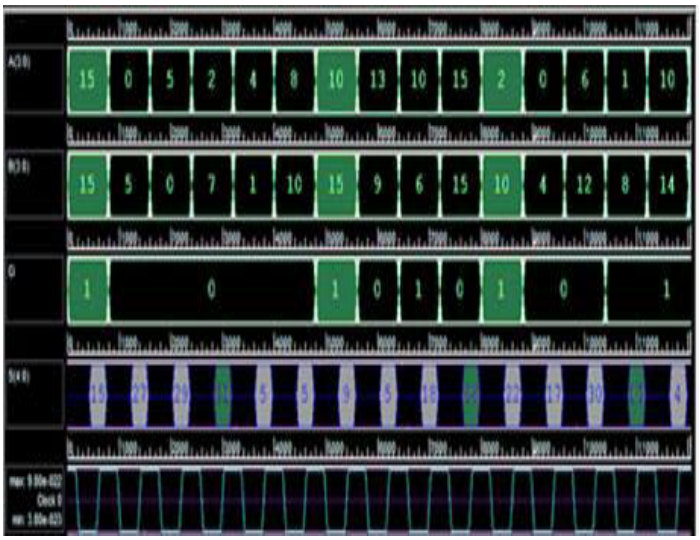
A 4-bit RCA adder formed via cascading 4-full adders to from a carry route in RCA (Maharaja,J, 2020). The planned 4-bit RCA QCA layout offered in fig. 11. In this work the optimal structure of RCA will be proposed using compact and robust 1-bit full adders for designing of RCA. The proposed 4- bit RCA contains 50 cell count and 0.14µm2 area and 47 cell count and 0.11µm2 which is optimized as compare to preceding RCA designs.



(a) Proposed design-1 N(50)



(b) Proposed design-2 N(47)



(c)

Figure 9. QCA Ripple Carry Adder (a) Proposed design-1 N(50) (b) Proposed design-2 N(47) (c) Simulation Waveform

4.The Proposed 4×4 Vedic Multiplier Topologies

4.1. The Proposed 4×4 Vedic Multiplier Topologies using proposed Full Adder Topology

The 4×4 Vedic Multiplier is simple to clarify the methods of multiplying 4×4 bits. The four binary numbers A1A0, B1B0, A3A2, B1B0, A2A0, B3B2, A3A2, B3B2 are taken for multiplication. An old frame of science is Vedic Calculations. There are 16 Vedic rules for scientific division. UT truly implies "Vertically and crosswise" (Babie,S.,2019) The suggested architecture is explained in Fig. 12 and Fig 13. The 4×4 Vedic multiplier contains a proposed QCA 4-bit with 2×2 Vedic Multiplier. The step used in multiplication is enclosed below-

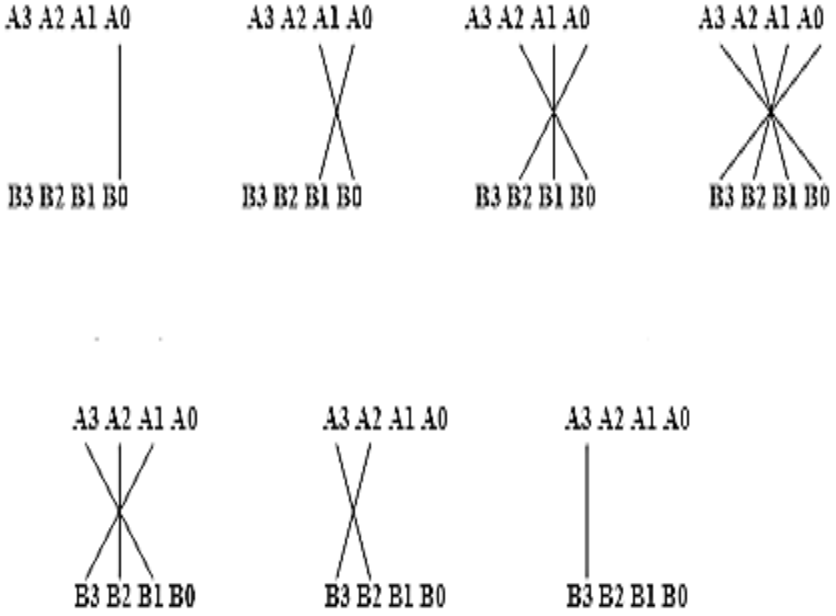


Figure10. Steps for 4-bit Vedic Multiplier

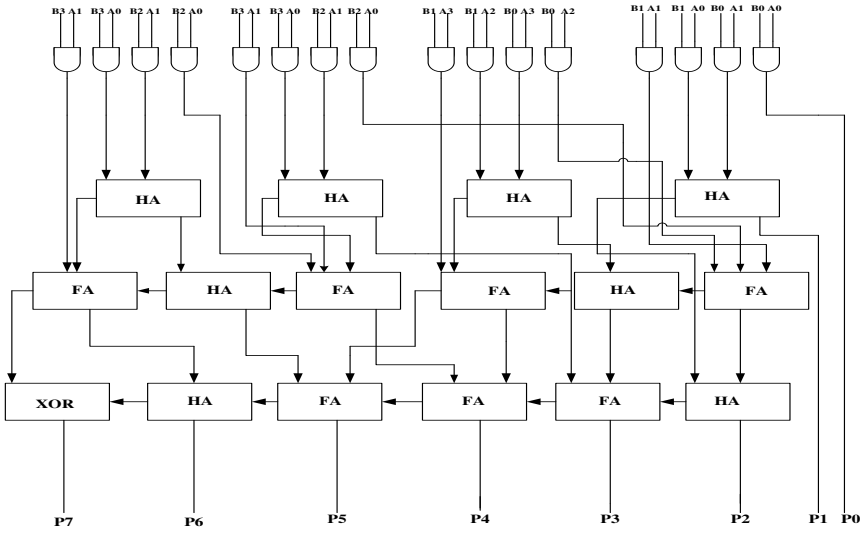


Figure11.Conventional block structure of 4-bit Vedic Multiplier

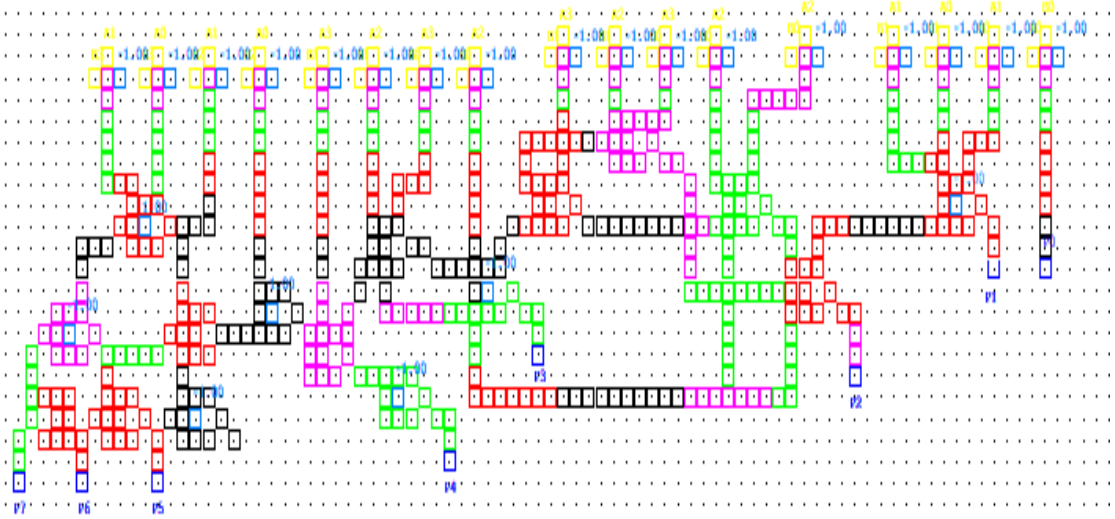


Figure12. Proposed QCA 4-bit Vedic Multiplier design-1 based on FA(N16)

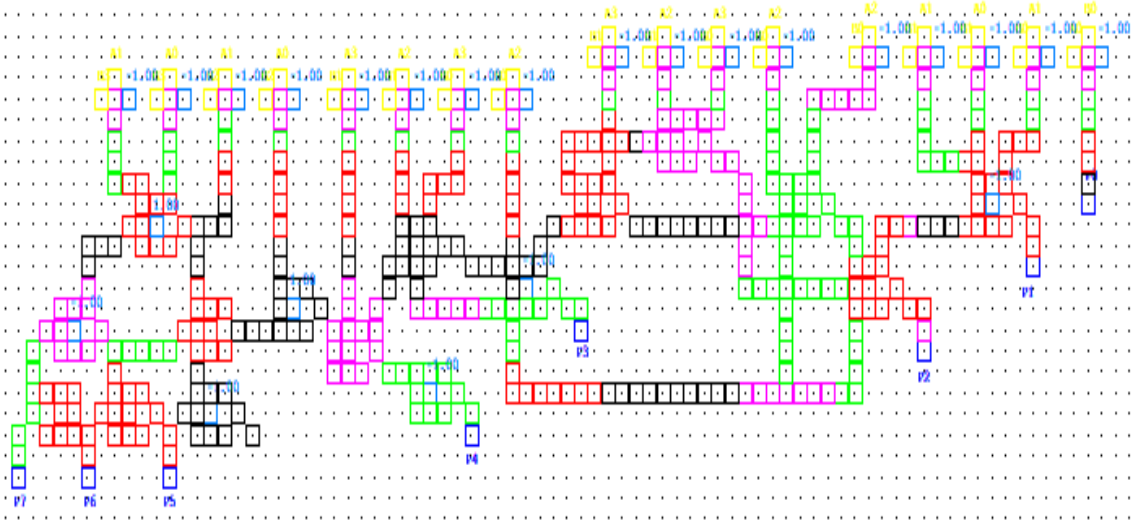


Figure13. Proposed QCA 4-bit Vedic Multiplier design-2 based on FA(N14)

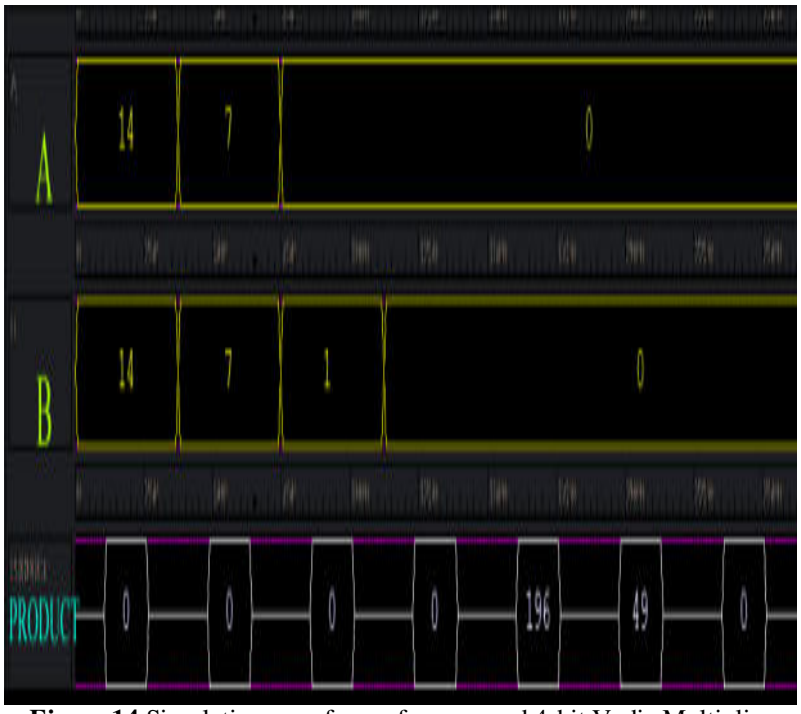


Figure.14. Simulation waveform of a proposed 4-bit Vedic Multiplier

4.2 The Proposed 4×4 Vedic Multipler Topologies using proposed RCA Topology

The 4×4 Vedic Multiplier contains a proposed QCA 4-bit RCA with 2-bit Vedic Multiplier. The conventional plan of 4-bit Vedic Multiplier is presented in Fig.15 and suggested QCA design in 4-bit Vedic Multiplier having 1234 QCA cells count and 2.44 μm^2 area as presented in fig. 12.

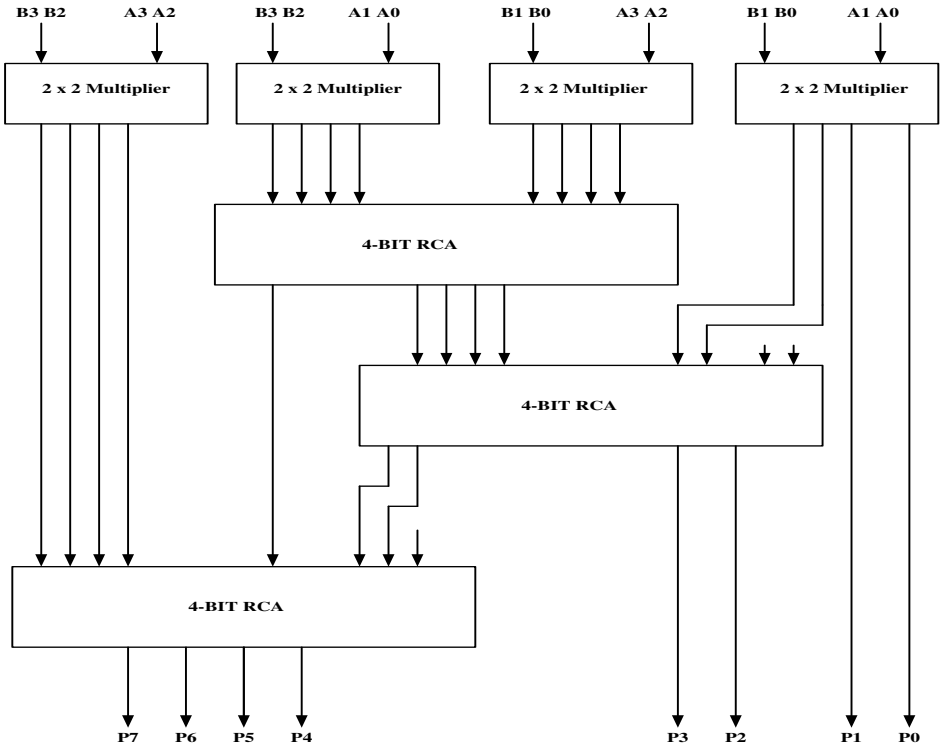


Figure 15 Conventional Block Structure of QCA 4-bit Vedic Multiplier using RCA

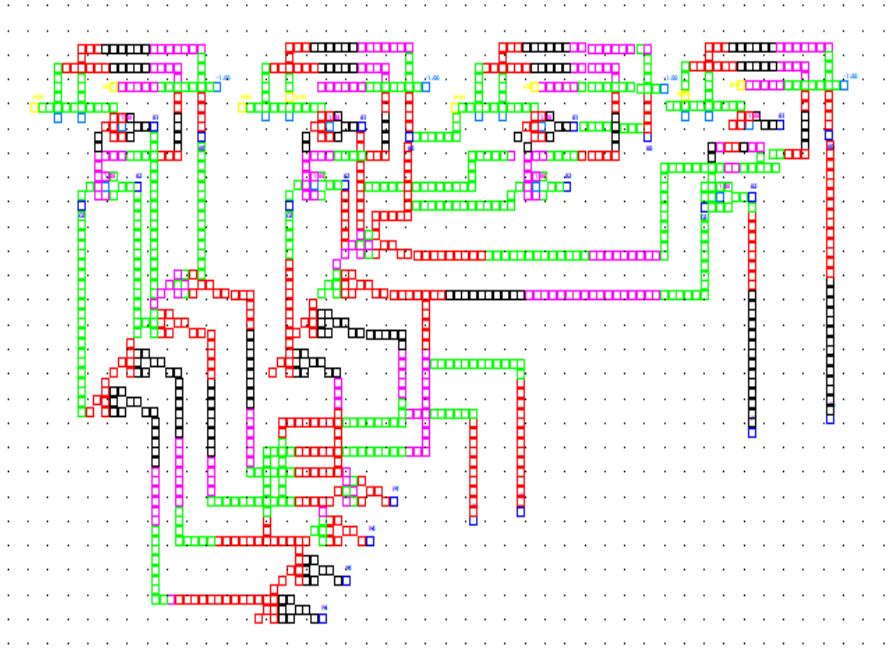


Figure 16. Proposed QCA design-1 of 4-bit Vedic Multiplier using RCA PD-1(N50)

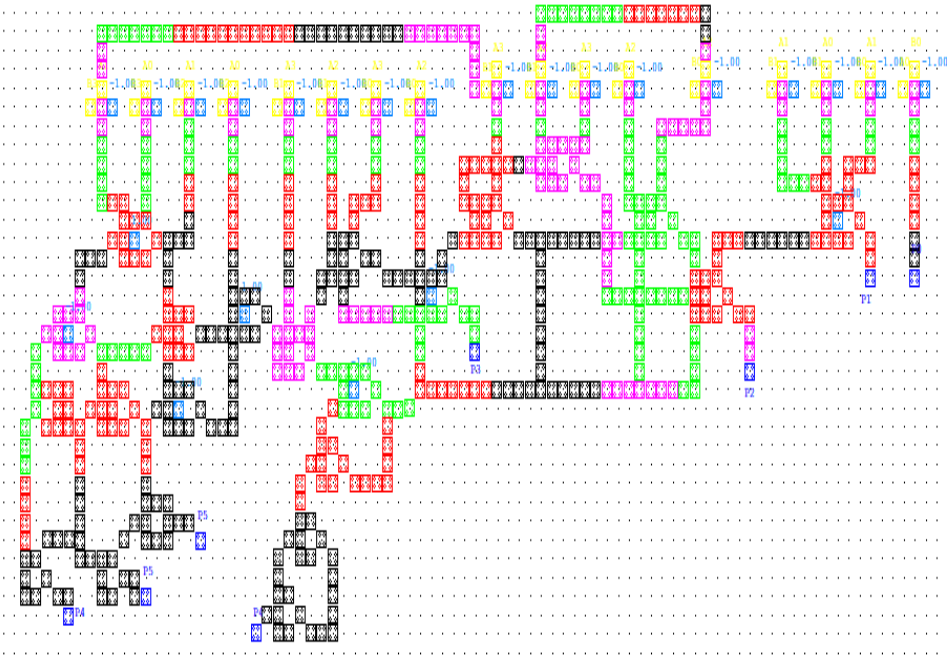


Figure. 17. Proposed QCA design-2 of 4-bit Vedic Multiplier using RCA PD-2(N47)

5. The Proposed 8-bit Vedic Multiplier Architecture

The previous 8-bit multiplier consists of 4-bit multipliers (four numbers) and 8-bit RCA(three numbers). The drawback of RCA is that, to produce the output it has to hold for the earlier carry. In the suggested 8 ×8 Vedic multiplier, there are four proposed 4 ×4 Vedic multipliers. The outcome of four 4-bit Multiplier is summed by recovering the main 8-bit RCA of previous multiplier having 8-bit FA. The 8-bit RCA is placed in the planned design by the 3-bit RCA to produce the final result, so that latency and area will reduce as depicted in Fig.18. The suggested 8× 8 Vedic Multiplier using RCA to contain 2250 numbers of cells and 3.49 μm^2 area occupied.

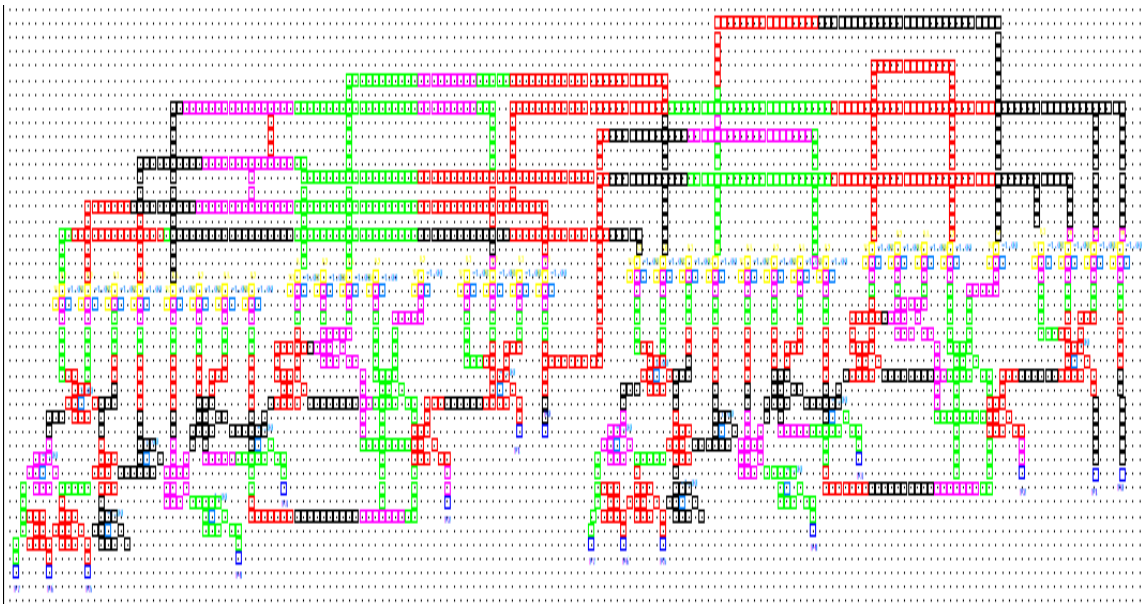


Figure18. Proposed QCA Layout of 8-bit Vedic Multiplier using RCA

6. Proposed Conventional Formula for n× n Vedic Multiplier Architecture

The suggested basic architecture of n-bit Vedic Multipliers are obtained by the planned 8 ×8 Vedic Multiplier. The n-bit Vedic Multiplier containing n/2-multipliers (four numbers), n-bit RCA(one number), n-bit FA (one number), and (n/2 −1) bit RCA(one number). Similarly for executing 16 ×16 Vedic Multiplier using a conventional formula that consists 8 ×8 multipliers (four numbers), 16-bit RCA(one number), 16-bit FA(one number) and 7-bit RCA (one number). The various modules in multiplier presents conventional formula for the parameters like majority gates count and inverters used etc. [24]. In 4×4 Vedic multiplier contains full adders (seven numbers),half adder (nine numbers) and And gate(16 numbers). Every adder contains 2 majority gate and 1 inverter respectively.

6.1. Conventional formula for Majority Gate Calculation

The calculation of the absolute number of majority gate in 4×4 Vedic Multiplier is
Maj.(4×4) = [(7FA×2) + (9HA×2) + (16 AND×1)] = 48 MG

The calculation of the absolute count of MG (majority Gate) in 8-bit Vedic Multiplier is

$$\text{Maj}(8\times8)= [4 \times (\text{Absolute count of Maj in } 4\times4 \text{ multiplier})] + [(8\text{-bit FA} + 8\text{-bit RCA} + 3\text{-bit HA}) \times 3]$$

$$=[4 \times 48] + [19 \times 3]$$

$$=249$$

Now, the calculation of the absolute number of majority gate in n-bit Vedic Multiplier is

$$\text{Maj.}(n \times n) = [4 \times (\text{Absolute count of Maj. in } n/2 \times n/2)] + [3 \times (n + n + \frac{n}{2} - 1)]$$

$$= [4 \times (\text{Maj.}\, n/2 \times n/2)] + [3 \times (\frac{5n}{2} - 1)] \qquad (4)$$

6.2. Conventional formula for Inverter Calculation

The calculation of the absolute count of the inverters count in 4-bit Vedic Multiplier is
Inv.(4×4) = [total no. of FA × 1] + [total no. of HA × 1] =[7×1] + [9×1]=16

The calculation of the absolute count of inverters counts in 8-bit Vedic Multiplier is

$$\text{Inv.}(8\times8) = [4 \times (\text{Inv.}(4\times4))] + [(8\text{FA} + 8\text{RCA} + 3\text{HA}) \times 1]$$

$$=[4\times16] + [19\times1] = 83$$

Now, the calculation of the absolute count of inverter count in n-bit Vedic Multiplier is

$$\text{Inv.}(n\times n) = [4 \times \text{Inv.}(\tfrac{n}{2} \times \tfrac{n}{2})] + \left(\tfrac{5n}{2} - 1\right) (5)$$

So as per the above formulation and conventional expression the n-bit Vedic Multiplier proposed structure is as presented in Fig.19.

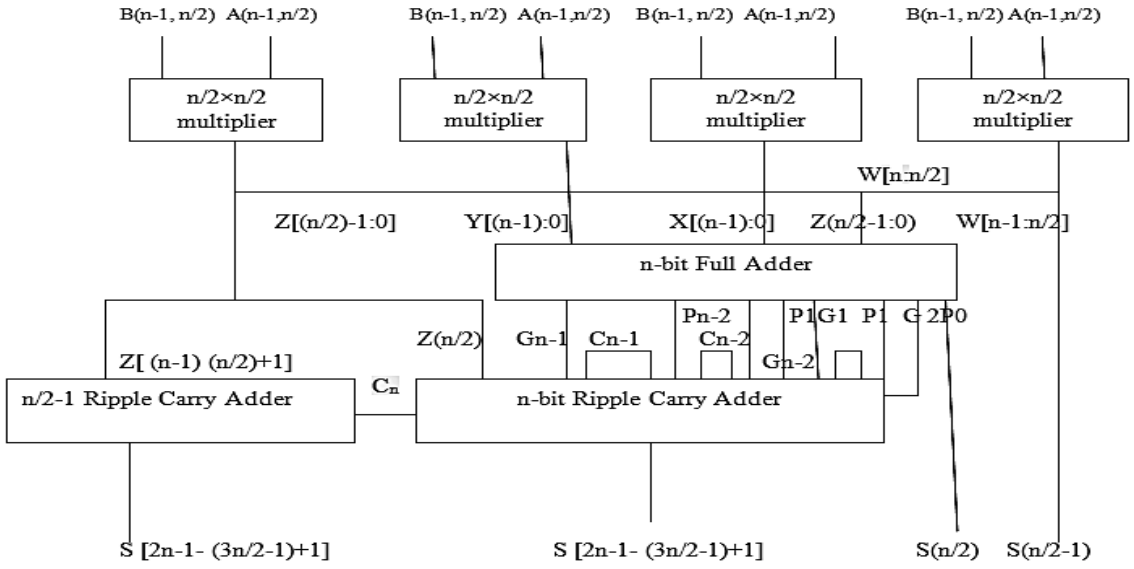


Figure19. The conventional structure of the n-bit Vedic Multiplier

7. Simulation Result and Discussion

QCA are utilized for simulation of recommended QCA layouts. The suggested technique used an optimization of the QCA layout having better competency associated with the past existing design. The comparison table appears that the planned layouts have picked up less QCA cells, area and are more competent within the parameters of the latency and quantum cost associated with its previous designs.

The suggested QCA architectures have very less cells as associated to its existing past counterpart. The suggested QCA XOR gate topology contains 9 and 7 QCA cells comparison shown in Table-1,QCA half adder contains 14 numbers of as shown in Table-2, QCA, 2×2 Vedic Multiplier contains 119 QCA cells as shown in Table-3, QCA Full Adder 16 number of cells as presented in Tables-4, QCA RCA holds 50 quantum cells as displayed in Table-5, QCA 4×4 Vedic Multiplier 488 numbers of QCA cells are used as displayed in Table-6.

Table-1. Performance Parameter Analogy of QCA XOR Design

QCA XOR Gate	Cell	Area (μm^2)	Latency (Clocking cycles)	Quantum Cost (Area * Latency)
Niemer. M.T.2004	60	0.011	1.5	0.016
Mustafa M. 2013	51	0.092	2.0	0.184
Singh. G. 2016	29	0.041	0.25	0.010
Bahar A.N.2018	12	0.021	0.05	0.001
Tripathi.D.2020	14	0.034	0.50	0.017
Proposed-1(N9)	9	0.018	0.25	0.004
Proposed-2 N(7)	7	0.014	0.25	0.003

As per table-1 the proposed QCA XOR gate contains 9 and 7 number of cells and occupied area 0.018μm^2 and 0.014μm^2which is smallest in comparison with all existing designs.

Table 2. Performance Parameter Analogy of QCA Half adder Design

QCA Half Adder	Cell	Area (µm2)	Latency (Clocking cycles)	Quantum Cost (Area* Latency)
Fengbin D. 2017	48	0.37	0.50	0.185
Proposed (N12)	12	0.02	0.25	0.005

As per table-2 the proposed QCA Half Adder gate contains 12 number of cells and occupied area 0.02μm^2 which is smallest in comparison with all existing designs.

Table 3. Performance Parameter Analogy of QCA 2×2 Vedic Multiplier Design Topology

QCA Vedic Multiplier	Cell	Area (µm2)	Latency (Clocking cycles)	Quantum Cost (Area* Latency)
Pooja V.G. 2018	291	2.39	3.00	7.17
ReddyBNK 2020	194	0.27	2.25	0.60
Proposed-1	119	0.17	2.00	0.34
Proposed-2	105	0.14	2.00	0.28

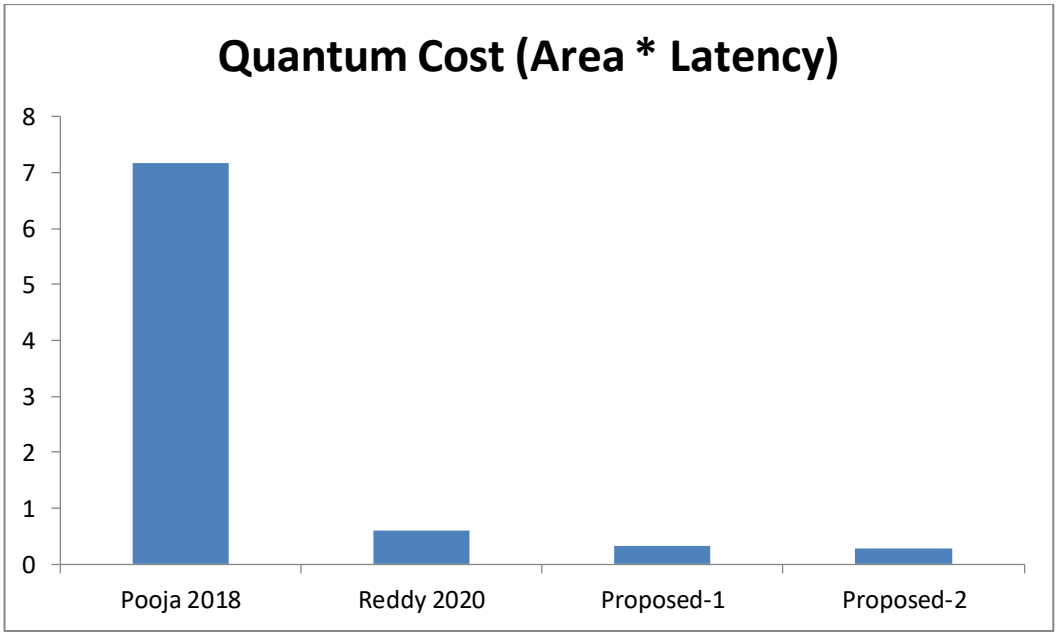


Figure.20. Quantum Cost analysis of variousQCA 2×2 Vedic multiplier topology

As per table-3 the proposed 2×2 Vedic Multiplier Design topology contains 119 and 105 number of cells and occupied area 0.17μm^2 and 0.14μm^2which is smallest in comparison with all existing designs.

Table 4. Performance Parameter Analogy of QCA Full Adder Topology

QCA Full Adder	Cell	Area (μm2)	Latency (Clocking Cycle)	Quantum Cost (Area * Latency)
Sasamal T.N.2018	40	0.030	0.50	0.015
Abedi D.2015	59	0.043	1.00	0.043
Zahmatkesh M. 2018	37	0.024	1.00	0.024
Rashidi h. 2017	33	0.030	0.50	0.015
Babaie S. 2019	44	0.035	0.50	0.017
Proposed-1	16	0.030	0.25	0.005
Proposed-2	14	0.270	0.25	0.067

As per table-4 the proposed full adder topology contains 16 and 14 number of cells and occupied area $0.03\mu m^2$ and $0.27\mu m^2$which is smallest as associated with all previous designs. The cost analysis of the proposed variousQCA 2×2 Vedic multiplier topology is mentioned in Fig.20

Table 5. Performance Parameter Analogy of QCA RCA

QCA RCA	Cell	Area (μm^2)	Latency (Clocking Cycle)	Quantum Cost (Area*Latency)
Sasamal T.N.2018	212	0.194	0.50	0.97
Labrado C. 2016	295	0.313	1.50	0.46
Roshay H.R. 2019	125	0.170	0.50	0.85
Balali.M. 2018	209	0.301	1.25	0.37
Maharaj.J. 2020	70	0.189	0.50	0.09
Proposed-1	50	0.140	0.50	0.07
Proposed-2	47	0.110	0.50	0.05

As per table-5 the proposed QCA RCA topology contains 50 and 47 number of cells and occupied area $0.14\mu m^2$ and $0.11\mu m^2$which is smallest in comparison with all existing designs.

Table 6. Performance Parameter Analogy of QCA 4×4 Vedic Multiplier Design Using FA

QCA Vedic Multiplier	Cell	Area (μm^2)	Latency (Clocking cycles)	Quantum Cost (Area*Latency)
Pooja V.G. 2018	1959	2.39	1.5	3.58
Safoyev, N. 2020	1726	1.74	5.25	9.13
Proposed-1	488	0.85	1.00	0.85
Proposed-2	470	0.79	1.00	0.79

As per table-6 the proposed QCA 4×4 Vedic Multiplier topology contains 488 and 470 number of cells and occupied area $0.85\mu m^2$ and $0.79\mu m^2$which is smallest as compared with all previous designs. The cost analysis of the proposed variousQCA 4×4Vedic multiplier topology using full adder is mentioned in Fig.21

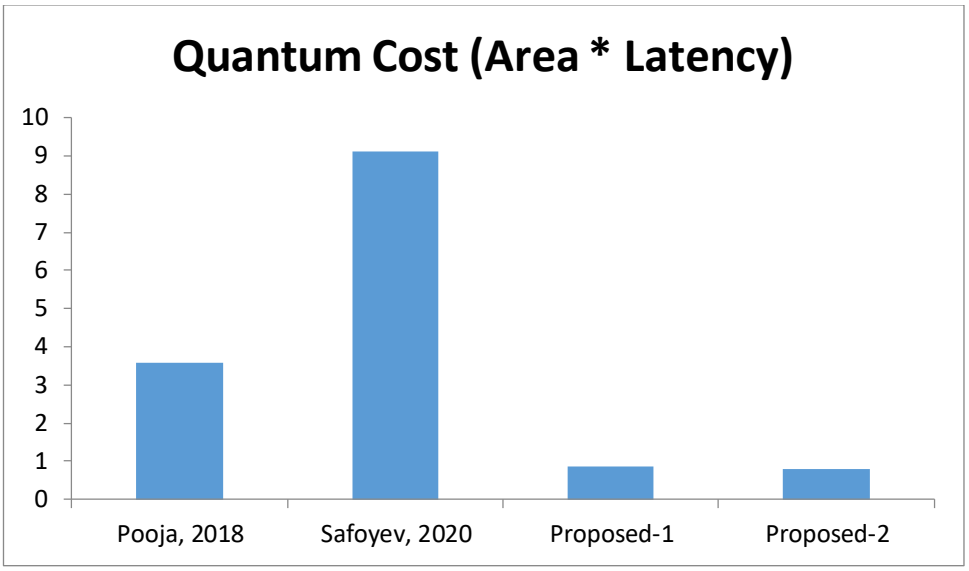


Figure21. Quantum Cost analysis of variousQCA 4×4Vedic multiplier topology using FA

Table 7. Performance Parameter Analogy of QCA 4×4 Vedic Multiplier Design Using RCA

QCA Vedic Multiplier	Cell	Area (μm^2)	Latency (Clocking cycles)	Quantum Cost (Area* Latency)
Pooja V.G. 2018	1959	2.39	1.5	3.58
Safoyev, N. 2020	1726	1.74	5.25	9.13
Proposed-1	1234	2.35	1.25	2.93
Proposed-2	897	1.79	1.00	1.79

Table.7 explained that the proposed QCA QCA 4×4 Vedic Multiplier Design Using RCA contains 1234 and 897 cell count and area 2.35 µm2 and 1.79 µm2 that is less as compare to other existing designs.

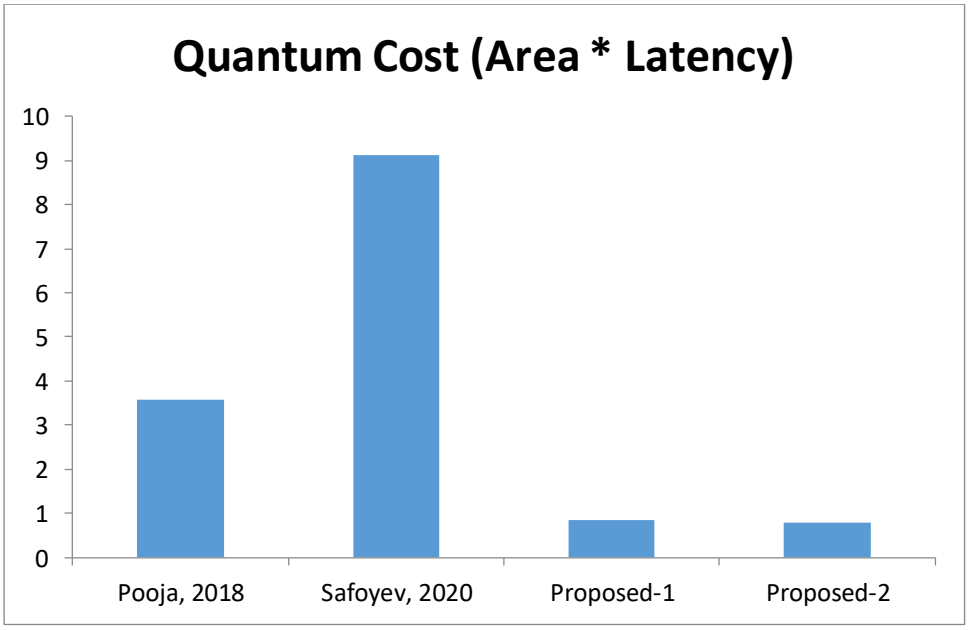


Figure22. Quantum Cost analysis of variousQCA 4×4Vedic multiplier topology using Full Adder

8. Energy Dissipation of Proposed 2×2 Vedic Multiplier

The kink energy dissipation is analyzed by considering various energy phases and calculated a Hamiltonian matrix using Hartree Fock approach, taking the Coulmbic interaction among QCA cells estimated by QCAPro tool. Energy dissipation of the suggested 2×2 Vedic Multiplier is calculated by QCADesigner E tool that is an extension of QCA Designer [14]. The parameters like is the energy dissipation in every cycle is E_bath_total, the total energy dissipation is Sum_bath, the average bath is Ab and average clock, energy dissipation is Ac while the simulation outcome as explained in Table.8. The suggested 2×2 Vedic Multiplier takes 15 iterations for the complete simulation process, the are explained by the equation (2)

$$H= \begin{bmatrix} -\frac{Ek}{2\sum_i Difi,j} & -\gamma \\ -\gamma & Ek\sum_i Cifi,j \end{bmatrix}$$

$$= \begin{bmatrix} -Ek/2(Cj-1+Cj+1) & -\gamma \\ -\gamma & Ek/2(Cj-1+Cj+1) \end{bmatrix} \quad (2)$$

The above equation suggested the energy dissipation where, polarization of ith compared cell is shown to by Ci and the geometrical calculation of the electrostatic interference among cells i and j is depicted by fi,j as the analytical separation where Ike is the kink energy among the cells. The kink energy dissipation at T=2K presented in a table is shown in Table 9.

Table 8. Energy dissipation in (Ev) of the Proposed 2×2 Vedic Multiplier

E_bath_total (Ebtx)	E_clk_total (Ectx)	E_Error_total (EEtx)	Sum_bath (Sb)	Avg_bath (Ab)	Sum_clk (Sc)	Avg_clk (Ac)
2.46e-003	2.02e-003	-1.72e-004				
4.14e-003	4.15e-003	-3.08e-004				
1.92e-003	1.09e-003	-1.28e-004				
3.20e-003	6.87e-003	-1.08e-004				
2.41e-003	6.59e-003	-1.85e-004	3.31e-002 (Er:-2.78e-003)	3.04e-003 (Er:-2.56e-004)	-4.19e-004	-5.21e-004
4.58e-003	4.93e-003	-4.00e-004				
1.89e-003	1.50e-003	-1.35e-004				
3.23e-003	4.79e-003	-4.12e-004				
3.10e-003	6.89e-004	-2.62e-004				
3.86e-003	3.65e-004	-3.39e-004				
2.53e-003	2.30e-004	-1.50e-004				

Table 9. Kink Energy Dissipation at T=2K of 2-bit Vedic Multiplier

2-bit Vedic Multiplier	0.5Ek(eV)	1.0Ek(eV)	1.5 Ek(eV)
Safoyev, N. 2020	0.07	0.09	0.12
Chudasama, A. 2018	0.10	0.12	0.15
Jeon J.C. 2021	0.06	0.08	0.10
Proposed-1	0.05	0.07	0.10
Proposed-2	0.04	0.06	0.11

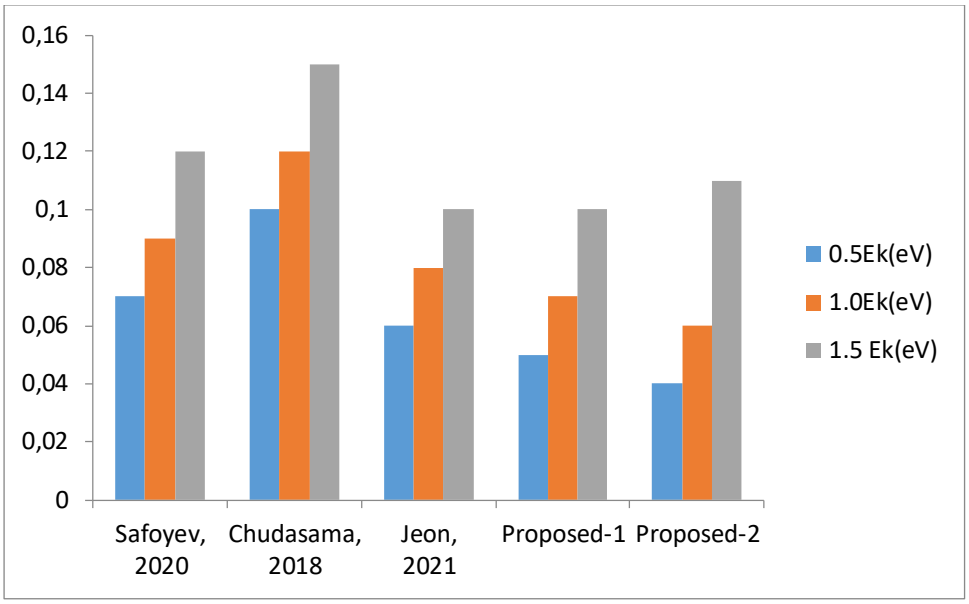


Figure 23. Average Kink energy dissipation of numerous 2 × 2 Vedic Multiplier

8.1. Energy Dissipation of Proposed 4×4 Vedic Multiplier

The suggested 4-bit QCA Vedic Multiplier takes 19 iterations for the complete simulation process. The energy dissipation is tabulated in Table-9

Table 9. Energy dissipation in (Ev) of the Suggested 4×4 Vedic Multiplier

E_bath_total (Ebtx)	E_clk_total (Ectx)	E_Error_total (EEtx)	Sum_bath (Sb)	Avg_bath (Ab)	Sum_clk (Sc)	Avg_clk (Ac)
2.76e-002	-2.28e-003	-2.05e-003				
2.94e-003	-2.15e-003	-2.35e-003				
2.82e-003	-2.04e-003	-2.21e-003				
3.00e-002	2.67e-003	-2.35e-003				
2.91e-003	2.58e-003	-2.35e-003	3.27e-001 (Er:-2.56e-002)	2.98e-002 (Er:-2.33e-003)	-2.80e-001	-2.55e-002
3.58e-002	-2.79e-003	-2.50e-003				
3.05e-002	-2.50e-003	-2.52e-003				
3.06e-002	-2.62e-003	-2.41e-003				
2.80e-002	-2.49e-003	-2.45e-003				
3.06e-002	2.45e-003	-2.26e-003				
2.93e-002	2.31e-003	-2.40e-003				

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As per the conventional formula of the calculation of majority gate and number of inverters used in various multiplier is tabulated in table 10 and the parameter comparison is explained in Fig.24 and Fig.25

Table.10 Performance comparison of Various 4- bit QCA Multipliers designs

4- bit Multiplier Design	Majority Gate Count	Inverter Count
Wallace	52	21
Dadda	52	21
Array I	52	21
Array II	64	32
Vedic	64	16
Proposed Vedic	48	16

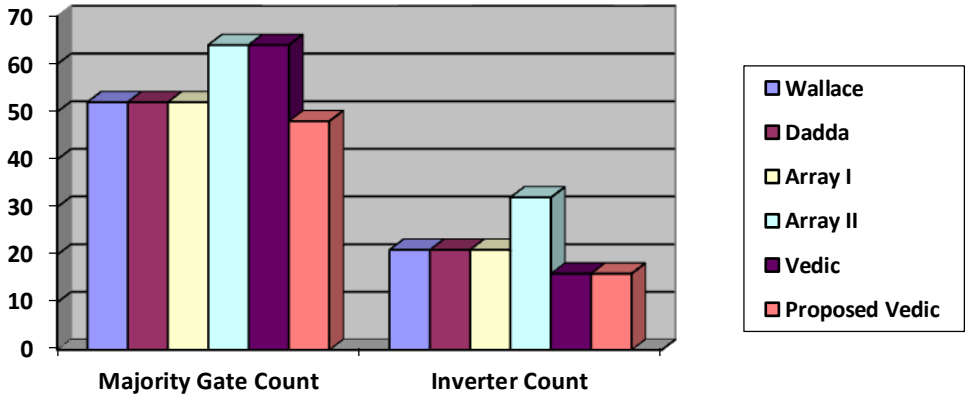

Figure.24 Performance comparison of majority gate and inverter count in various 4-bit multiplier

Table.11. Performance comparison of Various 8- bit QCA Multipliers designs

8- bit Multiplier Design	Majority Gate Count	Inverter Count
Dadda	232	105
Wallace	256	113
Array I	232	105
Array II	256	128
Vedic 8×8	313	83
Proposed Vedic	249	83

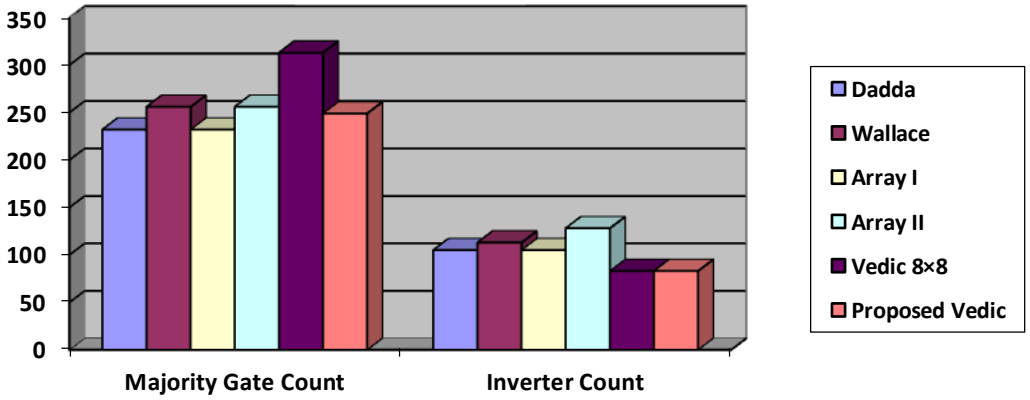

Figure.25 Performance comparison of majority gate and inverter count in various 8-bit multiplier

Table.12 Performance comparison of Various n-bit QCA Multipliers designs

n- bit Multiplier Design	Majority Gate Count	Inverter Count
Dadda	n$\times$(4n-3)	n$\times$(2n-3)+1
Array I	n$\times$(4n-3)	n$\times$(2n-3)+1
Array II	4$\times$(N^2)	2$\times$(N^2)
Vedic	$[4 \times (Maj.n/2 \times n/2)] + [3 \times (\frac{9n}{2} - 1)]$	$[4 \times Inv.(\frac{n}{2} \times \frac{n}{2})] + (\frac{9n}{2} - 1)$
Proposed Vedic	$[4 \times (Maj.n/2 \times n/2)] + [3 \times (\frac{5n}{2} - 1)]$	$[4 \times Inv.(\frac{n}{2} \times \frac{n}{2})] + (\frac{5n}{2} - 1)$

9. CONCLUSION

Moore's law suggests, the chip design industry has advanced remarkably up to nano scale. QCA is a nano architecture computation method for digital circuitry designing. The chip plan industry has advancement over conventional CMOS in the contemporary era and prove to be modified alternative than past automation methods. Quantum computing, molecular computing power efficient nano computation are few transformative nanotechnologies implemented based on Coulamb's repulsion. This paper offered an optimum approach to implementing all proposed circuits. QCA is a worthy and reliable alternative to CMOS technology at a nano scale as of less power consumption, higher speed and higher density devices. The suggested layouts have further reduced the area, which illustrate to be a finest overseeing when considered broad circuits like processors, ALU, etc. In addition the usual environment of QCA rationale encourages the reversal work impartial thereby heightening the speedy function within the tera hertz extend, it is overseen that the proposed QCA 2×2 Vedic Multiplier architectures constructed up of ultra effective QCA half adder combinations using QCA Designer tool to realize efficient and optimum QCA 2×2 binary Vedic multiplier for nano computing. In this paper, we proposed an ultra efficient, less complex Vedic 2×2 and 4×4 multiplier topology with the help of proposed ultra efficient Half Adder(HA), Full Adder (FA) followed by 4×4 Vedic multiplier using QCADesigner simulation environment for less energy and fast speed nano computing application. The proposed QCA 2×2 Vedic multiplier design shown 37.62% improvement in QCA cell count and 4×4 Vedic multiplier design shown 71.72% improvement in cell counts as well as 29.62% area is decreased for 2×2 QCA Vedic multiplier and 43.38% area decreased from 4×4 QCA Vedic multiplier as related to its best existing designs.

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